Preliminary Datasheet

High-Performance Processor

Advanced Digital Chips, Inc.

adStar-L

Hardware Manual

Rev. 1.2

December 21, 2017

Subject to Change Without Notice.

Office

Korea (Headquarters)
22F, Bldg A, Keumkang Penterium IT Tower,
810 Gwanyang-dong, Dongan-gu, Anyang-si,
Gyeonggi-do, 431-060, Korea
T : +82-31-463-7500 / F : +82-31-463-7588
E-mail : eisc@adc.co.kr
http://www.adc.co.kr

China
Peak Microtech Co., Ltd
北京芯首电子科技有限公司
E-mail : sales@peaktech.com.cn
http://www.peaktech.com.cn

Contents

Figures

Tables

History

Ver 1.0
June 29, 2017 1st version released

Ver 1.1
December 5, 2017 Correc the descerription of the ADC

1 DESCRIPTIONS AND FEATURES

1.1 General Description

adStar-L is a 32-bit micro-controller that has maximum 120HMz operation frequency. Especially, an embedded memory system of the *adStar-L* supports a flash memory as well as a SDRAM. Due to that reason, programmer can apply variable applications to the *adStar-L.*

PART NAME	FLASH	SDRAM
adStar-L8M	-	8MB
adStar-L8MF512	512KB	8MB
adStar-L16M	-	16MB
adStar-L16MF512	512KB	16MB

The *adStar-L* operates with off-chip or on-chip connected Quad Flash. The flash memory can be used as both a program memory and a data memory. The *adStar-L* can access the flash memory by configuring Quad-data bit for high speed. In addition, Serial Debugger lets developers download a program with high speed.

A CPU of the *adStar-L* has separated bus architecture to access data and program memory (Harvard Architecture), and is implemented as 5-stage pipeline EISC architecture which provides fast instruction execution.

A LCD controller that is organized as additional hardware supports RGB888 and RGB565. In addition the LCD controller of the *adStar-L* provides maximum 800 x 600 resolution, Graphic Library, and JPEG Decoding with hardware logic. The *adStar-L* is the best solution for smart application with the resolution and supported libraries.

Additionally, MP3 Decoding Library and Sound Mixer can be used for voice, sound effects, and background sound. 4-channel 12-bit ADC (1MSPS) can convert analog data of sensor or external input into digital.

Also, the *adStar-L* can expand Flash memory and SD card manually. Especially, in the case of the NAND flash memory, by adapting SLC Type as well as 24-bit ECC, developers can reduce entire system design cost

The *adStar-L* provides USB 1.1 Full-Speed Device/Host, 2-channel UART, 1-channel SPI_LCD, 1-channel SPI, Sound Mixer, TWI for communication and power management modes.

. In the case of 8-channel DMA provides more fast communication than others.

The *adStar-L* can be applied into Smart application of smart appliances, GUI (Graphical User Interface) of factory automation system with LCD, Access control system, Smart Greed, Sign pad, printer, POS, Barcode system, POP monitor, and etc.

Developers can download GCC based EISC compiler, software toolchain (assembler, linker, debugger), EISC Studio (IDE: Integrated Development Environment for EISC), Reference Circuit Schematics, software libraries, and example codes from ADChips homepage (http://www.adchips.co.kr) without any restriction. In addition, developers can purchase development board (test board), and E-con (download/debugging tool) with reasonable price. As mass product tool, we provide two writing methods. One is 8-socket GANG-writer that can write to the chips before packing. The other is stand-alone type EISC HANDY that can write to the chip by using target board's power.

1.2 Features

▫ **High-performance, Low-power 32-bit EISC Microprocessor**

▫ **32-bit EISC Architecture**
AE32000C-Lucida
Harvard Architecture
5-Stage Pipelining
1 Cycle 32bit MAC
Up to 120MIPS Throughput at 120MHz
8KB 2-way Instruction Cache
8KB 2-way Data Cache
Serial Wire Debugger

▫ **Embedded Memory**
2KBytes Internal SRAM for Instruction
1KBytes Internal SRAM for Data
8/16Mbytes SDRAM
Optional 512KBytes Flash (More than 100,000 erase/program cycles)

▫ **External Memory Interface**
8-bit NAND Flash Interface supports SLC and MLC (4/24-bit ECC) type

▫ **Boot Modes**
NAND Flash Booting
Serial Flash Booting

▫ **SWD Interface**
Extensive On-chip Debug Support
Programming of Serial Flash, other Ram

▫ **LCD Controller**
RGB 888 or 565 output
Supports up to 800 x 600 resolution display in RGB mode

▫ **SPI_LCD Interface**
Support 9bit data transfer for lcd control

▫ **USB 1.1 Full-Speed Device/Host Compatible**
Supports Full-speed Data Rate 12Mbps

▫ **SD-Card Interface**
Supports single/quad

▫ **Sound Mixer**
4ch mixing
1-ch PWM output for Stereo or 2-chPWM output for mono (1-CH Digital Modulator)

▫ **RTC**
Support RTC counter (hour, minute, second) and calendar counter(year, month, day, week)
Support Alarm counter (month, day, hour, minute, second)
Support periodic time tick interrupt with 14 period options
1/4sec, 1/2sec, 1sec, 2sec, 4sec, 12sec, 1min, 2min,4min, 16min, 1hour, 2hour, 4hour, 24hour
Support wake-up function

▫ **Other Peripherals**
32-bit Watchdog Timer
6-ch DMA
Interrupt Controller with 2 External IRQ
2 Channel 16-bit Timer/Counter with 15-bit Pre-scaler, Capture, PWM
2 Channel UART with 16Bytes FIFO, Functionally compatible with the 16550, with 1Channel IrDA
1 Channel Master/Slave SPI with 8Bytes FIFO
1 Channel TWI
Auto ECC NAND Flash Controller: 4-bit/24-bit ECC Support, Auto Booting with ECC Support
55-Port In/Out with open drain mode
55-Port GPIO
JPEG Decoder

▫ **Analog IPs**
12-bit 1MSPS SAR ADC with 4 analog input channels
POR (Power On Reset)
LDO
PLL x 2

▫ **Operating frequency**
Up to 120MHz

▫ **Power**
3.0V to 3.6V

▫ **Operating Temperature**
-40℃ / +85℃

▫ **Package**
100-Pin QFP (14mm x 14mm)

2 BLOCK DIAGRAM & PIN DESCRIPTIONS

2.1 Block Diagram

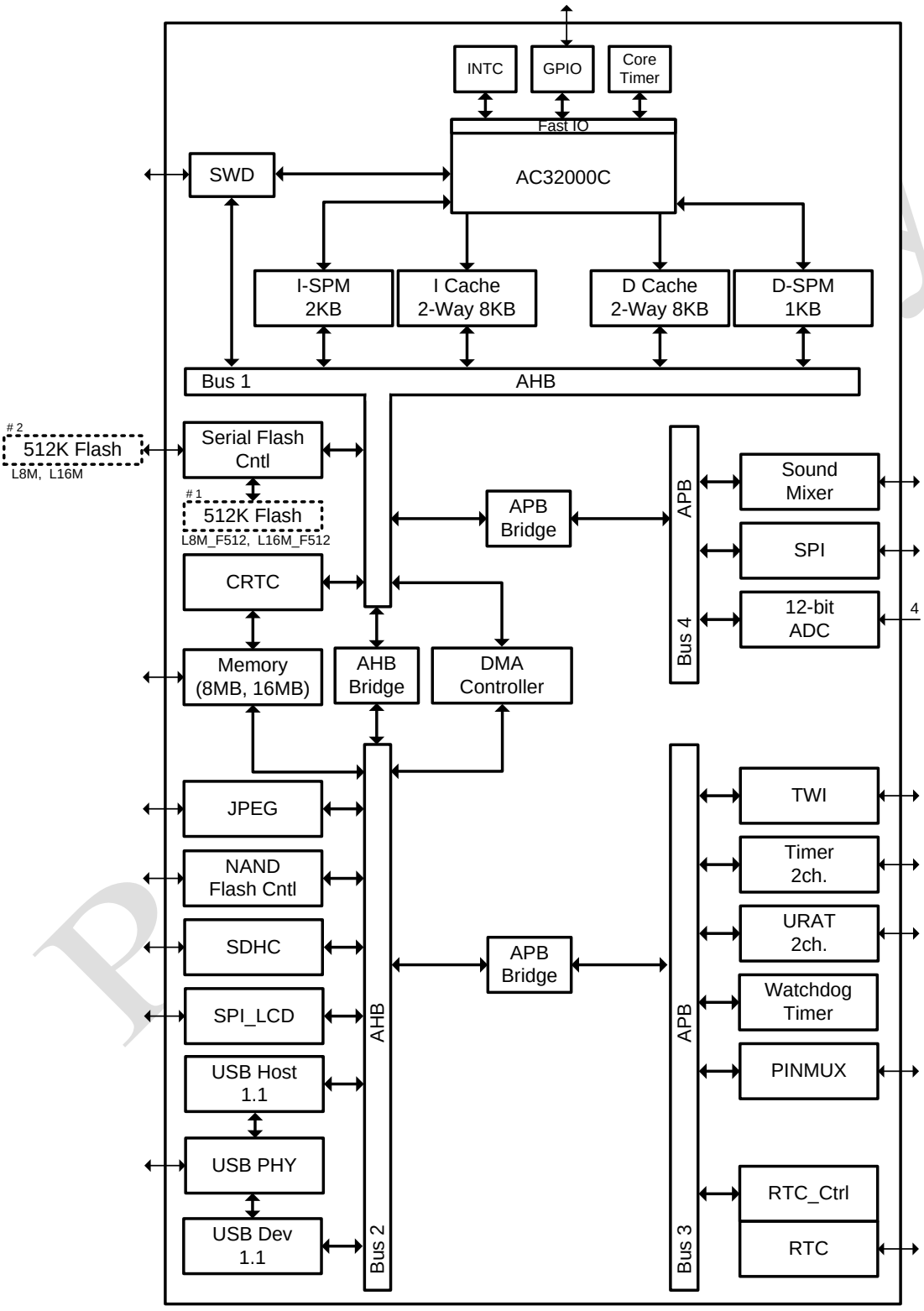


Figure 2-1 adStar-L Block Diagram

2.2 Pin Layout

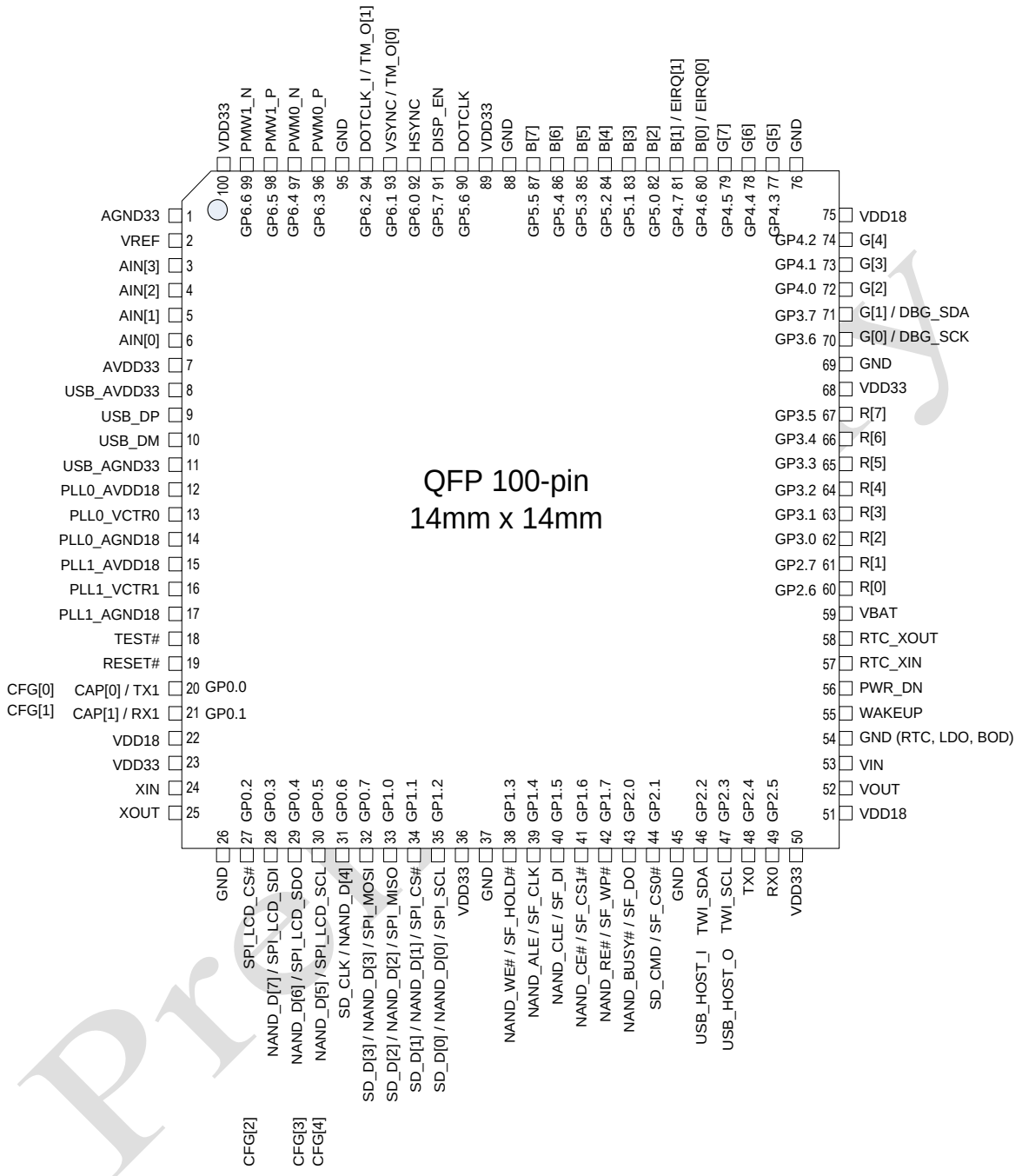


Figure 2-2 adStar-L Pin Layout

2.3 Pin Definition

Table 2-1 adStar-L Pin Definitions 100-Pin

No.	Pin Name	Alt CFG	Description.	Type	Output Drive Current	Pull-Up / Pull-Down
1	AGND33		ADC power ground	In		
2	VREF		ADC analog voltage input reference	In		
3	AIN[3]		ADC analog voltage input channel 3	In		
4	AIN[2]		ADC analog voltage input channel 2	In		
5	AIN[1]		ADC analog voltage input channel 1	In		
6	AIN[0]		ADC analog voltage input channel 0	In		
7	AVDD33		ADC power supply 3.3 V	In		
8	USB_AVDD33		USB power supply 3.3 V	In		
9	USB_DP		USB DP - data+ pin	Bidi		
10	USB_DM		USB DM - data- pin	Bidi		
11	USB_AGND33		USB power ground	In		
12	PLL0_AVDD18		PLL0 power supply 1.8V	In		
13	PLL0_VCTR0		Vco control voltage of pll0, corresponding LPF should be connected here	In		
14	PLL0_AGND18		Power ground	In		
15	PLL1_AVDD18		PLL1 power supply 1.8V	In		
16	PLL1_VCTR		vco control voltage of pll1, corresponding LPF should be connected here	In		
17	PLL1_AGND18		Power ground	In		
18	TEST#		Test mode entrance active low	In		
19	RESET#		Reset of system active low	In		
20	UART_TX1	0	Uart tx [1]	Bidi		
	CAP_IN0	1	Timer capture [0]			
	CFG[0]	3	Booting mode select [0]			
	GP0.0		General purpose I/O			
21	UART_RX1	0	Uart rx [1]	In		
	CAP_IN1	1	Timer capture [1]			
	CFG[1]	3	Booting mode Select [1]			
	GP0.1		General purpose I/O			
22	VDD18		Core power supply 1.8V	In		
23	VDD33		IO power supply 3.3V	In		
24	XIN		Oscillator xin	In		
25	XOUT		Oscillator xout	Out		
26	GND		Power gournd	Out		
27	SPI_LCD_CS#	0	SPI_LCD chip select signal [1]	In		
	CFG[2]	3	Booting mode Select [2]			
	GP0.2		General purpose I/O			
28	SPI_LCD_SDI	0	SPI data input [1]	Bidi	8mA	up, down or disable
	NAND_D[7]	1	Nand flash data [7]			
	GP0.3		General purpose I/O			
29	SPI_LCD_SDO	0	SPI_LCD data output [1]	Bidi	8mA	up, down or disable
	NAND_D[6]	1	Nand flash data [6]			
	CFG[3]	3	Booting mode select [3]			
	GP0.4		General purpose I/O			
30	SPI_LCD_SCL	0	SPI_LCD clock [1]	Bidi	8mA	up, down or disable
	NAND_D[5]	1	Nand flash data [5]			
	CFG[4]	3	Booting mode select [4]			
	GP0.5		General purpose I/O			
31	NAND_D[4]	1	Nand flash data [4]	Bidi	8mA	up, down or disable
	SD_CLK	2	SD card clock			
	GP0.6		General purpose I/O			
32	SPI_MOSI	0	When SPI is configured to master, It used for data output, otherwise, data input	Bidi	8mA	up, down or disable
	NAND_D[3]	1	Nand flash data [3]			
	SD_DATA[3]	2	SD card data [3]			
	GP0.7		General purpose I/O			
33	SPI_MISO	0	When SPI is configured to master, It used for data input, otherwise, data output	Bidi	8mA	up, down or

	NAND_D[2]	1	Nand flash data [2]			disable
	SD_DATA[2]	2	SD card data [2]			
	GP1.0		General purpose I/O			
34	SPI_CS#	0	SPI chip select signal [0]	Bidi	8mA	up, down or disable
	NAND_D[1]	1	Nand flash data [1]			
	SD_DATA[1]	2	SD card data [1]			
	GP1.1		General purpose I/O			
35	SPI_SCL	0	SPI clock [0]	Bidi	8mA	up, down or disable
	NAND_D[0]	1	Nand flash data [0]			
	SD_DATA[0]	2	SD card data [0]			
	GP1.2		General purpose I/O			
36	VDD33		IO power supply 3.3V	In		
37	GND		IO power ground	In		
38	SF_HOLD#	0	Serial flash hold signal	Bidi		
	NAND_WE#	1	Nand write enable			
	GP1.3		General purpose I/O			
39	SF_CLK	0	Serial flash clock	Bidi	8mA	up, down or disable
	NAND_ALE	1	Nand address latch enable			
	GP1.4		General purpose I/O			
40	SF_DI	0	Serial flash data Input	Bidi	8mA	up, down or disable
	NAND_CLE	1	Nand command latch enable			
	GP1.5		General purpose I/O			
41	SF_CS1#	0	Serial flash chip select 1			up, down or disable
	NAND_CE#	1	Nand chip enable			
	GP1.6		General purpose I/O			
42	SF_WP	0	Serial flash write protection signal	Bidi	8mA	up, down or disable
	NAND_RE#	1	Nand read enable			
	GP1.7		General purpose I/O			
43	SF_DO	0	Serial flash data out. data output signal.	Bidi		up, down or disable
	NAND_BUSY	1	Nand busy check			
	GP2.0		General purpose I/O			
44	SF_CS0#	0	Serial flash chip select 0	Bidi		up, down or disable
	SD_CMD	1	SD card command			
	GP2.1		General purpose I/O			
45	GND		Power ground	Bidi		
46	TWI_SDA	0	TWI data line	Bidi	8mA	up, down or disable
	USB_HOST_IN	1	USB host input			
	GP2.2		General purpose I/O			
47	TWI_SCL	0	TWI clock line	Bidi		up, down or disable
	USB_HOST_OUT	1	USB host output			
	GP2.3		General purpose I/O			
48	UART_TX0	0	Uart tx [0]	Bidi	8mA	up, down or disable
	GP2.4		General purpose I/O			
49	UART_RX0	0	Uart rx [0]	Bidi	8mA	up, down or disable
	GP2.5		General purpose I/O			
50	VDD33		IO power supply 3.3V	In		
51	VDD18		Core power supply 1.8V	In		
52	VOUT		LDO voltage output 1.8V	Out		
53	VIN		LDO voltage input 3.3V	In		
54	GND		Power ground	In		
55	WAKEUP		System wake up signal	In		
56	PWR_DN		System power down signal	Out		
57	RTC_XIN		RTC oscillator xin	In		
58	RTC_XOUT		RTC oscillator xout	Out		
59	VBAT		Battery voltage input	In		
60	R[0]	0	LCD red out [0]	Bidi	8mA	up, down or disable
	GP2.6		General purpose I/O			
61	R[1]	0	LCD red out [1]	Bidi	8mA	up, down or disable
	GP2.7		General purpose I/O			
62	R[2]	0	LCD red out [2]	Bidi	8mA	up, down or disable
	GP3.0		General purpose I/O			
63	R[3]	0	LCD red out [3]	Bidi	8mA	up,

	GP3.1		General purpose I/O			down or disable
64	R[4]	0	LCD red out [4]	Bidi	8mA	up, down or disable
	GP3.2		General purpose I/O			
65	R[5]	0	LCD red out [5]	Bidi	8mA	up, down or disable
	GP3.3		General purpose I/O			
66	R[6]	0	LCD red out [6]	Bidi	8mA	up, down or disable
	GP3.4		General purpose I/O			
67	R[7]	0	LCD red out [7]	Bidi	8mA	up, down or disable
	GP3.5		General purpose I/O			
68	VDD33		IO power supply 3.3V	In		
69	GND		Power ground	In		
70	G[0]	0	LCD green out [0]	Bidi	8mA	up, down or disable
	DBG_SCK	1	Debugger clock			
	GP3.6		General purpose I/O			
71	G[1]	0	LCD green out [1]	Bidi	8mA	up, down or disable
	DBG_SDA	1	Debugger data			
	GP3.7		General purpose I/O			
72	G[2]	0	LCD green out [2]	Bidi	8mA	up, down or disable
	GP4.0		General purpose I/O			
73	G[3]	0	LCD green out [3]	Bidi	8mA	up, down or disable
	GP4.1		General purpose I/O			
74	G[4]	0	LCD green out [4]	Bidi	8mA	up, down or disable
	GP4.2		General purpose I/O			
75	VDD18		Core power supply 1.8V	In		
76	GND		Power ground	In		
77	G[5]	0	LCD green out [5]	Bidi	8mA	up, down or disable
	GP4.3		General purpose I/O			
78	G[6]	0	LCD green out [6]	Bidi	8mA	up, down or disable
	GP4.4		General purpose I/O			
79	G[7]	0	LCD green out [7]	Bidi	8mA	up, down or disable
	GP4.5		General purpose I/O			
80	B[0]	0	LCD blue out [0]	Bidi	8mA	up, down or disable
	EIRQ0	1	External interrupt [0]			
	GP4.6		General purpose I/O			
81	B[1]	0	LCD blue out [1]	Bidi	8mA	up, down or disable
	EIRQ1	1	External interrupt [1]			
	GP4.7		General purpose I/O			
82	B[2]	0	LCD blue out [2]	Bidi	8mA	up, down or disable
	GP5.0		General purpose I/O			
83	B[3]	0	LCD blue out [3]	Bidi	8mA	up, down or disable
	GP5.1		General purpose I/O			
84	B[4]	0	LCD blue out [4]	Bidi	8mA	up, down or disable
	GP5.2		General purpose I/O			
85	B[5]	0	LCD blue out [5]	Bidi	8mA	up, down or disable
	GP5.3		General purpose I/O			
86	B[6]	0	LCD blue out [6]	Bidi	8mA	up, down or disable
	GP5.4		General purpose I/O			
87	B[7]	0	LCD blue out [7]	Bidi	8mA	up, down or disable
	GP5.5		General purpose I/O			
88	GND		Power ground	In		
89	VDD33		IO power 3.3V	In		
90	DOTCLK	0	LCD clock output	Bidi	8mA	up,

	GP5.6		General purpose I/O			down or disable
91	DISP_EN	0	Display enable	Bidi	8mA	up, down or disable
	GP5.7		General purpose I/O			
92	HSYNC	0	Signal for horizontally synchronization	Bidi	8mA	up, down or disable
	GP6.0		General purpose I/O			
93	VSYNC	0	Signal for vertically synchronization	Bidi	8mA	up, down or disable
	TM_OUT0	1	Timer pwm output [0]			
	GP6.1		General purpose I/O			
94	LCD_CLK_IN	0	Clock input (lcd controller)	Bidi	8mA	up, down or disable
	TM_OUT1	1	Timer pwm output [1]			
	GP6.2		General purpose I/O			
95	GND		Power ground	In		
96	PWM0_P	0	GP6.3 (sound pwm positive output channel 0)	Bidi	8mA	up, down or disable
	GP6.3		General purpose I/O			
97	PWM0_N	0	GP6.4 (sound pwm negative output channel 0)	Bidi	8mA	up, down or disable
	GP6.4		General purpose I/O			
98	PWM1_P	0	GP6.5 (sound pwm positive output channel 1)	Bidi	8mA	up, down or disable
	GP6.5		General purpose I/O			
99	PWM1_N	0	GP6.6 (sound pwm negative output channel 1)	Bidi	8mA	up, down or disable
	GP6.6		General purpose I/O			
100	VDD33		IO power supply 3.3V	In		

* Alt CFG is a number that corresponds to the pin mux settings.

2.4 Pin Description

VDD33, AVDD33, USB_AVDD33 : Independent 3.3V Supply and not connected each other.
PLL0_AVDD18, PLL1_AVDD18 : 1.8V Supply.
VDD18 : 1.8v Supply.

AGND33 : ADC Power Ground **.**
USB_AGND33 : USB Power Ground.
PLL0_AGND18 , PLL1_AGND18 : PLL Power Ground.
GND : Power Ground.

TEST# : Chip Test pin (Active Low)
When this pin is configured as set `Active low`, All pins serve as 3rd function (TEST MODE) through PinMux.
To enter operating mode, this pin must be set to `active high`.

CFG[4:0] : Booting Mode Select (Refer to 3.4 Boot Mode)
This Booting Mode Selection provides to choose several Booting Modes such as Flash booting, Nand Flahs booting etc

AIN[3:0] : This pin is for analog voltage level and it convert digital value (4-channel).

VREF : This pin is for reference voltage level of AIN input.

USB Pins: USB Shares USB Device and Host (Refer to 4.4.14 USB PHY Control Register).
USB_DP : USB Data+ I/O.
USB_DM : USB Data- I/O.

EIRQ0, EIRQ1 : External Interrupt Request Input Pins (8 Interrupt Controller).
Supporting external interrupt.

Serial Flash (Refer to 5 Flash Memory Controller).
SF_CS0#, SF_CS1# : Serial Flash Chip Selection.
SF_CLK, : Serial Flash Clock.
SF_DI : Serial Flash Data Input (Command, Address, Data input signal)..
SF_DO : Serial Flash Data Out. Data output signal.
SF_WP : Serial Flash write protection signal.
SF_HOLD : Serial Flash hold signal.

NAND Flash (Refer to 17 NAND Flash Controller).
NAND_CE: NAND Flash Chips Enable. It is used for NAND Flash activation.
NAND_ALE : NAND Flash Address Latch Enable. Sends an address to the NAND Flash..

NAND_CLE: NAND Flash Command Latch Enable. Sends a command to the NAND Flash.
NAND_WE# : NAND Flash Write Enable. Stores data into NAND Flash.
NAND_RE# : NAND Flash Read Enable. Reads data from NAND Flash.
NAND_BUSY# : NAND Flash Busy signal input pin. If the state of NAND Flash is Busy, the value of the pin is 0.
NAND_D[7:0] : NAND Flash 8-bit Data I/O.

LCD Controller : RGB 888 output. Provides 800x600 resolution (Refer to 24 TFT LCD Controller).
LCD_CLK_IN : Clock Input (LCD Controller).

VSYNC : Signal for vertical synchronization.

HSYNC : Signal for horizontal synchronization.

DISP_EN : Display Enable.
DOTCLK : LCD Clock Output.
R[7:0] : Red Output 8-bit.

G[7:0] : Green Output 8-bit.
B[7:0] : Blue Output 8-bit.

PWM/Capture : 2 channels (Refer to 11 Timer).
TM_OUT0, TM_OUT1 : PWM Output.
CAP_IN0, CAP_IN1 : Capture Input. Input pin to measure period and pulse width of external signal.

SPI : 1 channel (Refer to 20 SPI).
SPI_CS# : SPI Chip select signal.
SPI_SCK : SPI Clock pin.
SPI_MISO : When SPI is configured to Master, It used for Data input, otherwise, Data output.
SPI_MOSI : When SPI is configured to Master, It used for Data output, otherwise, Data input.

SPI_LCD : 1 channel (Refer to 19 SPI_LCD).
It controlled 9bit SPI interface LCD module.
SPI_LCD_CS# : SPI Chip select signal.
SPI_LCD_SCK : SPI Clock pin.
SPI_LCD _SDI : SPI Data input.
SPI_LCD _SDO : SPI Data output.

TWI (Refer to 21 TWI).
TWI_SCL : TWI Serial Clock.
TWI_SDA : TWI Serial Data.

UART : 2 channels.
Channel 0 is for UART only. Channel 1 supports IrDA.

UART_RX0 : UART RX.
UART_TX0 : UART TX.
UART_RX1 : UART RX with IrDA supported.
UART_TX1 : UART TX with IrDA supported.

Sound Mixer : Digital Modulator 2 channels (Refer to 22 Sound Mixer).
PWM_P0, PWM_N0, PWM_P1, PWM_N1
: Sound Mixer Digital Modulator PWM output.
These pins are used for either Mono Sound mode or Stereo Sound mode. The Mono mode and The Stereo are enabled to apply 2 channels and 1 channel respectively.

XIN, XOUT : It connected to external 2Mhz crystal. Circuit diagram is shown in the figure below.

3 MEMORY ARCHITECTURE AND BOOTING MODES

3.1 Memory Map

The memory map is designed as following figure 3-1.

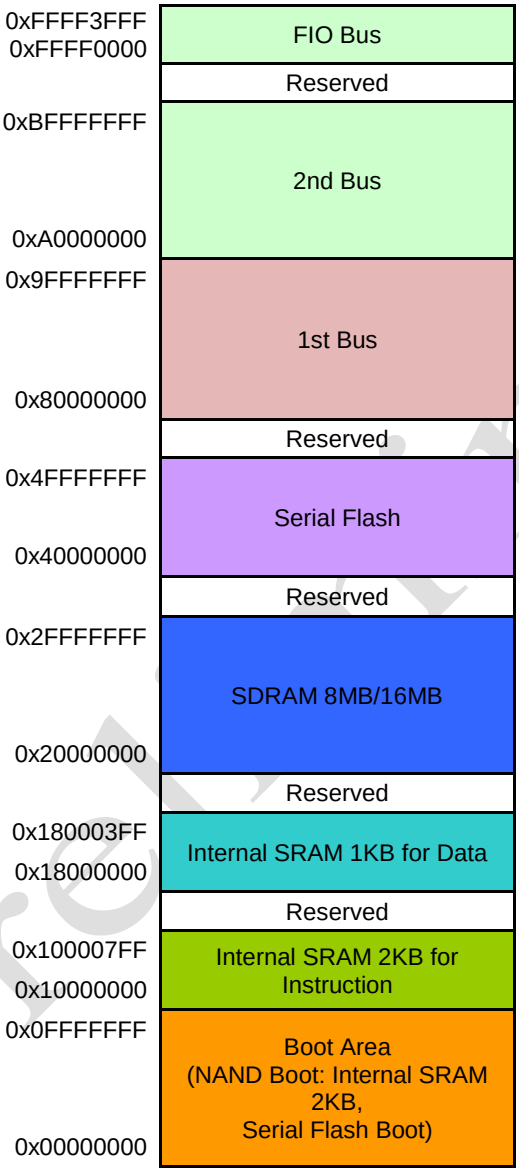


Figure 3-1 Memory Map

3.2 Embedded Memories

2KB Internal SRAM for Instruction
1KB Internal SRAM for Data

3.2.1 Internal SRAM for Instruction

adStar-L contains 2KB SRAM memory for instruction. The SRAM memory can be used to store instruction or data, and mainly it is used as instruction memory. In the case of reading an instruction, the SRAM memory access latency is 1-cycle and data read latency is 3-cycle.

3.2.2 Internal SRAM for Data

adStar-L contains 1KB SRAM memory for data. The data SRAM memory is used to store data, and its access latency is 1-cycle.

3.2.3 Internal SRAM Registers

adstar-L has Global Control Register which controls whole Internal SRAM. In addition, Internal SRAM can be configured as several Banks. For this reason, Local Register Set has as much as Bank numbers which are determined by Global Register configuration. Local Register Set is Composed of three 32bit Register as follow

- Local Internal SRAM Control Register
- Local Internal SRAM Start Address
- Local Internal SRAM End Address

Internal SRAM Global Control Register

Address : 0x700 - Global Control Register

Bit	*R/W*	*Description*	*Default*
31 : 28	R	Exception Status 4'b0001 : DATA Access Violation 4'b0010 : Instruction Access Violation	0h
27 : 24	R	Reserved	0h
23 : 20	R	iBank Size: Physical memory size of each bank of internal SRAM for instruction 4'h0 : 1 KB 4'h1 : 2 KB 4'h2 : 4 KB 4'h3 : 8 KB 4'h4 : 16 KB 4'h5 : 32 KB 4'h6 : 64 KB 4'h7 : 128 KB 4'h8 : 256 KB	
19 : 16	R/W	iSRAM Configuration 4'h0 : user is recognized as one chunk of memory 4'h1 : Reserved 4'h2 : user is recognized as four memory chunks (If more than four are currently not supported)	0h
15 : 12	R	iSRAM Enable 4'b0001 : SRAM Enable 4'b0000 : SRAM Disable	0h
11 : 8	R	dBank Size: Physical memory size of each bank of internal SRAM for data 4'h0 : 1 KB 4'h1 : 2 KB 4'h2 : 4 KB 4'h3 : 8 KB 4'h4 : 16 KB 4'h5 : 32 KB 4'h6 : 64 KB 4'h7 : 128 KB 4'h8 : 256 KB	
7 : 4	R/W	dSRAM Configuration 4'h0 : user is recognized as one chunk of memory 4'h1 : Reserved 4'h2 : user is recognized as four memory chunks (If more than four are currently not supported)	0h
3 : 0	R	dSRAM Enable 4'b0001 : SRAM Enable 4'b0000 : SRAM Disable	0h

Internal SRAM Local Control Register

Address : 0x701, 0x711 - Local iSRAM Control Register
Address : 0x704 - Local dSRAM Control Register

Bit	R/W	Description	Default
31 : 12	R	Reserved	0h
11 : 8	R	External Access: BUS Access Permission 4'h0 : External Access Not Support 4'h1 : External Access Support	
7 : 4	R/W	Privilege Mode: User Permission 4'h0 : Supervisor only Access 4'h1 : Supervisor/User Access	0h
3 : 0	R	Enable 4'b0001 : Local SRAM Enable 4'b0000 : Local SRAM Disable	0h

Internal SRAM Local Start Address Register

Address : 0x702, 0x712 - Local iSRAM Start Register
Address : 0x705 - Local dSRAM Start Register

Bit	R/W	Description	Default
31 : 0	R/W	SRAM Start Address	0h

Internal SRAM Local End Address Register

ADDRESS : 0x703, 0x713 - Local iSRAM End Register
ADDRESS : 0x706 - Local dSRAM End Register

Bit	R/W	Description	Default
31 : 0	R/W	SRAM End Address	0h

3.2.4 Internal SRAM Register Setting

Internal SRAM Register can be set through GAP (General Access Pointer). Using MVTC and MVFC that are co-processor register access instruction allow GAP to be used.

예제.

```
//#########################################################
//## Internal SRAM Global Register Setting
//#########################################################
asm(“ ldi 0x700,          %r0”);
asm(“ mvtc 0x0,           %r3”);
asm(“ ldi 0x00021021,     %r0”); //#ON //#Num of Memory Bank: 4
asm(“ mvtc 0x0,           %r4”);
```

3.3 Peripheral Memory Map

The register space is from 8000_0000h, and the size of each functional block is 1Kbyte.
The memory map is shown in Table 3-1.

Table 3-1 Peripheral Memory Map

Offset Address	*Block*	*BUS*	*Remark*
0x8000_0000	Flash Controller	1st AHB	
0x8000_0400	SDRAM Controller		
0x8000_0800	Reserved		
0x8000_0C00	Reserved		
0x8000_1000	Reserved		
0x8000_1400	DMA Controller		
0x8002_0000	Watchdog Timer	1st APB	
0x8002_0400	Timer		2 Channels
0x8002_0800	UART (2nd ch. IrDA)		2 Channels
0x8002_0C00 ~0x8002_17FF	Reserved		
0x8002_1800	TWI		
0x8002_1C00 ~0x8002_23FF	Reserved		
0x8002_2400	CRTC		
0x8002_2800 ~0x8002_33FF	Reserved		
0x8002_3400	Pin Mux		
0x8002_3800	RTC		
0x8002_3C00	System Control		
0x8003_0000 ~0x8003_FFFF	Reserved		
Offset Address	*Block*	*BUS*	*Remark*
0xA000_0000	USB Host	2nd AHB	
0xA000_0400	Reseved		
0xA000_0800	SPI_LCD		
0xA000_0C00	NAND Flash Controller		
0xA000_1000	SDHC		
0xA000_1400	Reserved		
0xA000_1800	USB Device		
0xA002_1000	SPI	2nd APB	
0xA002_1400	Reserved		
0xA002_1800	Reserved		
0xA002_1C00	Sound Mixer		
0xA002_2000 ~0xA002_37FF	Reserved		
0xA002_3800	ADC Controller		12-bit ADC
0xA002_3C00	Reserved		
0xA003_0000 ~0xA003_FFFF	Reserved		
0xffff_0000(1)	Interrupt Controller		
0xffff_1000(1)	Core Timer		
0xffff_3000(1)	GPIO		

(1) These regions (highlighted in green) are decoded internally by the CPU and are not physically connected to the bus, so they are not accessed by the other masters.

3.4 Boot Modes

When the External Reset release, CFG[4:0] pin voltage Level determined booting mode and go into that mode. Configuration pin assignment order as follow.

Table 1-1 lists the external signals for booting mode and describes each of functions.

Table 3-2 Signals for boot mode

Pin Functional Name	*Pin Name (refer to datasheet for pin numbers)*	
CFG[0]	#20_GP0.0	Debugger Mode or Boot Mode
CFG[1]	#21_GP0.1	Boundary Scan or SWD logic selection
CFG[2]	#27_GP0.2	Serial Flash Boot or Nand Flash Boot
CFG[3]	#29_GP0.4	
CFG[4]	#30_GP0.5	

3.4.1 Debugger Mode

If CFG[0]=0, then *adstar-L* boots as Debugger mode. In this mode, CPU's execution is stopped, and user can control the CPU's program execution via Serial Wire Debugger.

3.4.2 Boot Mode

If CFG[0]=1, then *adstar-L* boots as boot mode. In this mode, CPU executes a program normally. Booting memory is set by CFG[4:2]

3.4.3 Serial Flash Boot

If CFG[4:2]=111, then *adstar-L* boots with Serial Flash.

3.4.4 NAND Flash Boot

If CFG[4:2] is neither 111 nor 110, then *adstar-L* boots with NAND Flash. With this mode, initially, the boot codes are copied into 2KB internal SRAM memory, and then CPU executes the copied instructions.

CFG[4:2]	*NAND Boot Mode*	*NAND Flash Type*
000	Small type 3-Cycle	NAND Flash Small type Address 3 cycles
001	Small type 4-Cycle	NAND Flash Small type Address 4 cycles
010	Large type 4-Cycle	NAND Flash Large type Address 4 cycles
011	Large type 5-Cycle	NAND Flash Large type Address 5 cycles
100	MLC 4-Bit ECC	NAND Flash MLC type 4-bit ECC
101	MLC 24-Bit ECC	NAND Flash MLC type 24-bit ECC

3.4.5 SWD Selection

JTAG, SWD pins are selected by CFG[1] pin without PinMux.
If CFG[1] = 0, PinMux configuration set to Boundary Scan
If CFG[1] = 1, PinMux configuration set to SWD.

4 SYSTEM CONTROL

System control includes reset control, clock control, power control, and low-power modes.

4.1 Reset Control

Reset controller consists of External Reset, Power on Reset, Debugger Reset and Watchdog Reset. A following figure 4-1 shows the entire Reset signals.

The RESET# pin responds to an external reset signal (active LOW). When the device is out of reset, the device will start executing. When out of reset, the boot mode will be determined and the device will start executing its boot mode.

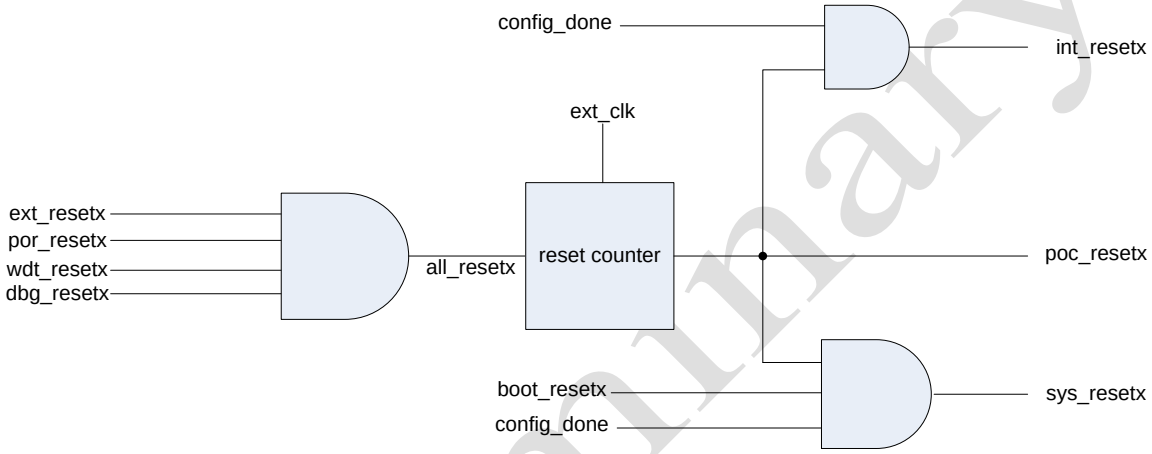


Figure 4-1 Reset

The debugger reset on system is realized by writing to SWD internal register.

4.1.1 System Reset

The System Reset is occurred at the following categories.

1. External Reset
2. Debugger Reset
3. Watchdog Reset
4. POR Reset

4.1.2 Power On Start Time

If VDD33 is assigned to 3.3V supply and Internal LDO assigns 1.8V supply to VDD, output POR will be released.
While POR is released, if External Reset occurs, Startup circuit starts operation using External Clock.
This Startup circuit prevent malfunction before the stabilization Xin, in the same time system reset of internal logic is released.
System reset is released when the POR Reset, External Reset are released and after 1024-cycle using Xin clock.

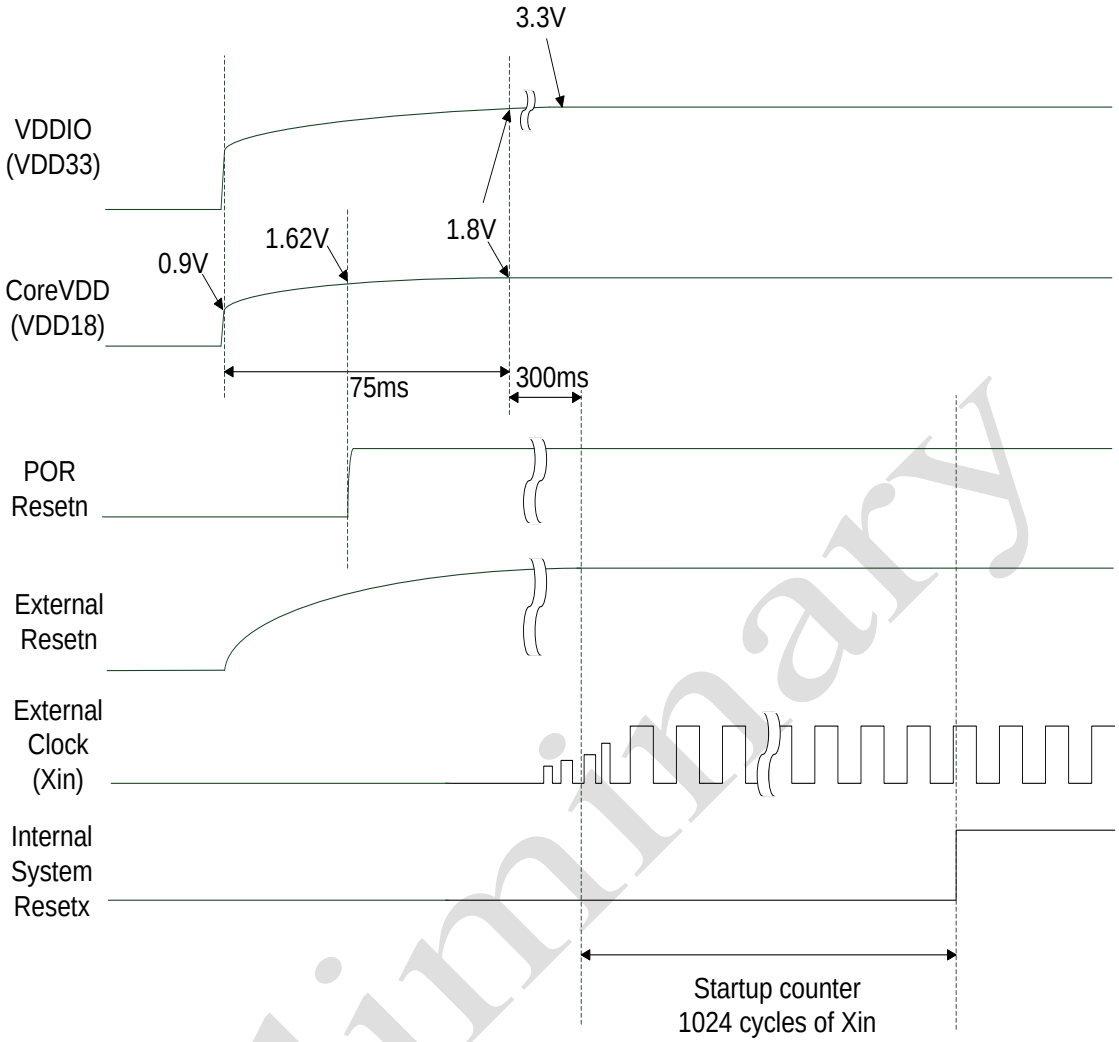


Figure 4-2 Power On Start Time Diagram

4.2 Clock control

The device has two on-chip PLLs and two on-chip oscillators.

The device is designed to operate with three clock sources. The first input clock is generated by main oscillator, the second clock input for the LCD module and others is optional GP6.2(DOTCLK_I) input from either external oscillator or divided clock of main oscillator, and the third clock input is generated by a RTC oscillator clock (32.768KHz) for the RTC module

There are two PLLs in this device. Each PLL is controlled by PLLCONx registers. Each PLL operates in the same manner.
The reference clock for PLL0 comes from the Xin input pin. The reference clocks for the PLL1 come from the external XIN input pin, external DOTCLK_I input pin and internal clk16_0 input.

All PLLs are powered down after reset

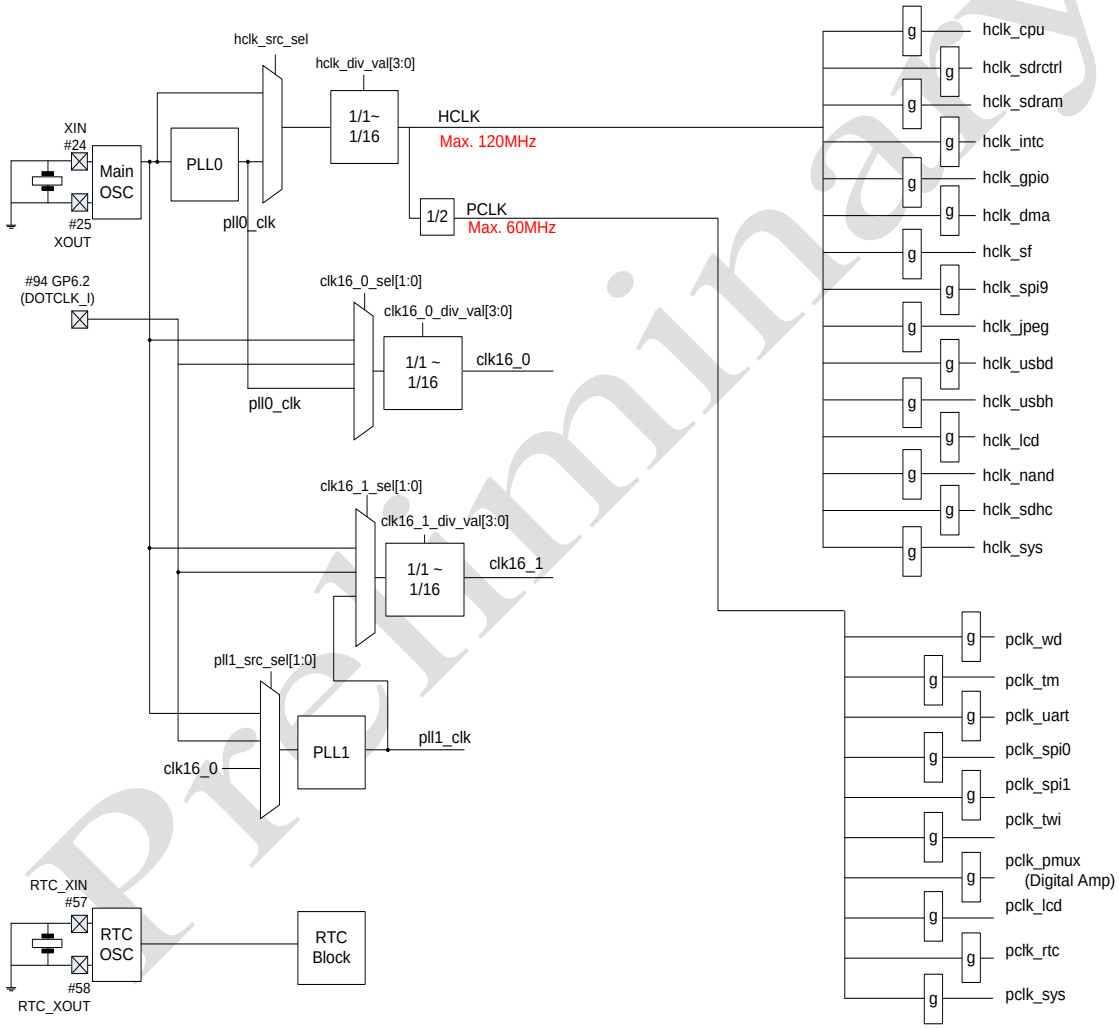


Figure 4-3 Clock Scheme

In most cases, the PLL may be selected for higher performance requirements but requires increased power consumption.
For lower performance and reduced power consumption, the crystal clock could be selected.

The main crystal clock and the PLL0 are used as reference clock sources to drive HCLK and PCLK for peripherals.

HCLK and PCLK clocks supply to AHB and APB, respectively. The two clocks have same phase and 2:1 frequency ratio.

The maximum frequency of HCLK is 120MHz and that of PCLK is 60MHz.

The HCLK domain is used to drive the cpu and AHB peripherals. The PCLK domain is used to drive the APB peripherals. The reference for HCLK and PCLK can be either main crystal clock or PLL0 clock output.

The PCLK is actually a branch of the HCLK domain. So, PCLK runs synchronous to HCLK. All of the APB peripherals on the PCLK branch are considered to be on the HCLK domain.

4.2.1 Main oscillator

The main oscillator can be used as the clock source for the PLL0 and PLL1.

The main oscillator operates at frequencies from 32 KHz to 27MHz.
When using internal PLLs, the crystal should be a frequency range from 60KHz to2.25MHz.

When the main oscillator is used to generate the clock, external crystal is required to be connected across the XIN and XOUT pins, along with two load capacitors, as shown in Figure 4-4.

The majority of internal modules are operated with clock source generated by main oscillator.

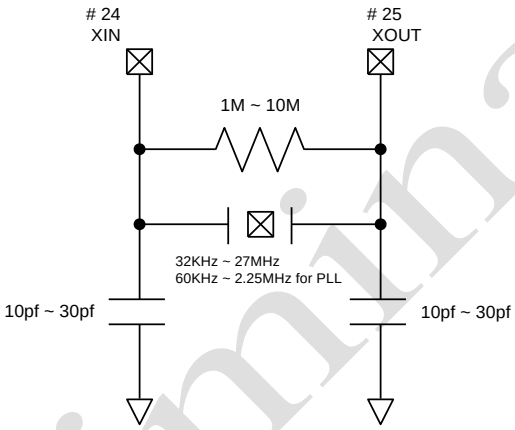


Figure 4-4 Main Oscillator Circuit

4.2.2 RTC oscillator (32KHz)

The RTC oscillator can be used as the clock source for the RTC block. The RTC oscillator remains enabled in all power modes except Static mode.
The oscillator requires the external crystal circuit to generate the RTC clock, as shown in Figure 4-5.

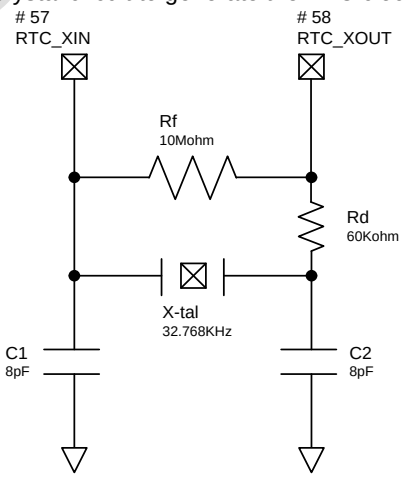


Figure 4-5 32.768-KHz Oscillator Circuit

4.2.3 PLL0

The PLL0 can take Main oscillator as reference clock.
The PLL0 accepts an input clock frequency in the range of 60 KHz to 2.25 MHz.

The PLL0 is enabled by software only. The program must be configured to activate the PLL0. wait for the PLL0 to be lock, and then connect to the PLL0 as a clock source.

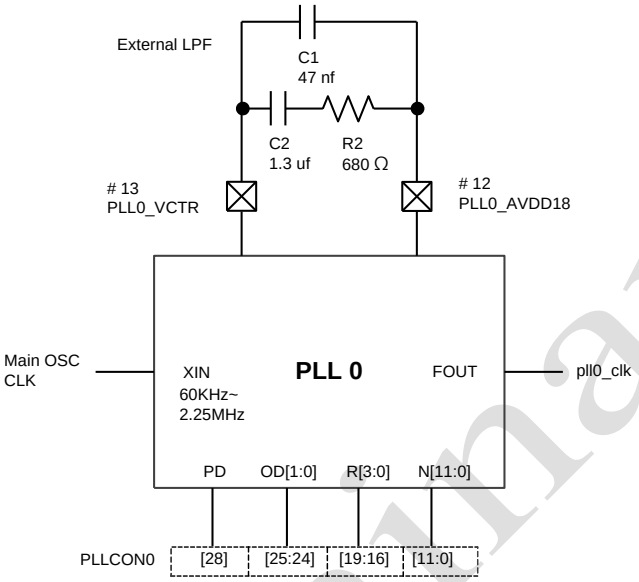


Figure 4-6 PLL0 with External Filter

Before the PLL0 is enabled it must be set up correctly. The main OSC clock is a source for the PLL0 reference clock.

PLL output frequency is calculated from the following the equation:

$$\text{Fout} = \frac{XIN \times \frac{N}{R}}{OD}$$

In actual application, correct setting should meet

$$50M \le XIN \times \frac{N}{R} \le 200M, R \ge 2, N \ge 2;$$

Where R is the input divider ratio, it can be adjusted by R[3:0] as below:

R[3:0]	***Input Divider Ratio (R)***
0010	2
0011	3
…	…
1101	13
1110	14
1111	15

N represents the feedback divider ratio of loop(multiplier), which can be adjusted by N[11:0] as follows:

N[11:0]	***Feedback Divider Ratio (N)***
0000,0000,0010	2
0000,0000,0011	3
…	…
1111,1111,1101	4093
1111,1111,1110	4094
1111,1111,1111	4095

OD is the output divider, which can be adjusted by OD[1:0] as follows:

OD[1:0]	*Output Divider Ratio (OD)*
00	Normal operation
10	divide by 2
01	divide by 4
11	divide by 8

As an example, if the XIN is 1MHz, the R[3:0] is 1000, the N[11:0] is 010000000000, the OD[1:0] is 11 then

$$\text{Fout} = \frac{1 \times \frac{1024}{8}}{8} = 16\,MHz$$

After setting up the PLL0, the PLL0 is enabled by writing a zero to the PLL Power down(PD) bit in the PLLCON0 register.

4.2.4 PLL1

The PLL1 accepts an input clock frequency in the range of 60 KHz to 2.25 MHz.
The PLL1 is disabled and powered off on reset.

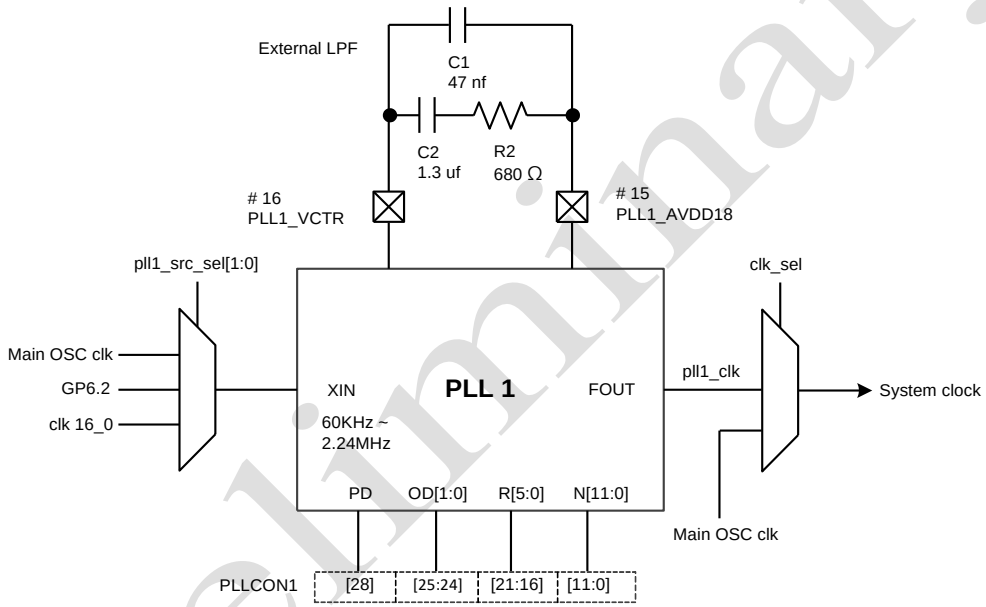


Figure 4-7 PLL1 with External Filter

The PLL1 source select field(pll1_src_sel) selects a source for the reference clock.
See the PLL0 Section for details about the calculation for the output frequency.

4.2.5 PLLx Clock Change

During System operation, System PLL Clock Frequency can be changed using two approaches, either a PLL Clock Source selection or a PLL Clock Frequency Configuration.
The system may became unstable or hang, if the PLL Clock Frequency is changed, While the System is operating
To avoid the unstable condition, External Clock must be connected to System clock before Changing PLL Clock

When PLL Clock change is completed, settling delay (Lock time) is implemented to allow the changed PLL clock Frequency to settle. The delay takes affect for Max. 2ms.
After the delay, The System Clock will be disconnected from external Clock and connected to Changed PLL Clock simultaneously.

To keep the system stable, the switching from external clock to PLL Clock is implemented by Glitch Free Mux in order to avoid Glitch.

4.2.6 Clock gating

The clock to each peripheral can be individually gated on and off using bits of the HCLKEN and PCLKEN registers of the system controller. These bits are cleared after any reset.
Before turning off the clock, make user that the peripheral is not running.

The software can gate off the interface clock of each peripheral, when it is not needed.

Any bus access to a peripheral that has its clock disabled generates an error termination.

4.2.7 Additional Clock Divider

Each divider has the capability to divide an input reference frequency by a fixed integer value or fractional value. The reference clock frequency must be selected to achieve the desired output frequency.

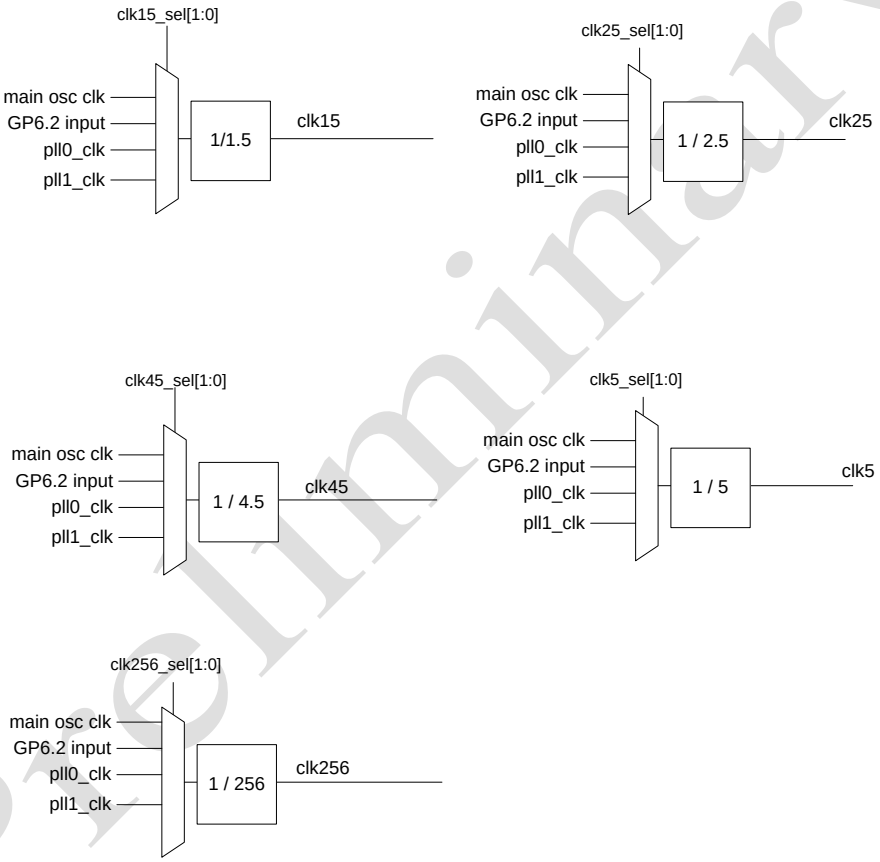


Figure 4-8 Additional Clock Divider

4.2.8 USB Clock

USB Host/Device is clocked from two clock source as shown in the following Figure 4-9.

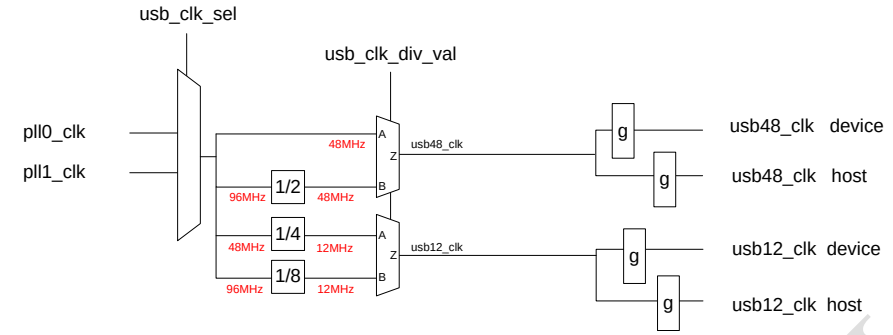


Figure 4-9 USB Clock

As shown in the Figure 4-9, there are two possible sources for USB clock, one clock from each of the two PLLs. The usb48_clk frequency must be 48MHz and the usb12_clk frequency must be 12MHz to guarantee operation.

4.2.9 TFT LCD Clock

The LCD controller uses three primary clocks: hclk_lcd, pclk_lcd, and the DOTCLK. The hclk_lcd and DOTCLK is asynchronous.

The LCD module can be clocked as shown in the following Figure 4-10.

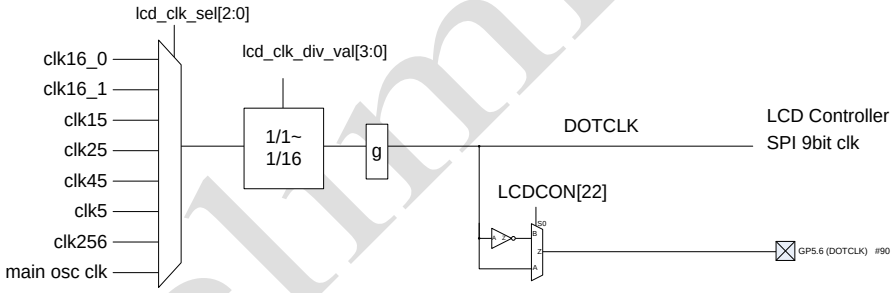


Figure 4-10 TFT LCD Clock

As shown in the Figure 4-10, there are eight possible sources for DOTCLK. The selected clock can be further divided by any ratio from 1 to 1/16 before going to the LCD module.
The DOTCLK is also output signals.

4.2.10 Sound Mixer Clock

The Sound Mixer module can be clocked as shown in the following Figure 4-11.

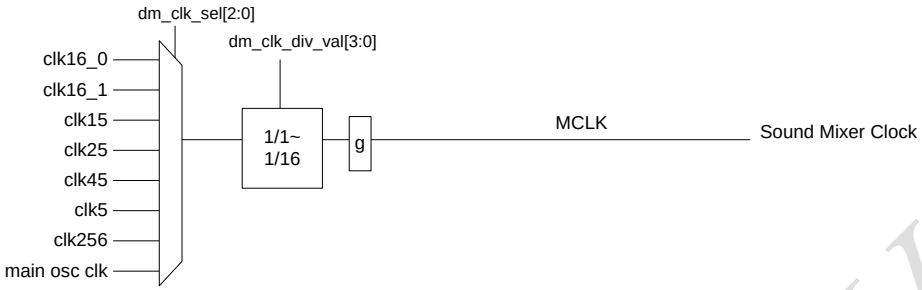


Figure 4-11 Sound Mixer Clock

As shown in the Figure 4-11, there are eight possible sources for MCLK. The selected clock can be further divided by any ratio from 1 to 1/16 before going to the Sound Mixer module.

4.2.11 Protection Mechanism

The adStar-L requires a two-step procedure for write accesses to the system control registers.

The GLOCK register is required to prevent accidental writes to the critical registers in system control module. The user must write the correct value(0xe5511acc) into the GLOCK register. This will unlock all the registers in the module.

To write the respective registers is also needed to enables its respective write enable bits of the WREN register.

4.3 Power modes

The Power Management Controller provides multiple power options to allow the user to optimize power consumption for the user applications needed.

Power modes are selected by the halt instruction, which takes the mode index number as argument.

Modes	*CPU Clock*	*Main OSC*	*Main domain Power*	*RTC OSC*	*RTC domain power*	*Exit*
Sleep(Halt3)	Off	On	On	On	On	RESET#, Interrupt Source
Stop(Halt2)	Off	Off	On	On	On	RESET# Event Source, Wake-up
Shutdown(Halt1)	Off	Off	Off	On	On	RTC Alarm Wake-up Reboot from Power-up
Static(Halt0)	Off	Off	Off	Off	On	Wake-up Reboot from Power-up

4.3.1 RUN mode

This is the normal operating mode for the chip. This mode is entered after any reset.
In RUN mode, all clocks are active, allowing software execution and peripheral operation.

To reduce power in this mode, disable the clocks to unused peripherals using their corresponding clock gating control bits in the clock enable registers (AHBCLKEN, APBCLKEN).

4.3.2 Sleep mode

The Halt3 instruction will halt the CPU and SPM memorys.
The CPU is stopped, the rest of the chip is operating.

any interrupts can be used as wake-up source in sleep mode.

The interrupts must be active high level to be used as wake-up source.

- CPU is disabled.
- SPM is disabled.

Wake-up from Sleep mode(Halt3)

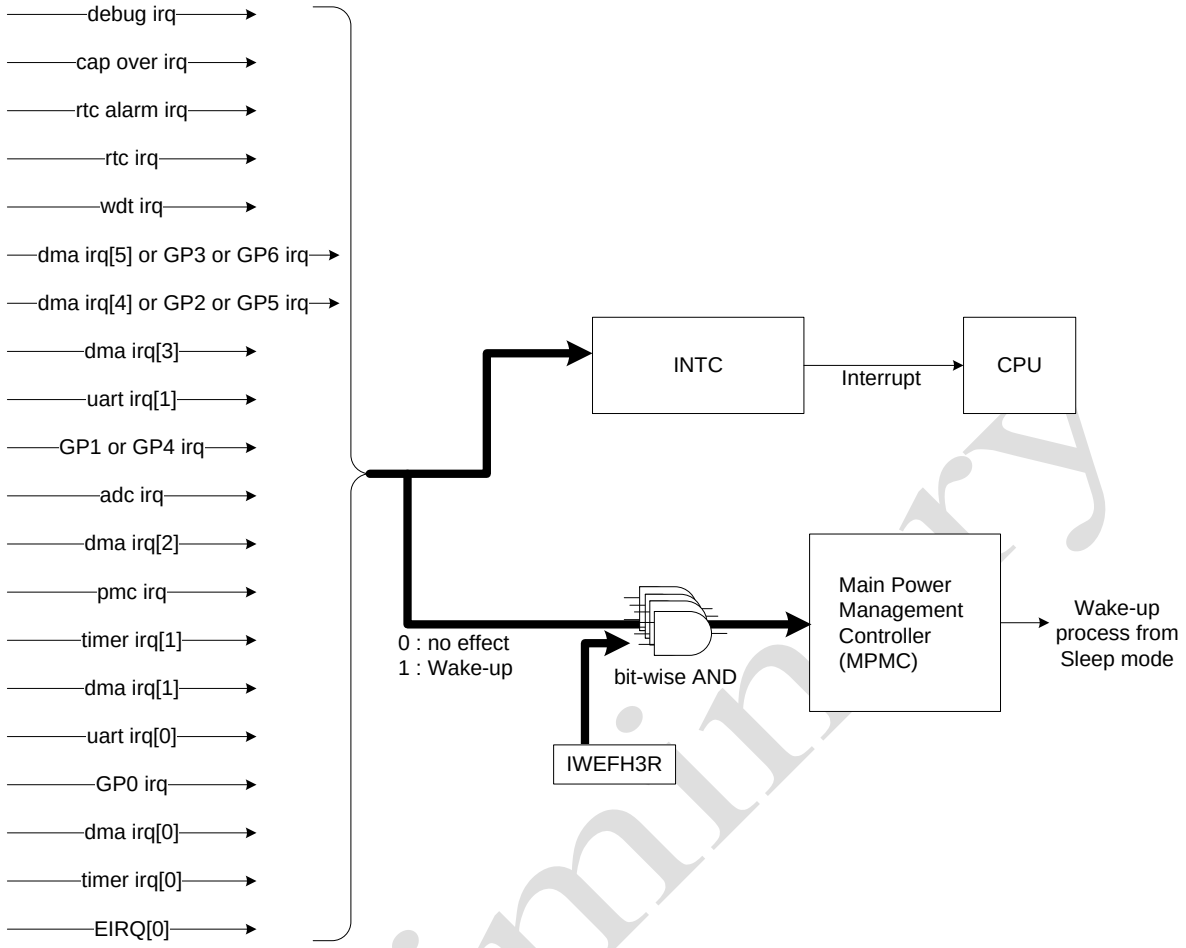


Figure 4-12 Wake-up process from Sleep mode

4.3.3 Stop mode

In Stop mode, all clocks are stopped except RTC oscillator and RTC block.
Wake-up sources are RTC interrupt signals or generated by external input pin.

- The PLLs are disabled
- The Main OSC is disabled
- RAM is retention

Wake-up from Stop mode(Halt2)

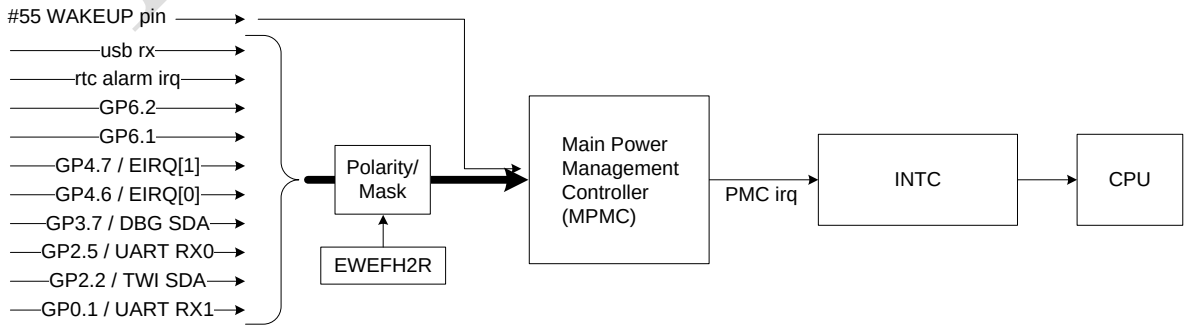


Figure 4-13 Wake-up process from Stop mode

4.3.4 Shutdown mode

Power of the main power domain is removed, to reduce current leakage.
Only a small amount of logic, including RTC oscillator and RTC Block remain powered.

The Shutdown mode is available only when the external voltage regulator is used with Power down and the RTC block is kept powered by VBAT.

When the device enters Shutdown mode, the external regulator is turned off.

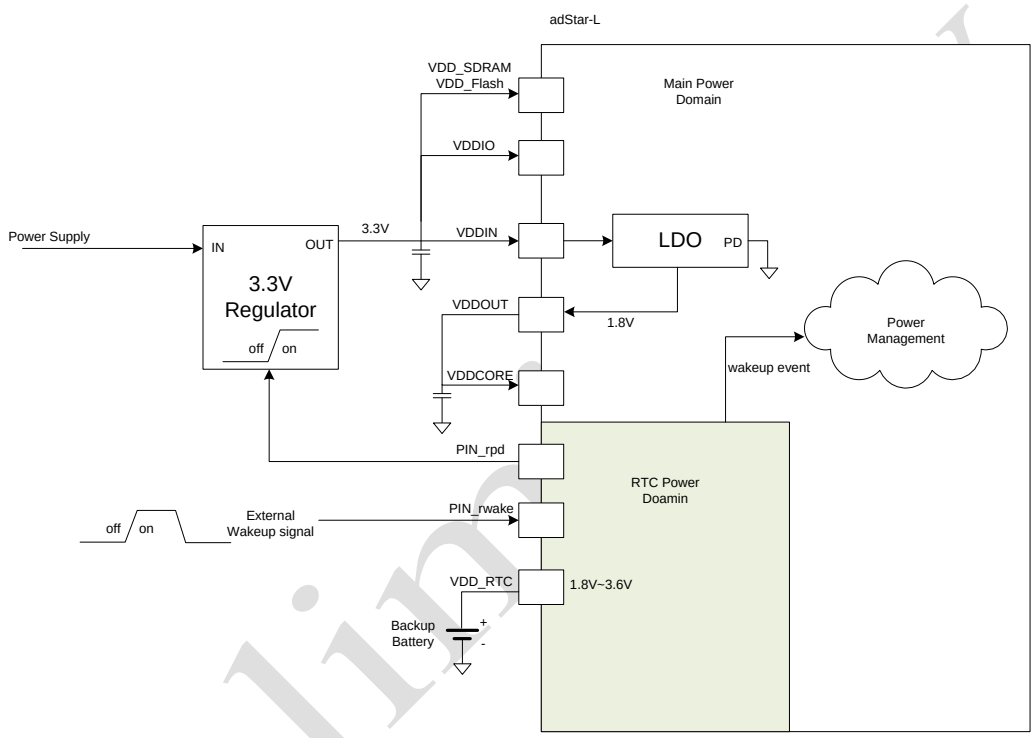


Figure 4-14 Power Off for Shutdown/Static mode

Wake-up sources are RTC interrupts, generated by external wake-up pin.

Wake-up from Shutdown mode(Halt1)

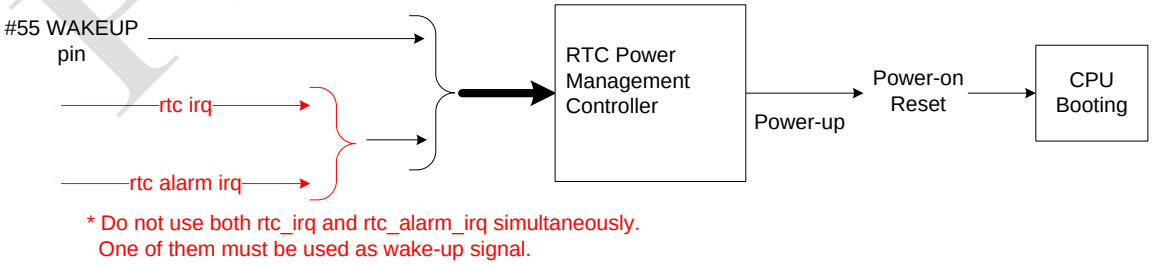


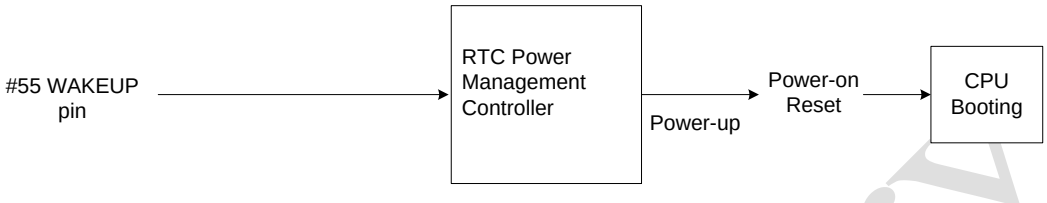
Figure 4-15 Wake-up process from Standby mode

4.3.5 Static mode

All clocks, including RTC oscillator and RTC block are stopped.
Wake-up sources are RTC interrupts, generated by external wake-up pin

- RTC OSC is disabled.

Wake-up from Static mode (Halt0)



* Both rtc_irq and rtc_alarm_irq should be de-active when using "Halt0"

Figure 4-16 Wake-up process from Static mode

4.4 System Control Registers

Try to be set the corresponding bit for the system register access.

4.4.1 System Control Global Lock Register (GLOCK)

Address : 0x8002_3C00

Bit	*R/W*	*Description*	*Default Value*
31:0	W	If user write 0xe5511acc system control will be unlock. Unlock state be allowed to write the other register When user write another value, it became lock state. Read operation shows the lock status 0 : lock 1 : unlock	0
	R		

4.4.2 System Control Write Enable Register (WREN)

Address : 0x8002_3C04

Bit	R/W	Description	Default Value
31:20	R	Reserved	-
19	R/W	DM Clock Divider register	0
18	R/W	LCD Clock Divider register	0
17	R/W	CLK16_1 Divider register	0
16	R/W	CLK16_0 Divider register	0
15	R/W	HCLK Divider register	0
14	R	Reserved	-
13	R/W	USB PHY Control Register Write Enable	0
12	R/W	PCLK Control Register Write Enable	0
11	R/W	HCLK Control Register Write Enable	0
10	R/W	Sound Clock Control Register Write Enable	0
9	R/W	PLL Control Register Write Enable	0
8	R/W	Clock Control Register Write Enable	0
7:4	R	Reserved	-
3	R/W	Reserved	-
2	R/W	Interrupt Wakeup Enable register	0
1	R/W	Reserved	-
0	R/W	halt register enable 1 - Disable write protection for the corresponding register. 0 - Enables write protection for the corresponding register	0

* To write freely to this register, unlock the global lock bit of the GLOCK register.

* If you turn off the Core Clock by Halt 3 command, you should be set bit[3] high.

* To wake up the core from a sleep mode, interrupt should be generated.

4.4.3 Halt Register

Address : 0x8002_3C08

Bit	R/W	Description	Default Value
31:5	R	Reserved	-
4:0	W	10 : halt0 11 : halt1 12 : halt2 13 : halt3 (cpu, spm clock off) One pulse signal of PCLK. Write data is not maintained.	0

* To write freely to this register, enable the corresponding write enable bit of the WREN register.

4.4.4 Halt Status Register

Address : 0x8002_3C0C

Bit	R/W	Description	Default Value
31:11	R	Reserved	-
10	R	PMC IRQ It canbe seen an interrupt has occured or not user can be confirm the PMU Status reg[0] either.	0
9	R	RTC wakeup event latch. It shows waking from Halt0 or Halt1.	0
8	R/W	Cpu only clock disable during halt3 0 : cpu, spm clock off when halt3 excuting 1 : cpu only clock off	0
7:5	R	Reserved.	-
4:0	R	12 : halt2 13 : halt3 It show which halt mode was performed. Halt0 and halt1 status is unknown. Because Main power was shut down and they are all cleared	0

* To write freely to this register, enable the corresponding write enable bit of the WREN register.

4.4.5 Interrupt Wake up Enable Register

Address : 0x8002_3C10

Bit	R/W	Description	Default Value
		Halt 3 mode only. Choose the interrupt type when the wakeup Choose the IRQ. It is used wake up the interrupt. As same as the IRQ reg order. (Debug irq is included) PMC irq is included RTC irq is included RTC wakeup irq is included Only activated interrupt revive the CPU's HCLK. Interrupt processing is irrelevant. Only revive the CPU clock. Assigned interrupt process ISR after Halt3, interrupt controller set appropriately. This register just only wake up CPU clock. This it unrelated ISR.	-
31	R/W	SWD Interrupt Use edge method Clock_ctrl_r[0]	0
30	R/W	MJPEG 1 Interrupt	0
29	R/W	Capture Over Interrupt	0
28	R/W	SPI_LCD Interrupt	0
27	R/W	RTC Alarm Interrupt	0
26	R/W	RTC Interrupt	0
25	R/W	TWI Interrupt	0
24	R/W	NAND Interupt	0
23	R/W	WDT Interrupt	0
22	R/W	DMA CH5 Interrupt , GPIO 3 interrupt, GPIO 6 interrupt	0
21	R/W	SDCard Interrupt	0
20	R/W	DMA CH4 Interrupt , GPIO 2 Interrupt, GPIO 5 Interrupt	0
19	R/W	MJPEG 0 Interrupt	0
18	R/W	SPI Interrupt	0
17	R/W	DMA CH3 Interrupt	0
16	R/W	UART 1 Interrupt	0
15	R/W	GPIO 1 Interrupt, GPIO 4 Interrupt	0
14	R/W	USB host interrupt, Device Interupt	0
13	R/W	ADC Interrupt	0
12	R/W	DMA CH2 Interrupt	0
11	R/W	PMC interrupt	0
10	R/W	Timer 1 Interrupt	0
9	R/W	DMA CH1 Interrupt	0
8	R/W	UART 0 Interrupt	0
7	R/W	GPIO 0 Interrupt	0
6	R/W	DMA CH0 Interrupt	0
5	R/W	LCD Frame sync Interrupt	0
4	R/W	EIRQ1 Interrupt	0
3	R/W	Sound Mixer Interrupt	0
2	R/W	Timer 0 Interrupt	0
1	R/W	Core timer Interrupt	0
0	R/W	EIRQ0 Interrupt (Highest Priority)	0

* To write freely to this register, enable the corresponding write enable bit of the WREN register.
* In the halt3 (sleep mode) mode, this register is used to determine which interrupt is implemented for wake-up

4.4.6 Event Wake up Enable Register

Address : 0x8002_3C14

Bit	R/W	Description	Default Value
31:27	R	Always awake by the RTC wakeup signal. This is not an option	-
26	R/W	SWD interrupt mask 0: mask 1: unmask	0
25	R/W	Usb receive data mask 0: mask 1: unmask	0
24	R/W	Rtc alarm interrupt mask 0: mask 1: unmask	0
23	R/W	Gp6.2 mask 0: mask 1: unmask	0
22	R/W	GP6.1 mask 0: mask 1: unmask	0
21	R/W	GP4.7 mask 0: mask 1: unmask	0
20	R/W	GP4.6 mask 0: mask 1: unmask	0
19	R/W	GP3.7 mask 0: mask 1: unmask	0
18	R/W	GP2.5 mask 0: mask 1: unmask	0
17	R/W	GP2.2 mask 0: mask 1: unmask	0
16	R/W	GP0.1 mask 0: mask 1: unmask	0
15:11	R	Reserved	_
10	R/W	SWD interrupt Polarity 0: active low 1: active high	0
9	R/W	Usb receive data Polarity 0: active low 1: active high	0
8	R/W	Rtc alarm interrupt Polarity 0: active high 1: active low	0
7	R/W	GP6.2 Polarity 0: active low 1: active high	0
6	R/W	GP6.1 Polarity 0: active low 1: active high	0
5	R/W	GP4.7 Polarity 0: active low 1: active high	0
4	R/W	GP4.6 Polarity 0: active low 1: active high	0
3	R/W	GP3.7 Polarity 0: active low 1: active high	0
2	R/W	GP2.5 Polarity 0: active low 1: active high	0
1	R/W	GP2.2 Polarity 0: active low 1: active high	0
0	R/W	GP0.1 Polarity 0: active low 1: active high	0

* To write freely to this register, enable the corresponding write enable bit of the WREN register.
* In the halt2 (stop mode) mode and halt1(shutdown mode), this register is used to determine which interrupt is implemented for wake-up

* This signal is integrated PCM_IRQ.
PMC ISR routine is executed.

User can check through this register which register occurred.

When user read this register, it let user know which register occur.
Every event will be ignored while entering into halt2 state. The event occurs after entering the mode completely and it awakes up.

4.4.7 PMC Status Register

Address : 0x8002_3C18

Bit	R/W	Description	Default Value
31:2	R	Reserved.	-
1	R/W	RTC s/w reset 0 : release reset(normal operation state) 1 : reset asserted	0
0	R/W	PMC IRQ clear bit Read this register makes you know IRQ occurence. When user write 1 it cleared. then it turns 0 automatically PMC IRQ occured at halt0, halt1,halt2. This is not occured at halt3 At halt3 wake is considered one block of irq.	0

4.4.8 OSC Stable Counter Register

Address : 0x8002_3C1C

Bit	R/W	Description	Default Value
31:11	R	Reserved.	-
10 : 0	R/W	The value of the osc stable counter be used for Wake	11'h7ff

* To write freely to this register, enable the corresponding write enable bit of the WREN register.

4.4.9 Clock Control Register (CLKCON)

Address : 0x8002_3C20

Bit	R/W	Description	Default Value
31:24	R	Reserved.	-
23:20	R/W	ADC Clock divider 0000: System Clock 0001: System Clock / 2 0010: System Clock / 3 0011: System Clock / 4 … 1110: System Clock / 15 1111: System Clock / 16	0
12:8	R/W	PLL Lock Counter value for halt2	5'h1f
7:4	R	Reserved.	-
5 : 4	R/W	PLL1 clock source select. These bits select the PLL1 clock source. 00:xin clock selected 01:GPIO clock selected 1x:clk16_0 clock selected	
3	R/W	USB Clock Enable 0: USB clock is off 1: USB clock is on	0
2	R/W	USB Clock divider. USB requires 48MHz clock. 0: USB Source Clock (when source clock is 48MHz) 1: USB Source Clock / 2 (when source clock is 96MHz)	0
1	R/W	USB Source Clock Select. 0: pll0_clk selected 1: pll1_clk selected	0
0	R/W	Select clock source for HCLK domain 0: XIN input selected 1: PLL0 clock selected	0

* To write freely to this register, enable the corresponding write enable bit of the WREN register and unlock the GLOCK register.

4.4.10 PLL0 Control Register (PLLCON0)

Address : 0x8002_3C24

Bit	R/W	Description	Default Value
31 : 29		Reserved	-
28	R/W	PLL Power Down 0 : normal operation 1 : power down	1
27 : 26	R	Reserved	-
25 : 24	R/W	OD (Output divider). These bits set the output divider value for the PLL0. 00 : divide by 1 01 : divide by 4 10 : divide by 2 11 : divide by 8	0
23 : 20	R	Reserved	-
19 : 16	R/W	R (Input divider). These bits set the input divider value for the PLL0. R must be >=2 or unpredictable operation results.	02h
15 : 12	R	Reserved	-
11 : 0	R/W	N (Multiplier). These bits set the multiplier value for the PLL0. N must be >=2 or unpredictable operation results.	002h

* To write freely to this register, enable the corresponding write enable bit of the WREN register and unlock the GLOCK register.
* FOUT = (XIN*N)/(R*OD)

4.4.11 Clock Divider Control Register (CLKDCON)

Address : 0x8002_3C28

Bit	R/W	Description	Default Value
31:28	R	Reserved	-
27:25	R/W	DM clock source select. 000: clk16_0 001: clk16_1 010: clk15 011: clk25 100: clk45 101: clk5 110: clk256 111: XIN	000
24:22	R/W	LCD clock source select. 000: clk16_0 001: clk16_1 010: clk15 011: clk25 100: clk45 101: clk5 110: clk256 111: XIN	000
21:20	R/W	CLK16_1 clock source select. 00 : XIN 01 : GP6.2 10 : PLL1	0
19:18	R/W	CLK16_0 clock source select. 00 : XIN 01 : GP6.2 10 : PLL0	0
17:16	R/W	CLK256 clock source select. 00 : xin 01: GP6.2 10: pll0 11: pll1	0
15:14	R/W	CLK5 clock source select. 00 : xin 01: GP6.2 10: pll0 11: pll1	0
13:12	R/W	CLK45 clock source select. 00 : xin 01: GP6.2 10: pll0 11: pll1	01
11:10	R/W	CLK25 clock source select. 00 : xin 01: GP6.2 10: pll0 11: pll1	0
9:8	R/W	CLK15 clock source select. 00 : xin 01: GP6.2 10: pll0 11: pll1	00
7:0	R	Reserved	-

* To write freely to this register, enable the corresponding write enable bit of the WREN register and unlock the GLOCK register.

4.4.12 AHB Clock Enable Register (HCLKEN)

Address : 0x8002_3C2C

Bit	R/W	Description	Default Value
31	R/W	bus clock enable	1
30:16	R	Reserved.	-
15	R/W	SD Card IO clock enable	1
14	R/W	NAND clock enable	1
13	R/W	CRTC clock enable	1
12	R/W	USB Host Clock Enable (12MHz, 48MHz, bus clock)	1
11	R/W	USB Device Clock Enable (12MHz, 48MHz, bus clock)	1
10	R	Reserved.	-
9	R	Reserved.	-
8	R/W	H/W JPEG AHB Clock Enable	1
7	R/W	SPI LCD Clock Enable	1
6	R/W	Flash Controller Clock Enable	1
5	R/W	DMA Clock Enable	1
4	R/W	GPIO Clock Enable	1
3	R/W	Interrupt Controller Clock Enable	1
2	R/W	SDRAM Clock Enable	1
1	R/W	SDRAM Controller Clock Enable	1
0	R	Reserved.	1

* To write freely to this register, enable the corresponding write enable bit of the WREN register and unlock the GLOCK register.

4.4.13 APB Clock Enable Register (PCLKEN)

Address : 0x8002_3C30

Bit	R/W	Description	Default Value
31	R/W	Bus clock Enable PMU block signal. Power management is not available without this	1

		clock.(Halt3)	
30:16	R	Reserved.	-
14	R/W	RTC interface clock enable	1
13	R/W	CRTC clock enable	1
12	R/W	Pin MUX Clock Enable	1
11	R/W	ADC APB Clock Enable	1
10	R	Reserved.	-
9	R	Reserved.	-
8	R/W	Sound Mixer APB Clock Enable	1
7	R/W	TWI Clock Enable	1
6	R/W	Reserved.	1
5	R/W	SPI Clock Enable	1
4	R/W	UART Clock Enable	1
3	R/W	Timer Clock Enable	1
2	R/W	Watch Dog Timer Clock Enable	1
1	R	Reserved.	-
0	R	Reserved.	-

* To write freely to this register, enable the corresponding write enable bit of the WREN register and unlock the GLOCK register.

4.4.14 USB PHY Control Register (USBPHYCON)

Address : 0x8002_3C34

Bit	R/W	Description	Default Value
31:18	R	Reserved	-
17	R	Reserved.	1
16	R	Reserved	0
15: 9	R	Reserved	-
8	R/W	USB Function Select bit 0: USB Device 1: USB Host	0
7	R	USB PHY suspend bit 0: No effect 1: Suspend	0
6	R/W	D- Pull-down Enable bit 0: Pull-down Disable 1: Pull-down Enable	0
5	R/W	D+ Pull-down Enable bit 0: Pull-down Disable 1: Pull-down Enable	0
4	R/W	Receive Enable bit 0: USB PHY does not receive external signal. 1: USB PHY receives external signal	0
3	R/W	D- Weak Pull-up Enable bit 0: Pull-up Disable 1: Pull-up Enable	0
2	R/W	D- Pull-up Enable bit 0: Pull-up Disable 1: Pull-up Enable	0
1	R/W	D+ Weak Pull-up Enable bit 0: Pull-up Disable 1: Pull-up Enable	0
0	R/W	D+ Pull-up Enable bit 0: Pull-up Disable 1: Pull-up Enable	0

* To write freely to this register, enable the corresponding write enable bit of the WREN register and unlock the GLOCK register.

4.4.15 Boot mode status register(BMST)

Address : 0x8002_3C38

Bit	R/W	Description	Default Value
31:1	R	Reserved	-
0	R	Boot mode 0: normal mode or debug mode.. etc 1: nandboot mode	1

* To write freely to this register, enable the corresponding write enable bit of the WREN register and unlock the GLOCK register.

4.4.16 HCLK clock divide register(HCLKDIV)

Address : 0x8002_3C3C

Bit	R/W	Description	Default Value
31:5	R	Reserved	-
4	R/W	Synchronization bit When user set 1 it tunes the sync, and you must set 0 again.	0
3:0	R/W	AHB Clock Select 0000: Source Clock 0001: Source Clock / 2 0010: Source Clock / 3 0011: Source Clock / 4 … 1110: Source Clock / 15 1111: Source Clock / 16	0

* To write freely to this register, enable the corresponding write enable bit of the WREN register and unlock the GLOCK register.

4.4.17 CLK16_0 clock divide register(CLK16DIV0)

Address : 0x8002_3C40

Bit	R/W	Description	Default Value
31:5	R	Reserved	-
4	R/W	Synchronization bit When user set 1 it tunes the sync, and you must set 0 again.	0
3:0	R/W	CLK16_0 Clock Select 0000: Source Clock 0001: Source Clock / 2 0010: Source Clock / 3 0011: Source Clock / 4 … 1110: Source Clock / 15 1111: Source Clock / 16	0

* To write freely to this register, enable the corresponding write enable bit of the WREN register and unlock the GLOCK register.

4.4.18 CLK16_1 clock divide register(CLK16DIV1)

Address : 0x8002_3C44

Bit	R/W	Description	Default Value
31:5	R	Reserved	-
4	R/W	Synchronization bit When user set 1 it tunes the sync, and you must set 0 again.	0
3:0	R/W	CLK16_1 Clock Select 0000: Source Clock 0001: Source Clock / 2 0010: Source Clock / 3 0011: Source Clock / 4 … 1110: Source Clock / 15 1111: Source Clock / 16	0

* To write freely to this register, enable the corresponding write enable bit of the WREN register and unlock the GLOCK register.

4.4.19 LCD clock divide register(LCDDIV)

Address : 0x8002_3C48

Bit	R/W	Description	Default Value
31:5	R	Reserved	-
4	R/W	Synchronization bit When user set 1 it tunes the sync, and you must set 0 again.	0
3:0	R/W	LCD Clock Select 0000: Source Clock 0001: Source Clock / 2 0010: Source Clock / 3 0011: Source Clock / 4 … 1110: Source Clock / 15 1111: Source Clock / 16	0

* To write freely to this register, enable the corresponding write enable bit of the WREN register and unlock the GLOCK register.

4.4.20 Sound Mixer clock divide register(SMDIV)

Address : 0x8002_3C4C

Bit	R/W	Description	Default Value
31:5	R	Reserved	-
4	R/W	Synchronization bit When user set 1 it tunes the sync, and you must set 0 again.	0
3:0	R/W	DM Clock Select 0000: Source Clock 0001: Source Clock / 2 0010: Source Clock / 3 0011: Source Clock / 4 … 1110: Source Clock / 15 1111: Source Clock / 16	0

* To write freely to this register, enable the corresponding write enable bit of the WREN register and unlock the GLOCK register.

4.4.21 PLL1 Control Register (PLLCON1)

Address : 0x8002_3C50

Bit	*R/W*	*Description*	*Default Value*
31 : 29		Reserved	-
28	R/W	PLL Power Down 0 : normal operation 1 : power down	1
27 : 26	R	Reserved	-
25 : 24	R/W	OD (Output divider). These bits set the output divider value for the PLL1. 00 : divide by 1 01 : divide by 4 10 : divide by 2 11 : divide by 8	0
23 : 20	R	Reserved	-
19 : 16	R/W	R (Input divider). These bits set the input divider value for the PLL1. R must be >=2 or unpredictable operation results.	02h
15 : 12	R	Reserved	-
11 : 0	R/W	N (Multiplier). These bits set the multiplier value for the PLL1. N must be >=2 or unpredictable operation results.	002h

* To write freely to this register, enable the corresponding write enable bit of the WREN register and unlock the GLOCK register.

* FOUT = (XIN*N)/(R*OD)

5 SPI FLASH MEMORY CONTROLLER

5.1 Introduction

Maximum capacity of Flash memory is 16Mbytes and maximum clock frequency is 80MHz. However Flash Memory Controller uses divided AHB Clock frequency. Due to that reason, Flash Memory operates half of the maximum frequency.

The controller has two separate bus interfaces: memory interface and register interface.
The memory interface can be used by the bus master (CPU, DMA) to read from, or write to, any memory location within the SPI flash memory. And it allows code execution (XIP) to be performed directly from the SPI flash.

The register interface provides an interface to configure both the controller and the SPI flash memory and issue any command in the SPI flash command set.

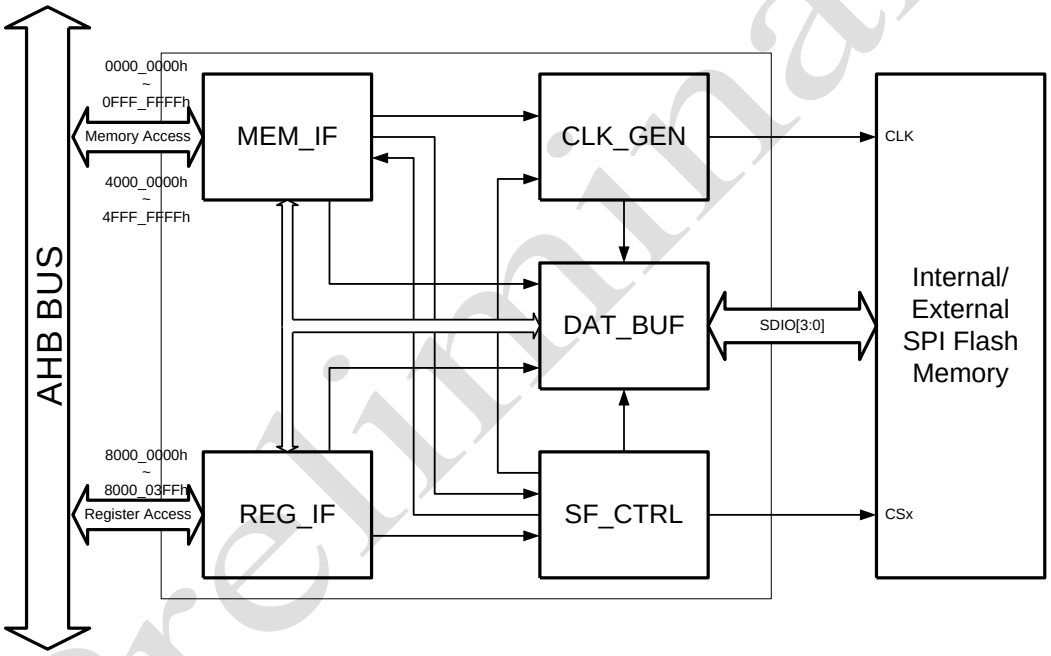


Figure 5-1 Flash Memory Controller Block Diagram

5.2 Feature

The SPI flash controller includes the following features:
- Provides Single, Double, and Quad bit data transfer
- Provides Flash Erase and Flash Program in both H/W and S/W
- Provides XIP (eXecute In Place)

5.3 Functional Description

5.3.1 Register Interface

The flash controller uses the register interface to select the operation modes and configure registers for command/data transfers.

The following operations are serviced through the register interface:
- Flash erase operation

- Flash program operation
- Read/Write status operation.
- Read data operation

5.3.2 Memory Interface

When the address of the read/write access is in the memory interface address range, the user can use XIP mode, reducing command overhead.

Once a read cycle has been started, the controller will automatically poll for the read cycle to complete before allowing any subsequent read accesses to issue. This is achieved by holding any further accesses in wait states.

The following operations are serviced through the memory interface:

- Flash program operation
- Read data operation

5.3.3 Internal Flash Memory

The following features are supported in the internal Flash memory:

- 4M-bit/512K-byte
- 256-byte per programmable page
- Uniform 4KB Sectors, 32KB & 64KB Blocks
- More than 100,000 erase/write cycles
- More than 20-year data retention

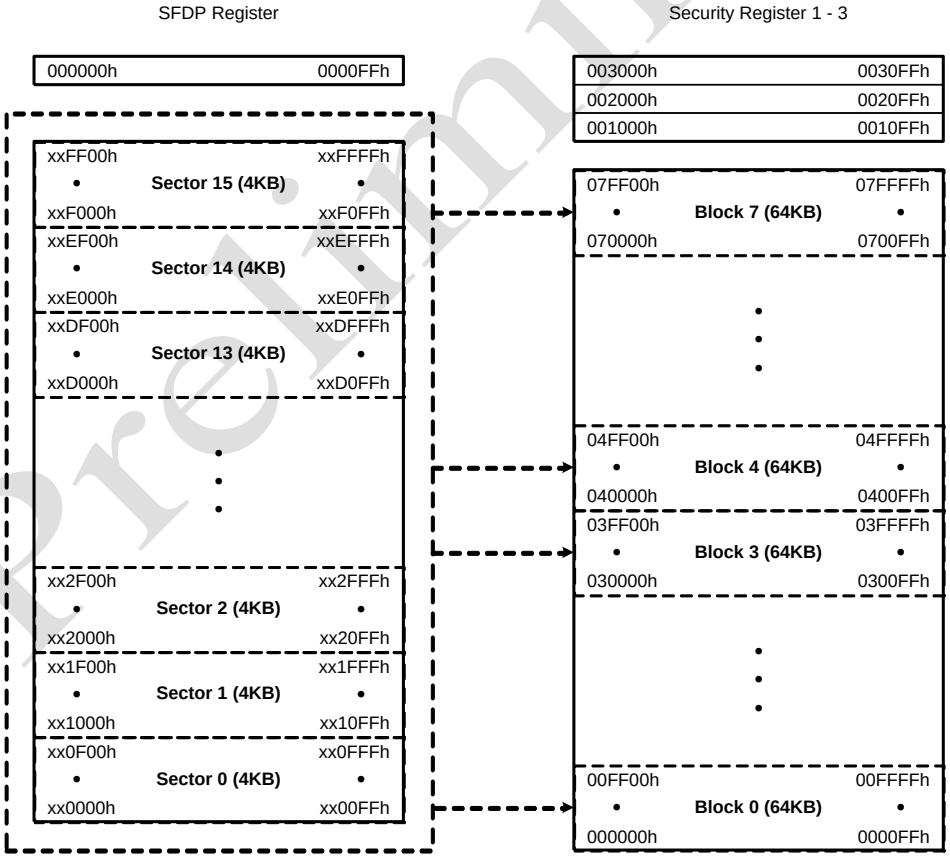


Figure 5-2 Internal Serial Flash Memory

5.3.4 Internal Flash Memory Commands

Table 5-1 Instruction Set Table 1 (Erase, Program Instructions)

Instruction NAME	*BYTE 1 (CODE)*	*BYTE2*	*BYTE3*	*BYTE4*	*BYTE5*	*BYTE6*
Write Enable	***06h***					
Write Enable for Volatile Status Register	***50h***					
Write Disable	***04h***					
Read Status Register-1	***05h***	(S7-S0)				
Read Status Register-2	***35h***	(S15-S8)				
Write Status Register	***01h***	S7-S0	S15-S8			
Page Program	***02h***	A23-A16	A15-A8	A7-A0	D7-D0	
Quad Page Program	***32h***	A23-A16	A15-A8	A7-A0	D7-D0, …	
Sector Erase (4KB)	***20h***	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	***52h***	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	***D8h***	A23-A16	A15-A8	A7-A0		
Chip Erase	***C7/60h***					
Erase / Program Suspend	***75h***					
Erase / Program Resume	***7Ah***					
Power-down	***B9h***					
Continuous Read Mode Reset	***FFh***	FFh				

Table 5-2 Instruction Set Table 2 (Read Instructions)

Instruction NAME	*BYTE 1 (CODE)*	*BYTE2*	*BYTE3*	*BYTE4*	*BYTE5*	*BYTE6*
Release Power Down/ Device ID	***ABh***	dummy	dummy	dummy	(ID7-ID0)	
Manufacturer/ Device ID	***90h***	dummy	dummy	00h	(MF-MF0)	(ID7-ID0)
Manufacturer/Device ID by Dual I/O	***92h***	A23-A8	A7-A0, M[7:0]	(MF[7:0], ID[7:0])		
Manufacturer/Device ID by Quad I/O	***94h***	A23-A0, M[7:0]	xxx,(MF[7:0] ,ID[7:0])	(MF[7:0], ID[7:0], …)		
JEDEC ID	***9Fh***	(MF7-MF0) manufacturer	(D15-ID8) Memory Type	(ID7-ID0) Capacity		
Read Unique ID	***4Bh***	dummy	dummy	dummy	dummy	(ID63-ID0)
Read SFDP Register	***5Ah***	00h	00h	A7-A0	dummy	(D7-D0)
Erase Security Registers	***44h***	A23-A16	A15-A8	A7-A0		
Program Security Registers	***42h***	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0
Read Security Registers	***48h***	A23-A16	A15-A8	A7-A0	dummy	D7-D0

Table 5-3 Instruction Set Table 3 (ID, Security Instructions)

Instruction NAME	*BYTE 1 (CODE)*	*BYTE2*	*BYTE3*	*BYTE4*	*BYTE5*	*BYTE6*
Release Power Down/ Device ID	***ABh***	dummy	dummy	dummy	(ID7-ID0)	
Manufacturer/ Device ID	***90h***	dummy	dummy	00h	(MF-MF0)	(ID7-ID0)
Manufacturer/Device ID by Dual I/O	***92h***	A23-A8	A7-A0, M[7:0]	(MF[7:0], ID[7:0])		
Manufacturer/Device ID by Quad I/O	***94h***	A23-A0, M[7:0]	xxx,(MF[7:0] ,ID[7:0])	(MF[7:0], ID[7:0], …)		
JEDEC ID	***9Fh***	(MF7-MF0) manufacturer	(D15-ID8) Memory Type	(ID7-ID0) Capacity		
Read Unique ID	***4Bh***	dummy	dummy	dummy	dummy	(ID63-ID0)
Read SFDP Register	***5Ah***	00h	00h	A7-A0	dummy	(D7-D0)
Erase Security Registers	***44h***	A23-A16	A15-A8	A7-A0		
Program Security Registers	***42h***	A23-A16	A15-A8	A7-A0	D7-D0	D7-D0
Read Security Registers	***48h***	A23-A16	A15-A8	A7-A0	dummy	D7-D0

5.3.5 Flash Status Register

Flash Status Register (FLSTS)

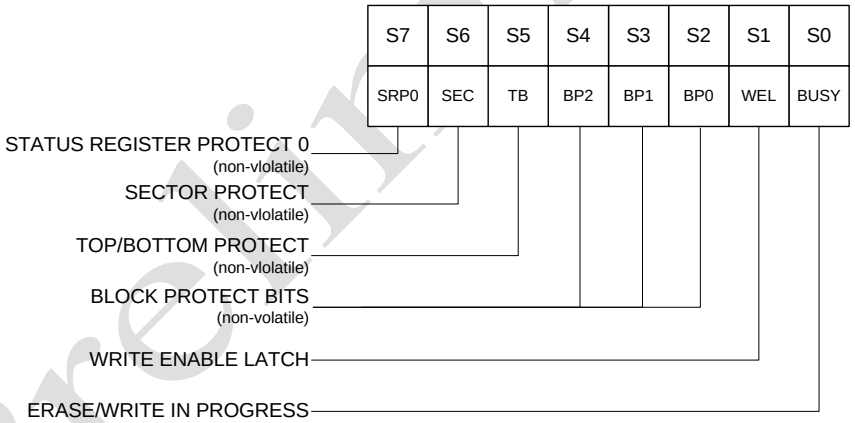


Figure 5-3 Serial Flash Memory Status Register 1

The register access the lowest 1byte of Flash status register.
It is used for checking bit0 (BUSY) that indicates write operation is finished or not.

Flash 2nd Status Register (FLSTS2)

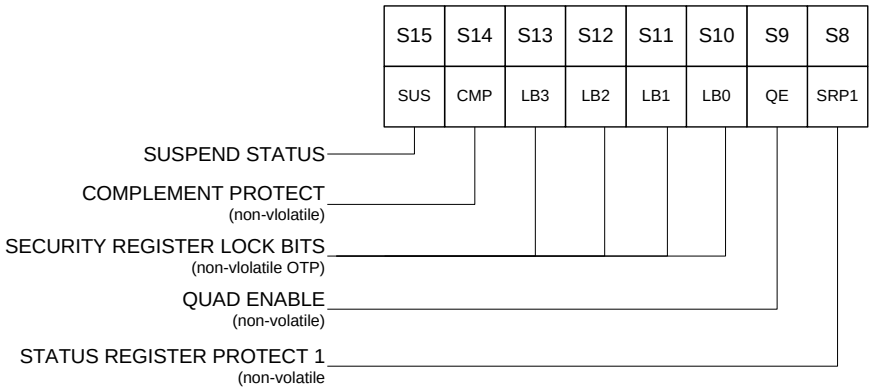


Figure 5-4 Serial Flash Memory Status Register 2

The register access the highest 1byte of Flash status register.
It is used for support Quad mode that can be done by setting bit1 (QE).

Table 5-4 Serial Flash Memory Status Register Description

Bit	*Signal Name*	*Description*
15	SUS	Erase/Program Suspend Status The suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing a Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.
14	CMP	Complement Protect The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 will be reversed. For instance, when CMP=0, a top 4KB sector can be protected while the rest of the array is not; when CMP=1, the top 4KB sector will become unprotected while the rest of the array become read-only, Please refer to the Status Register Memory Protection table for details. The default setting is CMP=0.
13	LB3	Security Register Lock Bits The Security Register Lock Bits (LB3, LB2, LB1, LB0) are non-volatile One Time Program (OTP) bits in Status Register (S13, S12, S11, S10) that provide the write protect control and status to the Security Registers. The default state of LB3-0 is 0, security Registers are unlocked. LB3-0 can be set to 1 individually using the Write Status Register instruction. LB3-0 are One Time Programmable (OTP), once it's set to 1, the corresponding 256-Byte Security Register will become read-only permanently.
12	LB2	
11	LB1	
10	LB0	
9	QE	Quad Enable The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI operation. When the QE bit is set to a 0 state (factory default), the /WP pin and /HOLD are enable. When the QE bit is set to a 1, the Quad IO2 and IO3 pins are enabled.
8	SRP1	Status Register Protect The Status Register Protect bits (SRP1 and SRP0) are non-volatile read/write bits in the status register (S8 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.
7	SRP0	
6	SEC	Sector/Block Protect The non-volatile Sector/Block Protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect either 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The default setting is SEC=0.
5	TB	Top/Bottom Block Protect The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP0, SRp1 and WEL bits.
4	BP2	Block Protect Bits The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tW in AC characteristics).; All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.
3	BP1	
2	BP0	
1	WEL	Write Enable Latch Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following

		instructions: Write Disable, Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Erase Security Register and Program Security Register.
0	BUSY	BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Quad Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register or Erase/Program Security Register instruction. During this time the device will ignore further instructions except for the Read Status Register and Erase/Program Suspend instruction (see TW, tPP, tSE,tBE, and tCE in AC Characteristics). When the program, erase or write status/security register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instruction.

5.3.6 Chip Erasing Flash memory

Using FLCMD register (entire flash memory)
- Write 06h command to the FLCMD register.
- Write C7h/60h command to the FLCMD register.

Using SFDAT register (entire flash memory)
- Set the chip select bit in the SFMOD register to 0x0(chip select low).
- Write 06h command to the SFDAT register.
- Set the chip select bit in the SFMOD register to 0x1(chip select high).
- Set the chip select bit in the SFMOD register to 0x0(chip select low).
- Write C7h/60h command to the SFDAT register.
- Set the chip select bit in the SFMOD register to 0x1(chip select high)
- Poll the busy status bit of the FLSTS register until this operation has completed (Chip Erase complete).

5.3.7 Sector/Block Erasing Flash memory

Using FLSEA register (4KB)
- Set the address associated with the Flash memory region.

Using FLBEA register (64KB)
- Set the address associated with the Flash memory region.

Using SFDAT register (4KB, 32KB, 64KB)
- Set the chip select bit in the SFMOD register to 0x0(chip select low).
- Write 06h command to the SFDAT register.
- Set the chip select bit in the SFMOD register to 0x1(chip select high).
- Set the chip select bit in the SFMOD register to 0x0(chip select low).
- Write 20h(4KB) or 52h(32KB) or D8h(64KB) command to the SFDAT register
- Write the target address [23:16] to the SFDAT register.
- Write the target address [15:8] to the SFDAT register.
- Write the target address [7:0] to the SFDAT register.
- Set the chip select bit in the SFMOD register to 0x1(chip select high).
- Poll the busy status bit of the FLSTS register until this operation has completed (Sector/Block Erase complete)

5.3.8 Programing Flash memory

Using SFDAT register

- Set the chip select bit in the SFMOD register to 0x0(chip select low).
- Write 06h command to the SFDAT register.
- Set the chip select bit in the SFMOD register to 0x1(chip select high).
- Set the chip select bit in the SFMOD register to 0x0(chip select low).
- Write 02h command to the SFDAT register
- Write the target address [23:16] to the SFDAT register.
- Write the target address [15:8] to the SFDAT register.
- Write the target address [7:0] to the SFDAT register
- Write a 32-bit, 16-bit or 8-bit data up to 256 byte.
- Set the chip select bit in the SFMOD register to 0x1(chip select high).
- Poll the busy status bit of the FLSTS register until this operation has completed (Erase complete)

5.3.9 Reading Flash memory

Using SFDAT register

- Set the chip select bit in the SFMOD register to 0x0(chip select low).
- Write 03h command to the SFDAT register.
- Write the target address [23:16] to the SFDAT register.
- Write the target address [15:8] to the SFDAT register.
- Write the target address [7:0] to the SFDAT register
- Read a 32-bit, 16-bit or 8-bit data up to 256 byte.
- Set the chip select bit in the SFMOD register to 0x1(chip select high).

5.3.10 Power Down and Release Power Down

Using SFDAT register (Power down)

- Set the chip select bit in the SFMOD register to 0x0(chip select low).
- Write B9h command to the SFDAT register.
- Set the chip select bit in the SFMOD register to 0x1(chip select high).

Using SFDAT register (Release Power down)

- Set the chip select bit in the SFMOD register to 0x0(chip select low).
- Write ABh command to the SFBAT register.
- SFDAT(8bit, 16bit, 32bit access 가능) Read
- Set the chip select bit in the SFMOD register to 0x1(chip select high).

5.3.11 Flash Mode Register (FLMOD)

Determines Flash operation mode.
It can access flash data by Single, Dual and Quad bit size.

5.3.12 Flash Baudrate Register (FLBRT)

Determines Flash Baudrate.
It can configure width between high pulse and low pulse of clock frequency..

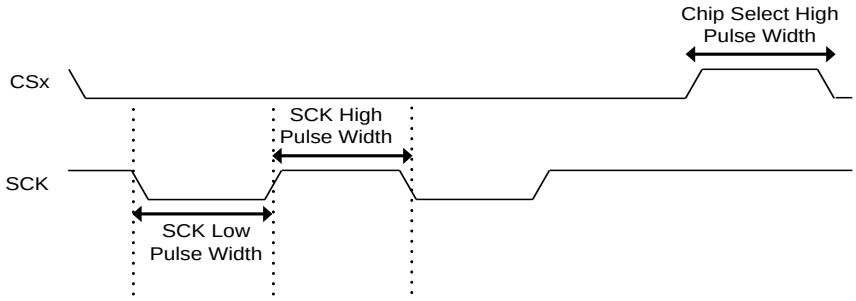


Figure 5-5 SCK and CS timing

5.3.13 Flash Chip Select High Pulse Width Register (FLCSH)

It determines deselect time of Chips select signal.
If the chips select signal is deselected, current status should not be changed.
After read operation, in the case of program tries to read, user keeps 50ns to access Status register after Erase or Program execution.
User connects external Flash memory to *adstar-L,* the value of time is different according to flash type. Due to that reason, user should check the Flash deselect time.

5.3.14 Flash WIP Check Period Register (FLWCP)

This register determines the period of check in hardware, when user writes Flash such as program and erase. According to the value, Flash controller reads status register 0bit (BUSY). If the value of the bit is changed 1 into 0, the write operation is finished.

5.3.15 Flash Clock Delay Register (FLCKDLY)

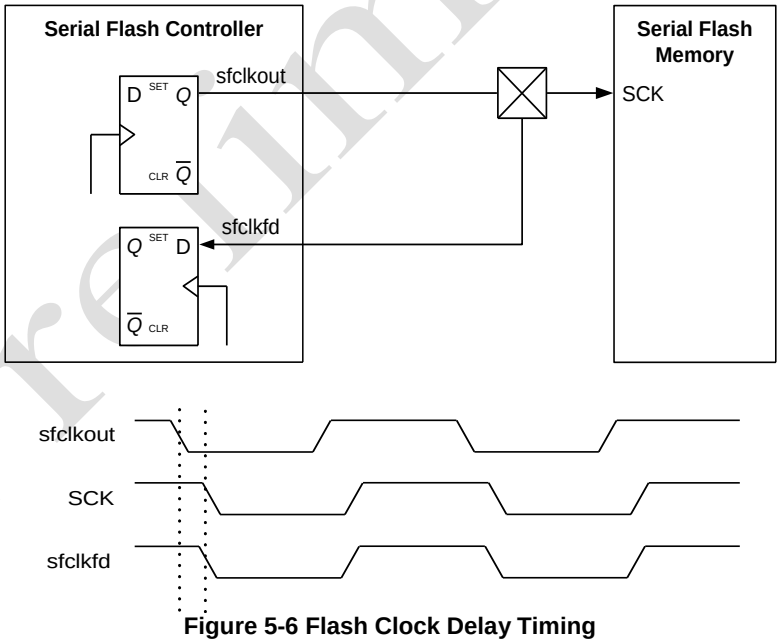


Figure 5-6 Flash Clock Delay Timing

The register is user for correction of Flash read timing.
User can delay read clock according to the value of the register.

5.4 Register Description

5.4.1 Flash Mode Register (FLMOD)

Address : 0x8000_0000

Bit	*R/W*	*Description*	*Default Value*
31:9	R	Reserved	-
8	R/W	Chip select control 1: Chip select signal is controlled by H/W 0: Fix Chip select signal to Low Level	1b
7	R/W	Bus Error Enable 1: When user accesses to Flash in order to write, incurs Bus Error. 0: Allows Flash write access.	1b
6	R	Reserved	-
5	R	EQIO Mode Flag; Checks whether or not this feature is available in flash memory. 1: EQIO Mode 0: Normal Mode If user writes EQIO (38h) to Command Register, Flash changes to EQIO mode.	0
4	R	Performance Enhance Mode; Checks whether or not this feature is available in flash memory. 1: Applied Performance Enhance Mode 0: Normal Mode. If user enables Enhance Mode by writing 1 to FLPEM Register, It is enabled only when the Flash mode is Quad read or EQIO mode.	0
3	R/W	Bus Ready Control 0: Controls bus ready in case of write operation. S/W needs not check flash status. 1: After write operation, S/W checks flash status.	0b
2	R	Reserved	-
1:0	R/W	Flash Read Mode 00: Single Read Mode 01: Dual Read Mode 10: Quad Read Mode 11: Reserved	00b

5.4.2 Flash Baudrate Register (FLBRT)

Address : 0x8000_0004

Bit	R/W	Description	Default Value
31:8	R	Reserved	-
7:4	R/W	SCK High Pulse Width 0000: 1clock 0001: 2clocks 0010: 3clocks … 1110: 15clocks 1111: 16clocks	111b
3:0	R/W	SCK Low Pulse Width 0000: 1clock 0001: 2clocks 0010: 3clocks … 1110: 15clocks 1111: 16clocks	111b

5.4.3 Flash Chip Select High Pulse Width Register (FLCSH)

Address : 0x8000_0008

Bit	R/W	Description	Default Value
31:8	R	Reserved	-
7:0	R/W	Chip Select High Pulse Width (It need 100ns) Delay in hclk_sf clocks for the length that the chip select output is de-asserted between transactions. The minimum delay is always the deselect period to ensure the chip select is never re-asserted within the deselect period. 0000: 1clock 0001: 2clocks 0010: 3clocks … 11111110: 255clocks 11111111: 256clocks	FFh

5.4.4 Flash Performance Enhance Mode Register (FLPEM)

Address : 0x8000_000C

Bit	R/W	Description	Default Value
31:1	R	Reserved	-
0	R/W	Performance Enhance Mode 1: Enabled 0: Disabled	0b

5.4.5 Flash Command Register (FLCMD)

Address : 0x8000_0010

Bit	R/W	Description	Default Value
31:8	R	Reserved	-
7:0	R/W	Flash Command	0b

5.4.6 Flash Status Register (FLSTS)

Address : 0x8000_0014

Bit	R/W	Description	Default Value
31:8	R	Reserved	-
7:0	R/W	Flash Status	0b

5.4.7 Flash Sector Erase Address Register (FLSEA)

Address : 0x8000_0018

Bit	R/W	Description	Default Value
31:24	R	Reserved	-
23:0	R/W	Flash Sector Address to Erase	0b

5.4.8 Flash Block Erase Address Register (FLBEA)

Address : 0x8000_001C

Bit	R/W	Description	Default Value
31:24	R	Reserved	-
23:0	R/W	Flash Block Address to Erase	0b

5.4.9 Flash Data Register (FLDAT)

Address : 0x8000_0020

Bit	R/W	Description	Default Value
31:0	R/W	Flash Data (8, 16, 32-bit supported)	0b

5.4.10 Flash WIP Check Period Register (FLWCP)

Address : 0x8000_0024

Bit	R/W	Description	Default Value
31:0	R/W	Flash WIP Status Check Period	FFFh

5.4.11 Flash Clock Delay Register (FLCKDLY)

Address : 0x8000_0028

Bit	R/W	Description	Default Value
31:4	R	Reserved	-
3:0	R/W	Serial Flash Feed-back Clock Delay Value	0h

5.4.12 Flash 2nd Status Register (FLSTS2)

Address : 0x8000_002C

Bit	R/W	Description	Default Value
31:8	R	Reserved	-
15:8	W	Flash 2nd Status (Winbond only)	-
7:0	R/W	During reading, Flash 2nd Status (Winbond only) During programing Flash 1nd Status (Winbond only)	-

5.4.13 Flash ID Read Register (FLIDR)

Address : 0x8000_0030

Bit	R/W	Description	Default Value
31:24	R	Reserved	-
23:0	R	Serial Flash JEDEC ID Read	000000h

5.4.14 Flash Memory Size Write Register (SFMSIZE)

Address : 0x8000_0034

Bit	R/W	Description	Default Value
31:9	R	Reserved	-
8	R/W	MSACC : SFMSIZE register access bit. To access the SFMSIZE register, you must enable the "MSACC". 1: Enable 0: Disable	0
7:5	R	Reserved	-
4	R/W	Serial Flash chip select 1 enable bit. 1: Chip select 1 enable 0: Chip select 1 disable	0
3:0	R/W	memory size selection register 0000:32Kbyte 0001: 64Kbyte 0010: 128Kbyte 0011: 256Kbyte 0100: 512Kbyte 0101: 1Mbyte 0110: 2Mbyte 0111: 4Mbyte 1000: 8Mbyte 1001: 16Mbyte	4h

6 GPIO (GENERAL PURPOSE I/O)

The GPIO Ports are composed of 8-bit 6 blocks and 7-bit 1 block. The GPIO provides totally 55 I/O ports. Each port can be configured with register easily, and can be used for various input/output and system organization.

6.1 Features

- GP0.x has 8 I/O Ports
- GP1.x has 8 I/O Ports
- GP2.x has 8 I/O ports
- GP3.x has 8 I/O ports
- GP4.x has 8 I/O Ports
- GP5.x has 8 I/O Ports
- GP6.x has 7 I/O ports

6.2 Block Diagram

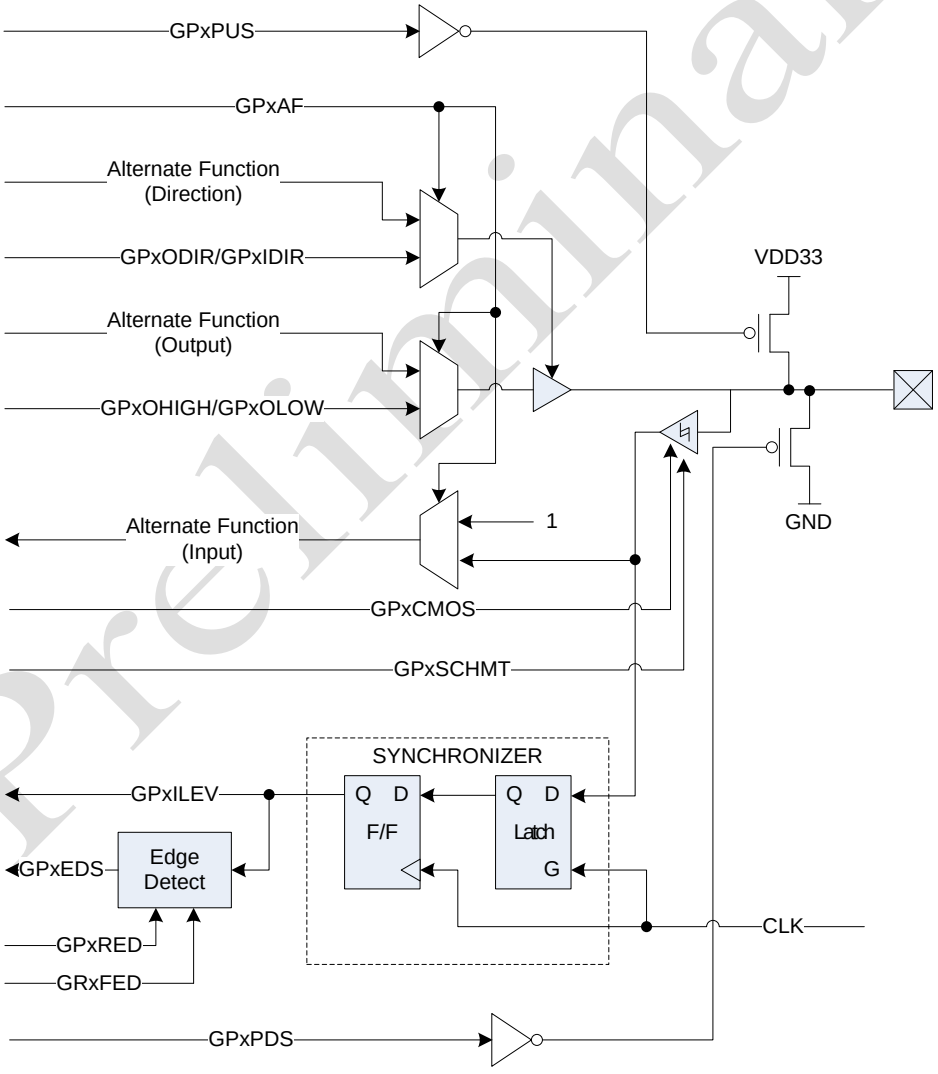


Figure 6-1 GPIO Block Diagram

6.3 Functional Description

6.3.1 Port Control

GPIO Ports are configured as Output mode by GPxODIR register and configured as Input mode by GPxIDIR register port by port. The configured status of each port is stored into GPxDIR register. When user configures GPxODIR register and GPxIDIR register, the value of bit is 1 is configured as the corresponding operation and that of bit is 0 does not affect anything.

The output level of GPIO Ports is set to High Level via GPxOHIGH register under Output mode and is set to Low Level via GPxOLOW register. The status of Output Level can be confirmed by checking GPxOLEV register.

The Input level of GPIO can be confirmed by checking GPxILEV. The Pull-up resistance is connected to each port. User can reduce leakage current if use removes Pull-up under the external input exists or ouput.

Table 6-1 Internal Pull-up Resistance Characteristics

Parameter	*Min*	*Typ*	*Max*	*Unit*
Pull-Up Resistance	34	41	64	KΩ
Pull-Down Resistance	33	44	79	KΩ

6.3.2 Port Edge Detect

External interrupt can be performed for each group by GPIO's Port Edge Detect as well as EIRQ pin. The port provides Rising Edge, Falling Edge and Any Edge modes.

6.4 Register Description

6.4.1 Port Direction Registers (GPxDIR)

Address: 0xFFFF_3000 / 0xFFFF_3040 / 0xFFFF_3080 / 0xFFFF_30C0 / 0xFFFF_3100 / 0xFFFF_3140 / 0xFFFF_3180

Bit	*R/W*	*Description*	*Default Value*
31 : 9	R	Reserved	-
8	R	GPx.OMD : GPx. Output Control Mode bit 0 : Control individual ports 1 : Control a group of 8 ports	0
7 : 0	R	GPx.yDIR : GPx.y Direction bit 0 : Input 1 : Output	0x00

6.4.2 Port Direction Output Mode Setting Registers (GPxODIR)

Address: 0xFFFF_3000 / 0xFFFF_3040 / 0xFFFF_3080 / 0xFFFF_30C0 / 0xFFFF_3100 / 0xFFFF_3140 / 0xFFFF_3180

Bit	*R/W*	*Description*	*Default Value*
31 : 9	R	Reserved	-
8	W	GPx.OPRT : Output Control by Port Mode Setting bit	-
7	W	GPx.7ODIR : GPx.7 Direction Output Mode Setting bit	-
6	W	GPx.6ODIR : GPx.6 Direction Output Mode Setting bit	-
5	W	GPx.5ODIR : GPx.5 Direction Output Mode Setting bit	-
4	W	GPx.4ODIR : GPx.4 Direction Output Mode Setting bit	-
3	W	GPx.3ODIR : GPx.3 Direction Output Mode Setting bit	-
2	W	GPx.2ODIR : GPx.2 Direction Output Mode Setting bit	-
1	W	GPx.1ODIR : GPx.1 Direction Output Mode Setting bit	-
0	W	GPx.0ODIR : GPx.0 Direction Output Mode Setting bit	-

* Port Direction Output Mode Setting bit
0 : No effect 1 : Set to output mode the corresponding bit

6.4.3 Port Direction Input Mode Setting Registers (GPxIDIR)

Address: 0xFFFF_3004 / 0xFFFF_3044 / 0xFFFF_3084 / 0xFFFF_30C4 / 0xFFFF_3104 / 0xFFFF_3144 / 0xFFFF_3184

Bit	R/W	Description	Default Value
31 : 9	R	Reserved	-
8	W	GPx.IPRT : Input Control by Port Mode Setting bit	-
7	W	GPx.7IDIR : GPx.7 Direction Input Mode Setting bit	-
6	W	GPx.6IDIR : GPx.6 Direction Input Mode Setting bit	-
5	W	GPx.5IDIR : GPx.5 Direction Input Mode Setting bit	-
4	W	GPx.4IDIR : GPx.4 Direction Input Mode Setting bit	-
3	W	GPx.3IDIR : GPx.3 Direction Input Mode Setting bit	-
2	W	GPx.2IDIR : GPx.2 Direction Input Mode Setting bit	-
1	W	GPx.1IDIR : GPx.1 Direction Input Mode Setting bit	-
0	W	GPx.0IDIR : GPx.0 Direction Input Mode Setting bit	-

* Port Direction Input Mode Setting bit
  0 : No effect 1 : Set to input mode the corresponding bit

6.4.4 Port Output Data Level Registers (GPxOLEV)

Address: 0xFFFF_3008 / 0xFFFF_3048 / 0xFFFF_3088 / 0xFFFF_30C8 / 0xFFFF_3108 / 0xFFFF_3148 / 0xFFFF_3188

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R	GPx.yOLEV : GPx.y Output Level bit 0 : Low Level 1 : High Level	0xFF

6.4.5 Port Output Data Registers (GPxDOUT)

Address: 0xFFFF_3008 / 0xFFFF_3048 / 0xFFFF_3088 / 0xFFFF_30C8 / 0xFFFF_3108 / 0xFFFF_3148 / 0xFFFF_3188

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R/W	GPx.DO : GPx.Port Output Data	0xFF

* If the value of GPxDIR[8] is 1, It decides GPIO Port ouput by the register.

6.4.6 Port Output Data High Level Setting Registers (GPxOHIGH)

Address: 0xFFFF_3008 / 0xFFFF_3048 / 0xFFFF_3088 / 0xFFFF_30C8 / 0xFFFF_3108 / 0xFFFF_3148 / 0xFFFF_3188

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	W	GPx.7OH : GPx.7 Output Data High Level Setting bit	-
6	W	GPx.6OH : GPx.6 Output Data High Level Setting bit	-
5	W	GPx.5OH : GPx.5 Output Data High Level Setting bit	-
4	W	GPx.4OH : GPx.4 Output Data High Level Setting bit	-
3	W	GPx.3OH : GPx.3 Output Data High Level Setting bit	-
2	W	GPx.2OH : GPx.2 Output Data High Level Setting bit	-
1	W	GPx.1OH : GPx.1 Output Data High Level Setting bit	-
0	W	GPx.0OH : GPx.0 Output Data High Level Setting bit	-

* Port Output Data High Level Setting bit (It is effective only when GPxDIR[8] is 0.)
  0 : No effect
  1 : Set to high level output data the corresponding bit

6.4.7 Port Output Data Low Level Setting Registers (GPxOLOW)

Address: 0xFFFF_300C / 0xFFFF_304C / 0xFFFF_308C / 0xFFFF_30CC / 0xFFFF_310C / 0xFFFF_314C / 0xFFFF_318C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	W	GPx.7OL : GPx.7 Output Data Low Level Setting bit	-
6	W	GPx.6OL : GPx.6 Output Data Low Level Setting bit	-
5	W	GPx.5OL : GPx.5 Output Data Low Level Setting bit	-
4	W	GPx.4OL : GPx.4 Output Data Low Level Setting bit	-
3	W	GPx.3OL : GPx.3 Output Data Low Level Setting bit	-
2	W	GPx.2OL : GPx.2 Output Data Low Level Setting bit	-
1	W	GPx.1OL : GPx.1 Output Data Low Level Setting bit	-
0	W	GPx.0OL : GPx.0 Output Data Low Level Setting bit	-

* Port Output Data Low Level Setting bit (It is effective only when GPxDIR[8] is 0.)
0 : No effect
1 : Set to low level output data the corresponding bit

6.4.8 Port Input Data Level Registers (GPxILEV)

Address: 0xFFFF_3010 / 0xFFFF_3050 / 0xFFFF_3090 / 0xFFFF_30D0 / 0xFFFF_3110 / 0xFFFF_3150 / 0xFFFF_3190

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	R	GPx.7ILEV : GPx.7 Input Level bit 0 : Low Level 1 : High Level	-
6	R	GPx.6ILEV : GPx.6 Input Level bit 0 : Low Level 1 : High Level	-
5	R	GPx.5ILEV : GPx.5 Input Level bit 0 : Low Level 1 : High Level	-
4	R	GPx.4ILEV : GPx.4 Input Level bit 0 : Low Level 1 : High Level	-
3	R	GPx.3ILEV : GPx.3 Input Level bit 0 : Low Level 1 : High Level	-
2	R	GPx.2ILEV : GPx.2 Input Level bit 0 : Low Level 1 : High Level	-
1	R	GPx.1ILEV : GPx.1 Input Level bit 0 : Low Level 1 : High Level	-
0	R	GPx.0ILEV : GPx.0 Input Level bit 0 : Low Level 1 : High Level	-

6.4.9 Port Pull-up Status Registers (GPxPUS)

Address: 0xFFFF_3018 / 0xFFFF_3058 / 0xFFFF_3098 / 0xFFFF_30D8 / 0xFFFF_3118 / 0xFFFF_3158 / 0xFFFF_3198

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R	GPx.yUP : GPx.y Pull-up Status bit 0 : Pull-up Disable 1 : Pull-up Enable	0x0

6.4.10 Port Pull-up Enable Registers (GPxPUEN)

Address: 0xFFFF_3018 / 0xFFFF_3058 / 0xFFFF_3098 / 0xFFFF_30D8 / 0xFFFF_3118 / 0xFFFF_3158 / 0xFFFF_3198

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	W	GPx.7PUEN : GPx.7 Pull-up enable bit	-
6	W	GPx.6PUEN : GPx.6 Pull-up enable bit	-
5	W	GPx.5PUEN : GPx.5 Pull-up enable bit	-
4	W	GPx.4PUEN : GPx.4 Pull-up enable bit	-
3	W	GPx.3PUEN : GPx.3 Pull-up enable bit	-
2	W	GPx.2PUEN : GPx.2 Pull-up enable bit	-
1	W	GPx.1PUEN : GPx.1 Pull-up enable bit	-
0	W	GPx.0PUEN : GPx.0 Pull-up enable bit	-

* Port Pull-up enable bit
  0 : No effect
  1 : the pull up of corresponding bit is set to enable.

6.4.11 Port Pull-up Disable Registers (GPxPUDIS)

Address: 0xFFFF_301C / 0xFFFF_305C / 0xFFFF_309C / 0xFFFF_30DC / 0xFFFF_311C / 0xFFFF_315C / 0xFFFF_319C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	W	GPx.7PUDIS : GPx.7 Pull-up disable bit	-
6	W	GPx.6PUDIS : GPx.6 Pull-up disable bit	-
5	W	GPx.5PUDIS : GPx.5 Pull-up disable bit	-
4	W	GPx.4PUDIS : GPx.4 Pull-up disable bit	-
3	W	GPx.3PUDIS : GPx.3 Pull-up disable bit	-
2	W	GPx.2PUDIS : GPx.2 Pull-up disable bit	-
1	W	GPx.1PUDIS : GPx.1 Pull-up disable bit	-
0	W	GPx.0PUDIS : GPx.0 Pull-up disable bit	-

* Port Pull-up disable bit
  0 : No effect
  1 : the pull up of corresponding bit is set to disable.

6.4.12 Port Rising Edge Detect Registers (GPxRED)

Address: 0xFFFF_3020 / 0xFFFF_3060 / 0xFFFF_30A0 / 0xFFFF_30E0 / 0xFFFF_3120 / 0xFFFF_3160 / 0xFFFF_31A0

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	R/W	GPx.7RED : GPx.7 Rising Edge Detect bit 0 : Disable 1 : Enable	0
6	R/W	GPx.6RED : GPx.6 Rising Edge Detect bit 0 : Disable 1 : Enable	0
5	R/W	GPx.5RED : GPx.5 Rising Edge Detect bit 0 : Disable 1 : Enable	0
4	R/W	GPx.4RED : GPx.4 Rising Edge Detect bit 0 : Disable 1 : Enable	0
3	R/W	GPx.3RED : GPx.3 Rising Edge Detect bit 0 : Disable 1 : Enable	0
2	R/W	GPx.2RED : GPx.2 Rising Edge Detect bit 0 : Disable 1 : Enable	0
1	R/W	GPx.1RED : GPx.1 Rising Edge Detect bit 0 : Disable 1 : Enable	0
0	R/W	GPx.0RED : GPx.0 Rising Edge Detect bit 0 : Disable 1 : Enable	0

* When both Rising Edge and Falling Edge are set, Edge detect mode becomes Any Edge mode.

6.4.13 Port Falling Edge Detect Registers (GPxFED)

Address: 0xFFFF_3024 / 0xFFFF_3064 / 0xFFFF_30A4 / 0xFFFF_30E4 / 0xFFFF_3124 / 0xFFFF_3164 / 0xFFFF_31A4

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	R/W	GPx.7FED : GPx.7 Falling Edge Detect bit 0 : Disable 1 : Enable	0
6	R/W	GPx.6FED : GPx.6 Falling Edge Detect bit 0 : Disable 1 : Enable	0
5	R/W	GPx.5FED : GPx.5 Falling Edge Detect bit 0 : Disable 1 : Enable	0
4	R/W	GPx.4FED : GPx.4 Falling Edge Detect bit 0 : Disable 1 : Enable	0
3	R/W	GPx.3FED : GPx.3 Falling Edge Detect bit 0 : Disable 1 : Enable	0
2	R/W	GPx.2FED : GPx.2 Falling Edge Detect bit 0 : Disable 1 : Enable	0
1	R/W	GPx.1FED : GPx.1 Falling Edge Detect bit 0 : Disable 1 : Enable	0
0	R/W	GPx.0FED : GPx.0 Falling Edge Detect bit 0 : Disable 1 : Enable	0

* When both Rising Edge and Falling Edge are set, Edge detect mode becomes Any Edge mode.

6.4.14 Port Edge Detect Status Registers (GPxEDS)

Address: 0xFFFF_3028 / 0xFFFF_3068 / 0xFFFF_30A8 / 0xFFFF_30E8 / 0xFFFF_3128 / 0xFFFF_3168 / 0xFFFF_31A8

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	R/W	GPx.7EDS : GPx.7 Edge Detect Status bit	0
6	R/W	GPx.6EDS : GPx.6 Edge Detect Status bit	0
5	R/W	GPx.5EDS : GPx.5 Edge Detect Status bit	0
4	R/W	GPx.4EDS : GPx.4 Edge Detect Status bit	0
3	R/W	GPx.3EDS : GPx.3 Edge Detect Status bit	0
2	R/W	GPx.2EDS : GPx.2 Edge Detect Status bit	0
1	R/W	GPx.1EDS : GPx.1 Edge Detect Status bit	0
0	R/W	GPx.0EDS : GPx.0 Edge Detect Status bit	0

* Port Edge Detect Status bit
  0 : No edge detect has occurred on port
  1 : Edge detect has occurred on port

* Status bits are cleared by writing a one to them.
* Writing a zero to a status bit are no effect.

6.4.15 Port Open Drain Mode Control Registers (GPxODM)

Address: 0xFFFF_302C / 0xFFFF_306C / 0xFFFF_30AC / 0xFFFF_30EC / 0xFFFF_312C / 0xFFFF_316C / 0xFFFF_31AC

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R/W	GPx.yOD : GPx.y Open Drain Mode Setting bit 0 : Normal 1 : Open Drain	0

6.4.16 Port Schmitt Input Enable Registers (GPxSHMT)

Address: 0xFFFF_3034 / 0xFFFF_3074 / 0xFFFF_30B4 / 0xFFFF_30F4 / 0xFFFF_3134 / 0xFFFF_3174 / 0xFFFF_31B4

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	W	GPx.7SHMT : GPx.7 Schmitt input enable bit	0
6	W	GPx.6SHMT : GPx.6 Schmitt input enable bit	0
5	W	GPx.5SHMT : GPx.5 Schmitt input enable bit	0
4	W	GPx.4SHMT : GPx.4 Schmitt input enable bit	0
3	W	GPx.3SHMT : GPx.3 Schmitt input enable bit	0
2	W	GPx.2SHMT : GPx.2 Schmitt input enable bit	0
1	W	GPx.1SHMT : GPx.1 Schmitt input enable bit	0
0	W	GPx.0SHMT : GPx.0 Schmitt input enable bit	0

* Port Schmitt input enable bit
  0 : CMOS input mode
  1 : Schmitt input mode

6.4.17 Port Pull-down Status Registers (GPxPDS)

Address: 0xFFFF_3030 / 0xFFFF_3070 / 0xFFFF_30B0 / 0xFFFF_30F0 / 0xFFFF_3130 / 0xFFFF_3170 / 0xFFFF_31B0

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R	GPx.yDN : GPx.y Pull-down Status bit 0 : Pull-down Disable 1 : Pull-down Enable	0x0

6.4.18 Port Pull-down Enable Registers (GPxPDEN)

Address: 0xFFFF_3030 / 0xFFFF_3070 / 0xFFFF_30B0 / 0xFFFF_30F0 / 0xFFFF_3130 / 0xFFFF_3170 / 0xFFFF_31B0

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	W	GPx.7PDEN : GPx.7 Pull-down enable bit	-
6	W	GPx.6PDEN : GPx.6 Pull-down enable bit	-
5	W	GPx.5PDEN : GPx.5 Pull-down enable bit	-
4	W	GPx.4PDEN : GPx.4 Pull-down enable bit	-
3	W	GPx.3PDEN : GPx.3 Pull-down enable bit	-
2	W	GPx.2PDEN : GPx.2 Pull-down enable bit	-
1	W	GPx.1PDEN : GPx.1 Pull-down enable bit	-
0	W	GPx.0PDEN : GPx.0 Pull-down enable bit	-

* Port Pull-down enable bit
  0 : No effect
  1 : the pull down of corresponding bit is set to enable.

6.4.19 Port Pull-down Disable Registers (GPxPDDIS)

Address: 0xFFFF_301C / 0xFFFF_305C / 0xFFFF_309C / 0xFFFF_30DC / 0xFFFF_311C / 0xFFFF_315C / 0xFFFF_319C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	W	GPx.7PDDIS : GPx.7 Pull-down disable bit	-
6	W	GPx.6PDDIS : GPx.6 Pull-down disable bit	-
5	W	GPx.5PDDIS : GPx.5 Pull-down disable bit	-
4	W	GPx.4PDDIS : GPx.4 Pull-down disable bit	-
3	W	GPx.3PDDIS : GPx.3 Pull-down disable bit	-
2	W	GPx.2PDDIS : GPx.2 Pull-down disable bit	-
1	W	GPx.1PDDIS : GPx.1 Pull-down disable bit	-
0	W	GPx.0PDDIS : GPx.0 Pull-down disable bit	-

* Port Pull-down disable bit
  0 : No effect
  1 : the pull down of corresponding bit is set to disable.

7 PIN MUX

Up to three different peripheral functions are multiplexed along with a general input/ouput(GPIO) function per pin.

7.1 Pin Mux register

Register	bit	1st	2nd	3rd	4th	Default value
		00	01	10	11	
GP0 Mux 0x80023400	1:0	uart_tx[1]	cap_in[0]		PG0.0	0xffff or 0x557f (nand boot)
	3:2	uart_rx[1]	cap_in[1]		PG0.1	
	5:4	spi_lcd_cs			PG0.2	
	7:6	spi_lcd _sdi	nand_d[7]		PG0.3	
	9:8	spi_lcd _sdo	nand_d[6]		PG0.4	
	11:10	spi_lcd _scl	nand_d[5]		PG0.5	
	13:12		nand_d[4]	sd_clk	PG0.6	
	15:14	spi_sdo	nand_d[3]	sd_d[3]	PG0.7	
GP1 Mux 0x80023404	1:0	spi_sdi	nand_d[2]	sd_d[2]	PG1.0	0x003f or 0x5555 (nand boot)
	3:2	spi_cs	nand_d[1]	sd_d[1]	PG1.1	
	5:4	spi_scl	nand_d[0]	sd_d[0]	PG1.2	
	7:6	sf_hold (d3)	nand_wrx		PG1.3	
	9:8	sf_clk	nand_ale		PG1.4	
	11:10	sf_di (d0)	nand_cle		PG1.5	
	13:12	sf_cs1	nand_cs		PG1.6	
	15:14	sf_wp (d2)	nand_rdx		PG1.7	
GP2 Mux 0x80023408	1:0	sf_do (d1)	nand_busy		PG2.0	0xfff0 or 0xfffd (nand boot)
	3:2	sf_cs0	sd_cmd		PG2.1	
	5:4	twi_sda	usb_host_in		PG2.2	
	7:6	twi_scl	usb_host_out		PG2.3	
	9:8	uart_tx[0]			PG2.4	
	11:10	uart_rx[0]			PG2.5	
	13:12	lcd_r[0]			PG2.6	
	15:14	lcd_r[1]			PG2.7	
GP3 Mux 0x8002340C	1:0	lcd_r[2]			PG3.0	0x5fff
	3:2	lcd_r[3]			PG3.1	
	5:4	lcd_r[4]			PG3.2	
	7:6	lcd_r[5]			PG3.3	
	9:8	lcd_r[6]			PG3.4	
	11:10	lcd_r[7]			PG3.5	
	13:12	lcd_g[0]	dbg_sck		PG3.6	
	15:14	lcd_g[1]	dbg_sda		PG3.7	
GP4 Mux 0x80023410	1:0	lcd_g[2]			PG4.0	0xffff
	3:2	lcd_g[3]			PG4.1	
	5:4	lcd_g[4]			PG4.2	
	7:6	lcd_g[5]			PG4.3	
	9:8	lcd_g[6]			PG4.4	
	11:10	lcd_g[7]			PG4.5	
	13:12	lcd_b[0]	ext_irq[0]		PG4.6	
	15:14	lcd_b[1]	ext_irq[1]		PG4.7	
GP5 Mux 0x80023414	1:0	lcd_b[2]			PG5.0	0xffff
	3:2	lcd_b[3]			PG5.1	
	5:4	lcd_b[4]			PG5.2	
	7:6	lcd_b[5]			PG5.3	
	9:8	lcd_b[6]			PG5.4	
	11:10	lcd_b[7]			PG5.5	
	13:12	dotclk			PG5.6	
	15:14	disp_en			PG5.7	
GP6 Mux 0x80023418	1:0	hsync			PG6.0	0xffff
	3:2	vsync	tm_out[0]		PG6.1	
	5:4	lcd_clk_in	tm_out[1]		PG6.2	
	7:6	pwm_p0			PG6.3	
	9:8	pwm_n0			PG6.4	
	11:10	pwm_p1			PG6.5	
	13:12	pwm_n1			PG6.6	

8 INTERRUPT CONTROLLER

adStar-L provides 32-channel interrupt input that consists of 30 interrupts from internal devices such as Timer, SPI, TWI, UART and 2-external interrupts.

8.1 Features

- 32 channel interrupts (2-external interrupts and 30-internal interrupts)
- 5 operating configurations for external interrupts
- 2 operating configurations for internal interrupts
- Interrupt enable for each channel
- Interrupt masking for each channel
- Programmable interrupt priority

8.2 Functional Description

Interrupt handling processes are following steps.

1. Each interrupts source requests to interrupt controller.
2. After choose the interrupt according to Interrupt Enable Register, the interrupt controller stores the interrupt of Interrupt Pending Register.
3. After decide interrupt priority, the interrupt controller request to CPU.
4. If the CPU receive an interrupt request, CPU's interrupt is disabled and reads interrupt vector address from interrupt vector table. After CPU reads the address, the CPU calls Interrupt Service Routine (ISR).
5. Executes ISR
6. After finish executing ISR, CPU removes Interrupt value in the Interrupt Pending Register by writing Vector value into Interrupt Pending Clear Register.
7. CPU's interrupt is enabled after finish (return) ISR routine.

Nested Interrupt handling processes are following steps.

1. Each interrupts source requests to interrupt controller.
2. After choose the interrupt according to Interrupt Enable Register, the interrupt controller stores the interrupt of Interrupt Pending Register.
3. After decide interrupt priority, the interrupt controller request to CPU.
4. If the CPU receive an interrupt request, CPU's interrupt is disabled and reads interrupt vector address from interrupt vector table. After CPU reads the address, the CPU calls Interrupt Service Routine (ISR).
5. In order to allow nested interrupt, CPU removes interrupt that is already stored into Interrupt Pending Register by writing correspond vector value to Interrupt Pending Clear Register. After that CPU's interrupt is enabled by asm("set 13") instruction.
6. Executes ISR.
7. If interrupt are occurred during ISR execution, CPU allows the interrupt and then execute the corresponding ISR.
8. After finish the new ISR execution, CPU returns the old ISR and then continues to execute.
9. Finish the ISR.

8.2.1 Interrupt Vector and Priority

EIRQ0 has the highest priority. The size of interrupt address is 4-byte because interrupt vector address is 32-bit addressing mode.

Table 8-1 Interrupt Vector & Priority

Index	*Vector No.*	*Description*	*Vector Address*
31	0x3F	SWD Interrupt Use edge method Clock_ctrl_r[0]	0x000000FC
30	0x3E	MJPEG 1 Interrupt	0x000000F8
29	0x3D	Capture Over Interrupt	0x000000F4
28	0x3C	SPI_LCD Interrupt	0x000000F0
27	0x3B	RTC Alarm Interrupt	0x000000EC
26	0x3A	RTC Interrupt	0x000000E8
25	0x39	TWI Interrupt	0x000000E4
24	0x38	NAND Interupt	0x000000E0
23	0x37	WDT Interrupt	0x000000DC
22	0x36	DMA CH5 Interrupt , GPIO 3 interrupt, GPIO 6 interrupt	0x000000D8
21	0x35	SDCard Interrupt	0x000000D4
20	0x34	DMA CH4 Interrupt , GPIO 2 Interrupt, GPIO 5 Interrupt	0x000000D0
19	0x33	MJPEG 0 Interrupt	0x000000CC
18	0x32	SPI Interrupt	0x000000C8
17	0x31	DMA CH3 Interrupt	0x000000C4
16	0x30	UART 1 Interrupt	0x000000C0
15	0x2F	GPIO 1 Interrupt, GPIO 4 Interrupt	0x000000BC
14	0x2E	USB host interrupt, Device Interupt	0x000000B8
13	0x2D	ADC Interrupt	0x000000B4
12	0x2C	DMA CH2 Interrupt	0x000000B0
11	0x2B	PMC interrupt	0x000000AC
10	0x2A	Timer 1 Interrupt	0x000000A8
9	0x29	DMA CH1 Interrupt	0x000000A4
8	0x28	UART 0 Interrupt	0x000000A0
7	0x27	GPIO 0 Interrupt	0x0000009C
6	0x26	DMA CH0 Interrupt	0x00000098
5	0x25	LCD Frame sync Interrupt	0x00000094
4	0x24	EIRQ1 Interrupt	0x00000090
3	0x23	Sound Mixer Interrupt	0x0000008C
2	0x22	Timer 0 Interrupt	0x00000088
1	0x21	Core timer Interrupt	0x00000084
0	0x20	EIRQ0 Interrupt (Highest Priority)	0x00000080

8.2.2 External Interrupt (EIRQx)

External Interrupt receives 5 types of external interrupt by configuring EINTMOD register.

- In the Low Level Mode, Interrupt is occurred every system cycle during External Interrupt signal keeps “Low“.
- In the High Level Mode, Interrupt is occurred every system cycle during External Interrupt signal keeps “High“.
- In the Falling Edge Mode, Interrupt is occurred when External Interrupt signal changes “High“ to “Low“.
- In the Rising Edge Mode, Interrupt is occurred when External Interrupt signal changes “Low“ to “High“
- In the Any Edge Mode, Interrupt is occurred when External Interrupt signal changes “Low“ to “High“ or “High“ to “Low“.

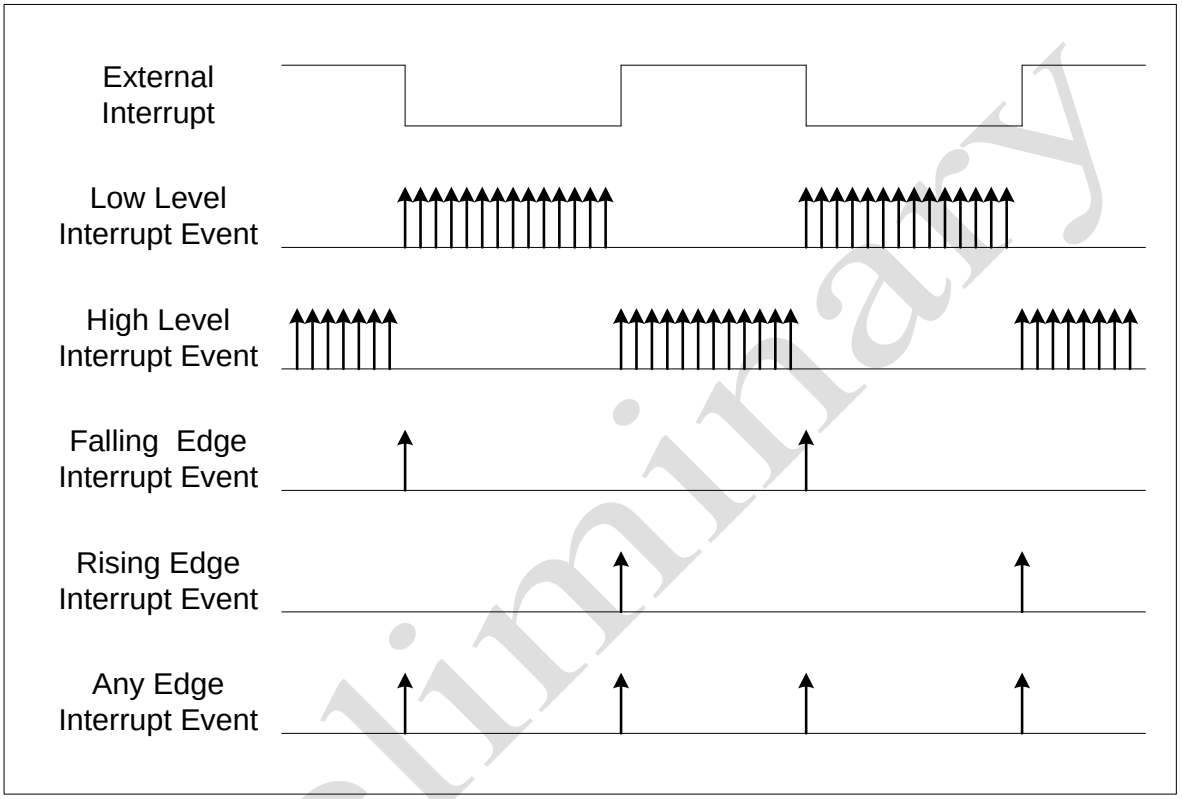


Figure 8-1 External Interrupt Mode

8.2.3 Internal Interrupt Mode

All of the internal interrupts are executed in “Rising Edge Mode”. However, if user wants to “High Level” interrupt handling, user can configures Internal Interrupt Mode Register.

8.2.4 Interrupt Pending and Interrupt Pending Clear

User can check interrupt status via Interrupt Pending Registers. An interrupt is stored into Interrupt Pending Register until be cleared by Interrupt Pending Clear Register. Also, if higher priority interrupt is stored in the Interrupt Pending Registers without Masking, the currently occurred interrupt is waiting for all of the higher priority interrupts are cleared.

In order to clear the interrupts that are stored in Interrupt Pending Registers, user should write the corresponding vector number into Interrupt Pending Clear Register.

8.2.5 Interrupt Enable

An interrupt, which is masked by Interrupt Mask Registers, is stored in Interrupt Pending Registers. However, an interrupt, which is disabled by Interrupt Enable Registers (IENR), is not stored in the Interrupt Pending Registers. Therefore, user can disable an interrupt that not allowed by using the registers (IENR).

8.2.6 Interrupt Mask Set/Clear Register

If the register is set, an interrupt request is enabled, otherwise disabled..

CPU executes corresponding interrupt request by Interrupt Mask Registers. If the Interrupt Mask Set bit is 1, the interrupt controller requests the interrupt service to CPU. However, if the Interrupt Mask Clear bit is 1, the interrupt controller does not request the interrupt service to CPU.

Although, the Mask bit is 0, because an interrupt is stored into Interrupt Pending Registers (IPR), if user sets the Mask bit to 1, the interrupt controller requests interrupt service stored in Interrupt Pending Registers in the order of priority.

8.3 Register Description

8.3.1 Interrupt Pending Clear Register (INTPENDCLR)

Address : 0xFFFF_0000

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	W	Interrupt Pending Register Clear Value (0x20 ~ 0x3F)	0xFF

* In order to clear Interrupt Pending Register, user should clear according to the Interrupt Vector No. (Refer to Interrupt Vector No.)

8.3.2 External Interrupt Mode and External PIN Level Register (EINTMOD)

Address : 0xFFFF_0004

Bit	R/W	Description	Default Value
31:8	R	Reserved	-
7	R	EIRQ1ST : EIRQ1 PIN Level	-
6 : 4	R/W	EIRQ1MOD : EIRQ1 Active State 000 : Low Level 001 : High Level 010 : Falling Edge 011 : Rising Edge 1xx : Any Edge	010
3	R	EIRQ0ST : EIRQ0 PIN Level	-
2 : 0	R/W	EIRQ0MOD : EIRQ0 Active State 000 : Low Level 001 : High Level 010 : Falling Edge 011 : Rising Edge 1xx : Any Edge	010

8.3.3 Internal Interrupt Mode Register (IINTMODn)

Address : 0xFFFF_0008

Bit	R/W	Description	Default Value
31	R/W	Vector No. 0x3F Interrupt Mode bit	0
30	R/W	Vector No. 0x3E Interrupt Mode bit	0
29	R/W	Vector No. 0x3D Interrupt Mode bit	0
28	R/W	Vector No. 0x3C Interrupt Mode bit	-
27	R/W	Vector No. 0x3B Interrupt Mode bit	0
26	R/W	Vector No. 0x3A Interrupt Mode bit	0
25	R/W	Vector No. 0x39 Interrupt Mode bit	0
24	-	Reserved	-
23	R/W	Vector No. 0x37 Interrupt Mode bit	0
22	R/W	Vector No. 0x36 Interrupt Mode bit	0
21	R/W	Vector No. 0x35 Interrupt Mode bit	0
20	R/W	Vector No. 0x34 Interrupt Mode bit	-
19	R/W	Vector No. 0x33 Interrupt Mode bit	0
18	R/W	Vector No. 0x32 Interrupt Mode bit	0
17	R/W	Vector No. 0x31 Interrupt Mode bit	0
16	-	Reserved	-
15	R/W	Vector No. 0x2F Interrupt Mode bit	0
14	R/W	Vector No. 0x2E Interrupt Mode bit	0
13	R/W	Vector No. 0x2D Interrupt Mode bit	0
12	R/W	Vector No. 0x2C Interrupt Mode bit	-
11	R/W	Vector No. 0x2B Interrupt Mode bit	0
10	R/W	Vector No. 0x2A Interrupt Mode bit	0
9	R/W	Vector No. 0x29 Interrupt Mode bit	0
8	-	Reserved	-
7	R/W	Vector No. 0x27 Interrupt Mode bit	0
6	R/W	Vector No. 0x26 Interrupt Mode bit	0
5	R/W	Vector No. 0x25 Interrupt Mode bit	0
4	R/W	Vector No. 0x24 Interrupt Mode bit	-
3	R/W	Vector No. 0x23 Interrupt Mode bit	0
2	R/W	Vector No. 0x22 Interrupt Mode bit	0
1	R/W	Vector No. 0x21 Interrupt Mode bit	0
0	-	Reserved	-

* Internal Interrupt Mode bit
  0 : High Level Mode
  1 : Rising Edge Mode

8.3.4 Interrupt Pending Register (INTPENDn)

Address : 0xFFFF_000C

Bit	R/W	Description	Default Value
31	R	Vector No. 0x3F Interrupt Pending bit	-
30	R	Vector No. 0x3E Interrupt Pending bit	-
29	R	Vector No. 0x3D Interrupt Pending bit	-
28	R	Vector No. 0x3C Interrupt Pending bit	-
27	R	Vector No. 0x3B Interrupt Pending bit	-
26	R	Vector No. 0x3A Interrupt Pending bit	-
25	R	Vector No. 0x39 Interrupt Pending bit	-
24	R	Vector No. 0x38 Interrupt Pending bit	-
23	R	Vector No. 0x37 Interrupt Pending bit	-
22	R	Vector No. 0x36 Interrupt Pending bit	-
21	R	Vector No. 0x35 Interrupt Pending bit	-
20	R	Vector No. 0x34 Interrupt Pending bit	-
19	R	Vector No. 0x33 Interrupt Pending bit	-
18	R	Vector No. 0x32 Interrupt Pending bit	-
17	R	Vector No. 0x31 Interrupt Pending bit	-
16	R	Vector No. 0x30 Interrupt Pending bit	-
15	R	Vector No. 0x2F Interrupt Pending bit	-
14	R	Vector No. 0x2E Interrupt Pending bit	-
13	R	Vector No. 0x2D Interrupt Pending bit	-
12	R	Vector No. 0x2C Interrupt Pending bit	-
11	R	Vector No. 0x2B Interrupt Pending bit	-
10	R	Vector No. 0x2A Interrupt Pending bit	-
9	R	Vector No. 0x29 Interrupt Pending bit	-
8	R	Vector No. 0x28 Interrupt Pending bit	-
7	R	Vector No. 0x27 Interrupt Pending bit	-
6	R	Vector No. 0x26 Interrupt Pending bit	-
5	R	Vector No. 0x25 Interrupt Pending bit	-
4	R	Vector No. 0x24 Interrupt Pending bit	-
3	R	Vector No. 0x23 Interrupt Pending bit	-
2	R	Vector No. 0x22 Interrupt Pending bit	-
1	R	Vector No. 0x21 Interrupt Pending bit	-
0	R	Vector No. 0x20 Interrupt Pending bit	-

* Each bit of Interrupt Pending Register indicates the corresponding interrupt is occurred. The value of the Interrupt Pending Register is cleared by Interrupt Pending Clear Register. Generally, the interrupt is cleared when the interrupt request is finished.

8.3.5 Interrupt Enable Register (INTENn)

Address : 0xFFFF_0010

Bit	R/W	Description	Default Value
31	R/W	Vector No. 0x3F Interrupt Enable bit	0
30	R/W	Vector No. 0x3E Interrupt Enable bit	0
29	R/W	Vector No. 0x3D Interrupt Enable bit	0
28	R/W	Vector No. 0x3C Interrupt Enable bit	0
27	R/W	Vector No. 0x3B Interrupt Enable bit	0
26	R/W	Vector No. 0x3A Interrupt Enable bit	0
25	R/W	Vector No. 0x39 Interrupt Enable bit	0
24	R/W	Vector No. 0x38 Interrupt Enable bit	0
23	R/W	Vector No. 0x37 Interrupt Enable bit	0
22	R/W	Vector No. 0x36 Interrupt Enable bit	0
21	R/W	Vector No. 0x35 Interrupt Enable bit	0
20	R/W	Vector No. 0x34 Interrupt Enable bit	0
19	R/W	Vector No. 0x33 Interrupt Enable bit	0
18	R/W	Vector No. 0x32 Interrupt Enable bit	0
17	R/W	Vector No. 0x31 Interrupt Enable bit	0
16	R/W	Vector No. 0x30 Interrupt Enable bit	0
15	R/W	Vector No. 0x2F Interrupt Enable bit	0
14	R/W	Vector No. 0x2E Interrupt Enable bit	0
13	R/W	Vector No. 0x2D Interrupt Enable bit	0
12	R/W	Vector No. 0x2C Interrupt Enable bit	0
11	R/W	Vector No. 0x2B Interrupt Enable bit	0
10	R/W	Vector No. 0x2A Interrupt Enable bit	0
9	R/W	Vector No. 0x29 Interrupt Enable bit	0
8	R/W	Vector No. 0x28 Interrupt Enable bit	0
7	R/W	Vector No. 0x27 Interrupt Enable bit	0
6	R/W	Vector No. 0x26 Interrupt Enable bit	0
5	R/W	Vector No. 0x25 Interrupt Enable bit	0
4	R/W	Vector No. 0x24 Interrupt Enable bit	0
3	R/W	Vector No. 0x23 Interrupt Enable bit	0
2	R/W	Vector No. 0x22 Interrupt Enable bit	0
1	R/W	Vector No. 0x21 Interrupt Enable bit	0
0	R/W	Vector No. 0x20 Interrupt Enable bit	0

* Interrupt Enable bit
  0 : Interrupt Disable and Pending Clear
  1 : Interrupt Enable

8.3.6 Interrupt Mask Status Register (INTMASKn)

Address : 0xFFFF_0014

Bit	R/W	Description	Default Value
31 : 0	R	Interrupt Mask Status Register	0x0000_0000

* Can check all of the Mask bit status.

8.3.7 Interrupt Mask Set Register (INTMASKSETn)

Address : 0xFFFF_0014h

Bit	R/W	Description	Default Value
31	W	Vector No. 0x3F Interrupt Request Set bit	0
30	W	Vector No. 0x3E Interrupt Request Set bit	0
29	W	Vector No. 0x3D Interrupt Request Set bit	0
28	W	Vector No. 0x3C Interrupt Request Set bit	0
27	W	Vector No. 0x3B Interrupt Request Set bit	0
26	W	Vector No. 0x3A Interrupt Request Set bit	0
25	W	Vector No. 0x39 Interrupt Request Set bit	0
24	W	Vector No. 0x38 Interrupt Request Set bit	0
23	W	Vector No. 0x37 Interrupt Request Set bit	0
22	W	Vector No. 0x36 Interrupt Request Set bit	0
21	W	Vector No. 0x35 Interrupt Request Set bit	0
20	W	Vector No. 0x34 Interrupt Request Set bit	0
19	W	Vector No. 0x33 Interrupt Request Set bit	0
18	W	Vector No. 0x32 Interrupt Request Set bit	0
17	W	Vector No. 0x31 Interrupt Request Set bit	0
16	W	Vector No. 0x30 Interrupt Request Set bit	0
15	W	Vector No. 0x2F Interrupt Request Set bit	0
14	W	Vector No. 0x2E Interrupt Request Set bit	0
13	W	Vector No. 0x2D Interrupt Request Set bit	0
12	W	Vector No. 0x2C Interrupt Request Set bit	0
11	W	Vector No. 0x2B Interrupt Request Set bit	0
10	W	Vector No. 0x2A Interrupt Request Set bit	0
9	W	Vector No. 0x29 Interrupt Request Set bit	0
8	W	Vector No. 0x28 Interrupt Request Set bit	0
7	W	Vector No. 0x27 Interrupt Request Set bit	0
6	W	Vector No. 0x26 Interrupt Request Set bit	0
5	W	Vector No. 0x25 Interrupt Request Set bit	0
4	W	Vector No. 0x24 Interrupt Request Set bit	0
3	W	Vector No. 0x23 Interrupt Request Set bit	0
2	W	Vector No. 0x22 Interrupt Request Set bit	0
1	W	Vector No. 0x21 Interrupt Request Set bit	0
0	W	Vector No. 0x20 Interrupt Request Set bit	0

* Interrupt Request Set bit
  0 : No Effect interrupt Mask.
  1 : Pending interrupt is allowed to become active (interrupts sent to CPU).

8.3.8 Interrupt Mask Clear Register (INTMASKCLRn)

Address : 0xFFFF_0018

Bit	*R/W*	*Description*	*Default Value*
31	W	Vector No. 0x3F Interrupt Req. Clear bit	0
30	W	Vector No. 0x3E Interrupt Req. Clear bit	0
29	W	Vector No. 0x3D Interrupt Req. Clear bit	0
28	W	Vector No. 0x3C Interrupt Req. Clear bit	0
27	W	Vector No. 0x3B Interrupt Req. Clear bit	0
26	W	Vector No. 0x3A Interrupt Req. Clear bit	0
25	W	Vector No. 0x39 Interrupt Req. Clear bit	0
24	W	Vector No. 0x38 Interrupt Req. Clear bit	0
23	W	Vector No. 0x37 Interrupt Req. Clear bit	0
22	W	Vector No. 0x36 Interrupt Req. Clear bit	0
21	W	Vector No. 0x35 Interrupt Req. Clear bit	0
20	W	Vector No. 0x34 Interrupt Req. Clear bit	0
19	W	Vector No. 0x33 Interrupt Req. Clear bit	0
18	W	Vector No. 0x32 Interrupt Req. Clear bit	0
17	W	Vector No. 0x31 Interrupt Req. Clear bit	0
16	W	Vector No. 0x30 Interrupt Req. Clear bit	0
15	W	Vector No. 0x2F Interrupt Req. Clear bit	0
14	W	Vector No. 0x2E Interrupt Req. Clear bit	0
13	W	Vector No. 0x2D Interrupt Req. Clear bit	0
12	W	Vector No. 0x2C Interrupt Req. Clear bit	0
11	W	Vector No. 0x2B Interrupt Req. Clear bit	0
10	W	Vector No. 0x2A Interrupt Req. Clear bit	0
9	W	Vector No. 0x29 Interrupt Req. Clear bit	0
8	W	Vector No. 0x28 Interrupt Req. Clear bit	0
7	W	Vector No. 0x27 Interrupt Req. Clear bit	0
6	W	Vector No. 0x26 Interrupt Req. Clear bit	0
5	W	Vector No. 0x25 Interrupt Req. Clear bit	0
4	W	Vector No. 0x24 Interrupt Req. Clear bit	0
3	W	Vector No. 0x23 Interrupt Req. Clear bit	0
2	W	Vector No. 0x22 Interrupt Req. Clear bit	0
1	W	Vector No. 0x21 Interrupt Req. Clear bit	0
0	W	Vector No. 0x20 Interrupt Req. Clear bit	0

* Interrupt Request Clear bit
  0 : No Effect Interrupt Mask.
  1 : Pending interrupt is masked from becoming active (interrupts not sent to CPU).

9 CORE TIMER

adStar-L includes 32-bit Core Timer near by MCU.

9.1 Features

- 15-bit Pre-scaler
- 32-bit Timer/Counter
- If CPU in halt(halt3) mode, core timer's counter is stop.
  If CPU resume, counter count continuously.

9.2 15-bit Pre-scaler with clock source selection

Pre-scaler divide the clock 1/2 to 1/32768 times using 15-bit Pre-scaler. And it will be transfer to the Timer / Counter. Timer/Counter select clock which divided by Pre-scaler. And selected clock drive the 32-bit Counter.

If you need exactly phase of divided clock you should reset the Pre-scaler counter using CNTCLR bit in TPCON register.

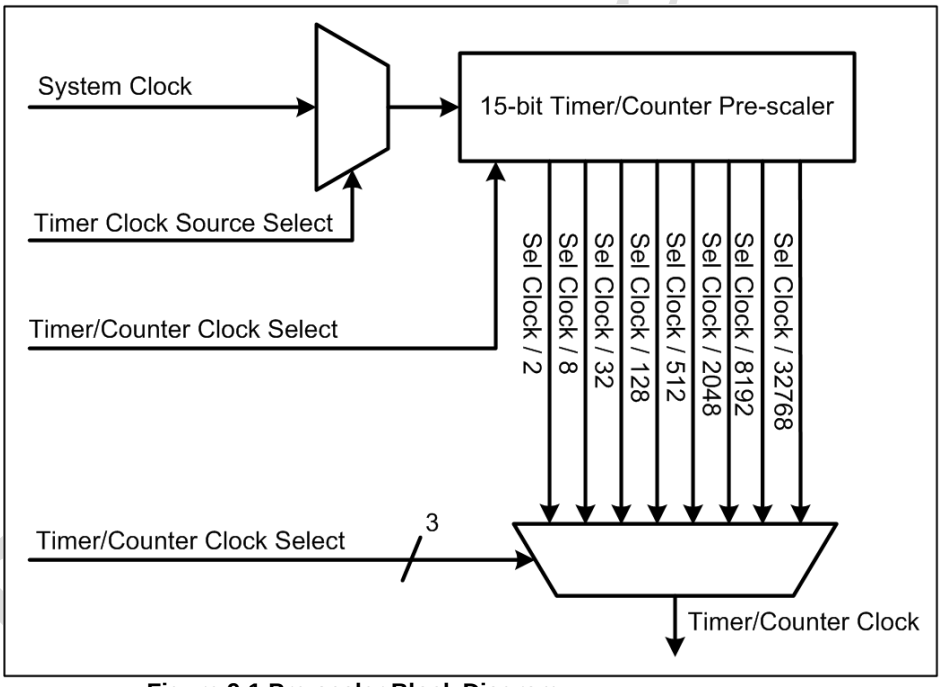


Figure 9-1 Pre-scaler Block Diagram

9.3 Timer/Counter

Timer/Counter used clock which generated by pre-scaler. The value decrease 1 every clock from Timer Counter register value. If the value reach the 0x0 it occured interrupt, and decrease 1 every clock from Timer Counter register value.(Down Counter)

(* TMCNT : Timer counter register value which configured by user)

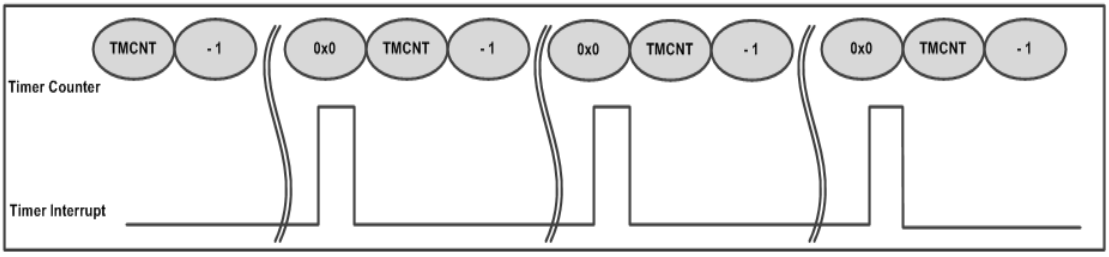


Figure 9-2 Timer Operation

The period of a timer is decided by selected clock, pre-scaler, and timer counter.

$$Timer\ \ Period = \frac{1}{Clock\ \ Source\ \ Frequency} \times \frac{1}{\Pr e - scaler\ \ Factor} \times (TMCNT)\ \ [\sec] \qquad \{\Pr e - scaler\ \ Factor \geq 3\}$$

$$Timer\ \ Period = \frac{1}{Clock\ \ Source\ \ Frequency} \times \frac{1}{\Pr e - scaler\ \ Factor} \times (TMCNT + 1)\ \ [\sec] \qquad \{\Pr e - scaler\ \ Factor < 3\}$$

Timer Period Example :
- Clock Source Frequency : 12MHz System Clock
- Pre-scaler Factor : 1 / 1024
- Timer Counter Value (TMCNT) : 1000

=> 1/12MHz X 1024 X 1000 = 85.333msec = 11.718Hz

Following registers should be configured to run a timer counter.
- TMRST : Pre-scaler clear if necessary.
- TMCON's PFSEL : Determines the clock used in the Time Counter.
- TMCON's TMEN : User have to enable Timer Counter.
- TMCNT : Set timer counter start value.

Following procedure is required to run a Timer Counter.
- Set TMCNT
- Set TMCTRL
- Set CNTCLR bit of TMRST register if necessary.

9.4 Timer Control Registers

9.4.1 Timer Reset Control Register (TMRST)

Address : 0xFFFF_1000

Bit	R/W	Description	Default Value
31 : 2	R	Reserved	-
1	R/W	CNTCLR : Pre-scale Counter and Timer Counter Reset When this bit is “1”, the Timer Pre-scale and Counter will be reset.	0
0	R	Reserved	-

9.4.2 Timer Control Registers (TMCON)

Address : 0xFFFF_1004

Bit	R/W	Description	Default Value
31 : 4	R	Reserved	-
3 : 1	R/W	PFSEL : Pre-scale Factor Selection 000 : clock / 1 001 : clock / 2 010 : clock / 8 011 : clock / 32 100 : clock / 128 101 : clock / 2048 110 : clock / 8192 111 : clock / 32768	111
0	R/W	TMEN : Timer Enable bit 0 : Disable 1 : Enable	0

- If CPU in core break(Core debug) mode, core timer’s counter is stop.
  If CPU resume, counter count continuously.
- If CPU in halt(halt3) mode, core timer’s counter is stop.
  If CPU resume, counter count continuously.

9.4.3 Timer Counter Registers (TMCNT)

Address : 0xFFFF_1008

Bit	R/W	Description	Default Value
31 : 0	R/W	- Write : Timer Counter Value - Read : Current Up-counter Value	0xFFFFFFFFh

9.4.4 Timer Interrupt waveform

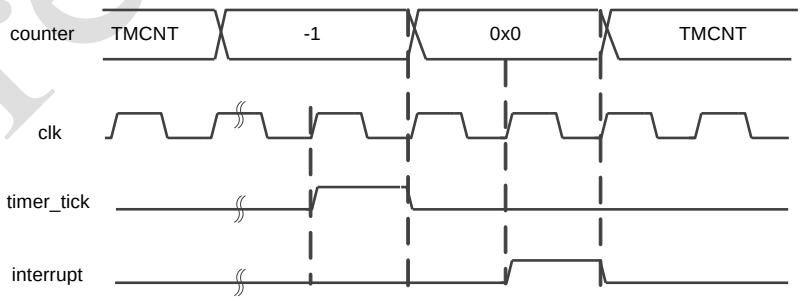


Figure 9-3 core timer interrupt waveform

*** Core timer consist of down counter. The down counting start from configuration value to 0, interrupt occupied like Figure 9-3. After interrupt occupied, counter value set to configured value and counting is begin.

10 WATCHDOG TIMER

The Watchdog Timer is responsible for rollback the system when CPU operates wrong execution due to system errors, device's wrong response, and noise.

If the watchdog time is enabled, the counter value WDTCNT is decreased by 1, and when the value becomes 0, Watchdog Reset is occurred.

If the Watchdog Reset is signaled, the status of the system is stored into WDTST bit.

In order to prevent Watchdog Reset from system under Watchdog Timer enabled, because 32-bit Watchdog Counter value should not be 0, developer should re-configure the WDTCNT.

If WDTMOD bit is set as Interrupt mode, system occurs Interrupt rather Watchdog Reset. In that case, the system informs that WDTCNT value is 0.

Watchdog timer has Lock function. When WDT at Lock state, WDCON value is not changeable and maintain before recorded data. If WDT at unlock state, changed WDCON value is accepted
(UnLock : 0x1ACCE551 write.)

10.1 Register Description

10.1.1 Watchdog Timer Control Register (WDTCTRL)

Address : 0x8002_0000

Bit	*R/W*	*Description*	*Default Value*
31 : 8	R	Reserved	-
7	R/W	HALTEN : Watchdog timer halt enable bit 0: Disable 1: Enable If the core stopped by Halt3, counting is also stopped. (set 1) If the core is active by wakeup the WDT counter resume continuously.	0
6	R/W	BRKEN : Watchdog timer core break enable bit 0: Disable 1: Enable If the core stopped by Debugger, counting is also stopped. (set 1) If the core is active, WDT counter resume continuously.	0
5	R	WDTLOCK : Watchdog timer lock state bit When watchdog timer is Lock, 0 : Lock 1 : Unlock	0
4	R	WDTST : Watchdog timer status bit When watchdog timer is reset mode, 0 : No watchdog reset 1 : Watchdog reset Clear at read	0
3 : 2	R	Reserved	-
1	R/W	WDTMOD : Watchdog timer mode select bit 0 : Reset mode 1 : Interrupt mode	0
0	R/W	WDTEN : Watchdog timer enable bit 0 : Disable 1 : Enable	0

* If WDT at unlock state, user can write the setting value.

10.1.2 Watchdog Timer Counter Value Register (WDTCNT)

Address : 0x8002_0004

Bit	R/W	Description	Default Value
31 : 0	R/W	Watchdog timer counter 32-bit value. Down-counter	0xFFFF_FFFF

* If WDT at unlock state, user can write the setting value.

10.1.3 Watchdog Timer Lock Value Register (WDTLOCK)

Address : 0x8002_0008h

Bit	R/W	Description	Default Value
31 : 0	RW	Watchdog Timer Lock 32-bit Value. (Unlock = 0x1ACCE551) At read is Lock : 0x00000001 Unlock :0x00000000	0x00000000h

10.1.4 Operational Flow Diagrams

* Figure represent the WatchDogTimer flow.
  If user want to set the Watch Dog Timer, user write 0x1ACCE551 at Lock register.
  (Counter value and control registrt setting is available in Unlock state.)

* User can choose reset mode or interrupt mode set by Control register [1]bit.

* Watch Dog Timer consist of down counter. If the count value reached at 0, reset or interrupt is occurred. If the interrupt was occurred, Watch Dog Timer have to maintain the state.
  (Periodical operation is not supported)
* If user want to resume the Watch Dog Timer in interrupt state, user enable the Watch Dog Timer after disable in ISR.

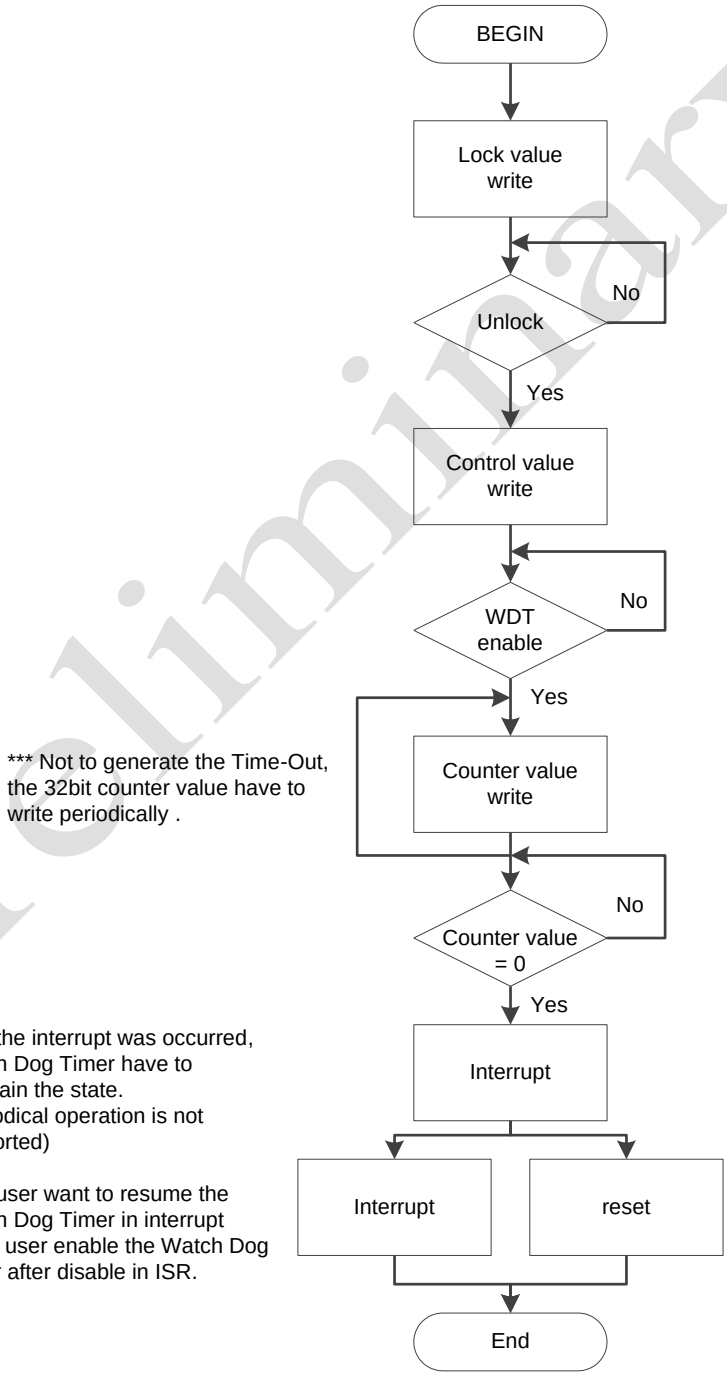


Figure 10-1 Operational flow

11 TIMERS

adStar-L includes 2-channel 32-bit timer/counter which support timer/counter, capture, and PWM functions.

11.1 Features

- 15-bit Pre-scale
- 32-bit Timer/Counter
- 32-bit Capture
- 32-bit PWM
- 32-bit Timer Counter Wave-Out

11.2 Functional Description

11.2.1 15-bit Pre-scaler with clock source selection

Pre-scaler choose an input source between system clock and external clock with CLKSEL bit. It divides the input source by between 2 and 32768, and transfers the divided clock to timer/counter. Timer/counter receives the divided clock, and runs 32bit counter.

When precise phase of the divided clock is needed, pre-scaler counter should be initilaized by setting CNTCLR bit of TPxCTRL register.

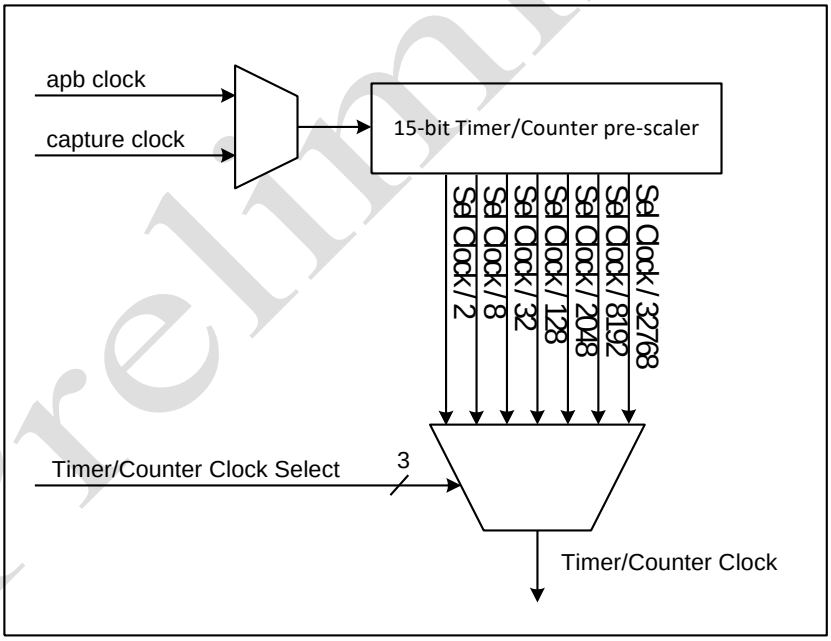


Figure 11-1 Pre-scaler Block Diagram

11.2.2 Timer/Counter

On every cycle of divided clock from pre-scaler, counter value is increment by one from 0x0 until it reaches the user-difined timer counter register value. When reached, the counter value is reset(=0) and interrupt raises.

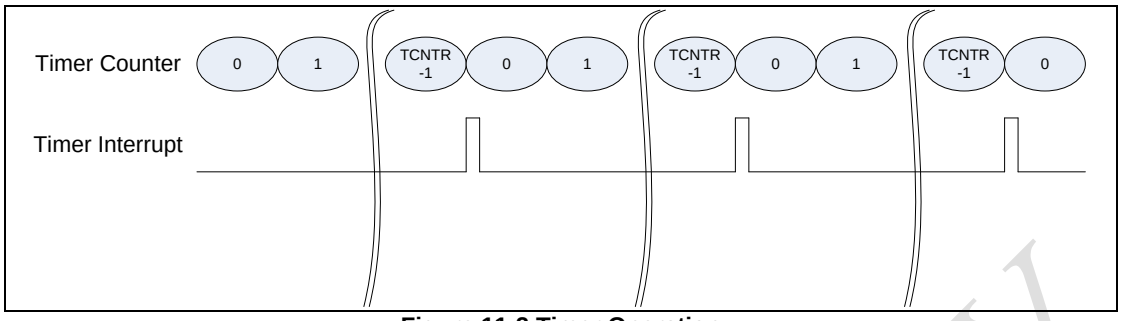


Figure 11-2 Timer Operation

*** TCNTR = Timer Counter Read.

The period of a timer is decided by selected clock, pre-scaler, and timer counter.

$$Timer\ \ Period = \frac{1}{Clock\ \ Source\ \ Frequency} \times \frac{1}{\Pr e - scaler\ \ Factor} \times (TMCNT)\ \ [\sec] \qquad \{\Pr e - scaler\ \ Factor \geq 3\}$$

$$Timer\ \ Period = \frac{1}{Clock\ \ Source\ \ Frequency} \times \frac{1}{\Pr e - scaler\ \ Factor} \times (TMCNT + 1)\ \ [\sec] \qquad \{\Pr e - scaler\ \ Factor < 3\}$$

Timer Period Example :
- Clock Source Frequency : 12MHz System Clock
- Pre-scaler Factor : 1 / 1024
- Timer Counter Value (TMCNT) : 1000

=> 1/12MHz X 1024 X 1000 = 85.333msec = 11.718Hz

Following registers should be configured to run a timer counter.
- TPxCTRL : decide the clock input of pre-scaler. Also, it is used to clear pre-scaler.
- TMxCTRL's TMOD : decides the mode of Timer Counter
- TMxCTRL's WAVE: decide whether output or not the clock of timer counter period.
- TMxCTRL's PFSEL: decide the clock to be used for Timer Counter
- TMxCTRL's TMEN: Enable Timer Counter
- TMxCNT: Decide the maximum counter value of Timer Counter

Following procedure is required to run a Timer Counter.
- Set TPxCTRL
- Set TMxCNT
- Set TMxCTRL
- Set CNTCLR bit of TPxCTRL register if necessary

11.2.3 Pulse Width Modulation (PWM)

PWM is a controller to output pulse signals of programmer-defined duty and period.

PWM references clock generated by pre-scaler, and outputs the wave form of user defined period.

PWM output pulse is toggled whenever its 32bit counter value reaches PWM duty or PWM period register value. The number of outputs is limited by PWM pulse number register. When it reaches the limit, PWM interrupt raises. However, if there is no special hanldler for the interrupt, PWM will output continuously. Thus, timer interrupt should disable PWM to stop PWM pulse.

$$PWM\ \ Pulse\ \ Period = \frac{1}{Clock\ \ Source\ \ Frequency} \times \frac{1}{\Pr e - scaler\ \ Factor} \times (TMCNT)\ [\sec] \qquad \{\Pr e - scaler\ \ Factor \geq 3\}$$

$$PWM\ \ Pulse\ \ Period = \frac{1}{Clock\ \ Source\ \ Frequency} \times \frac{1}{\Pr e - scaler\ \ Factor} \times (TMCNT + 1)\ [\sec] \qquad \{\Pr e - scaler\ \ Factor < 3\}$$

PWM Period Example :
- Clock Source Frequency : 12MHz System Clock
- Pre-scaler Factor : 1 / 1024
- PWM Period Value(TMxCNT) : 10
- PWM Duty Value : 6

=> 1/12MHz X 1024 X 10 = 0.853msec = 1.171KHz

Following registers should be configured to run PWM.
- TPxCTRL: choose clock input of pre-scaler. Also, it can be used to clear pre-scaler.
- TMxCTRL's TMOD: decide PWM mode
- TMxCTRL's PWML: decide start level of PWM output
- TMxCTRL's PFSEL: decide clock of PWM
- TMxCTRL's TMEN: enable PWM
- TMxCNT: decide the period of PWM
- TMxDUT: decide the duty of PWM
- TMxPUL: decide the number of pulse outputs of PWM. If it reaches it limit, timer interrupt raises. However, it doesn't stop PWM pulse output.

Following procedure is required to run PWM.
- Set TPxCTRL
- Set TMxCNT
- Set TMxDUT
- Set TMxPUL
- Set CNTCLR of TPxCTRL register if necessary

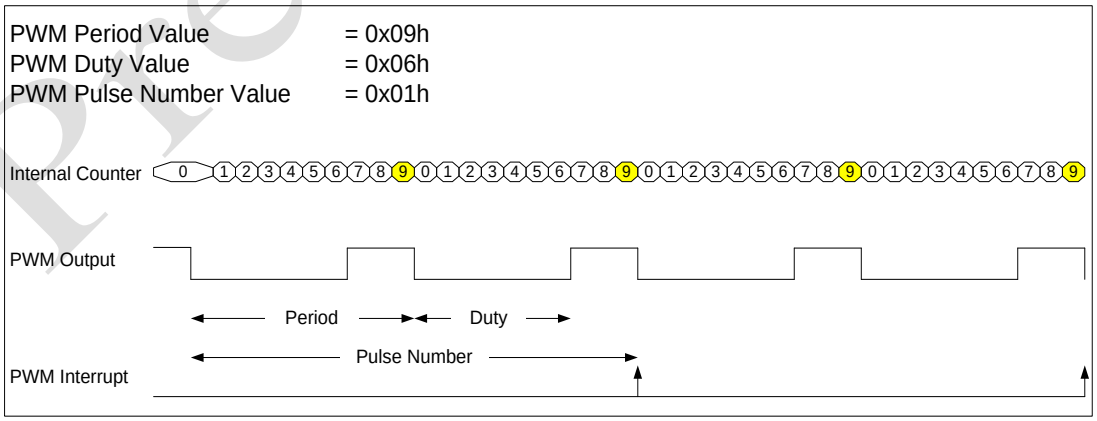


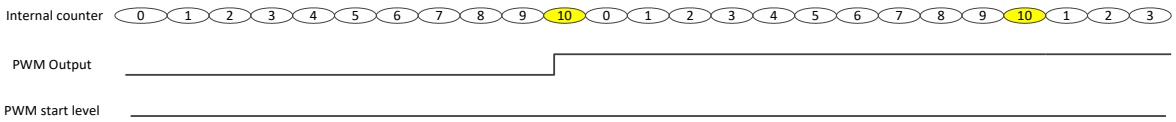
Figure 11-3 PWM Operation

**** Special Case**

If user configure Duty 100% or 0%, output of PWM wave as follow.

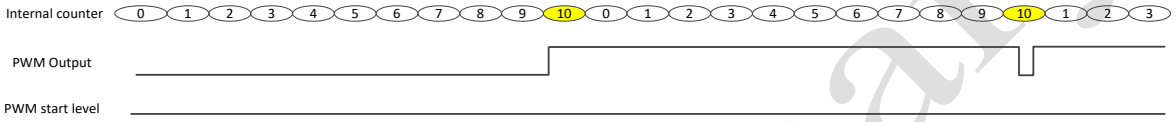
* period 100% ,Duty 100% ,start level = low

PWM period value = 0x10h
PWM Duty Value = 0x10h
PWM start level = LOW



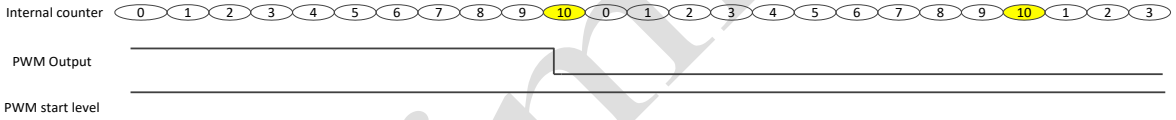
* period 100% ,Duty 0% ,start level = low

PWM period value = 0x10h
PWM Duty Value = 0x00h
PWM start level = LOW



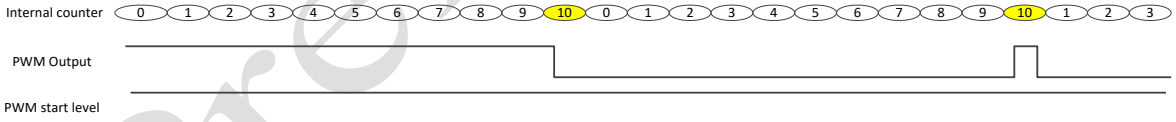
* period 100% ,Duty 100% ,start level = high

PWM period value = 0x10h
PWM Duty Value = 0x10h
PWM start level = HIGH



* period 100% ,Duty 0% ,start level = high

PWM period value = 0x10h
PWM Duty Value = 0x00h
PWM start level = HIGH



11.2.4 Capture

Capture function measures the external output referencing the clock defined by pre-scaler.

Five kind of external periods can be measured: Low/High pulse, Low Pulse, High Pulse, Falling to Falling Period, Rising to Rising Period.

The first capture after enabling timer should be ignored because it is a transient value.

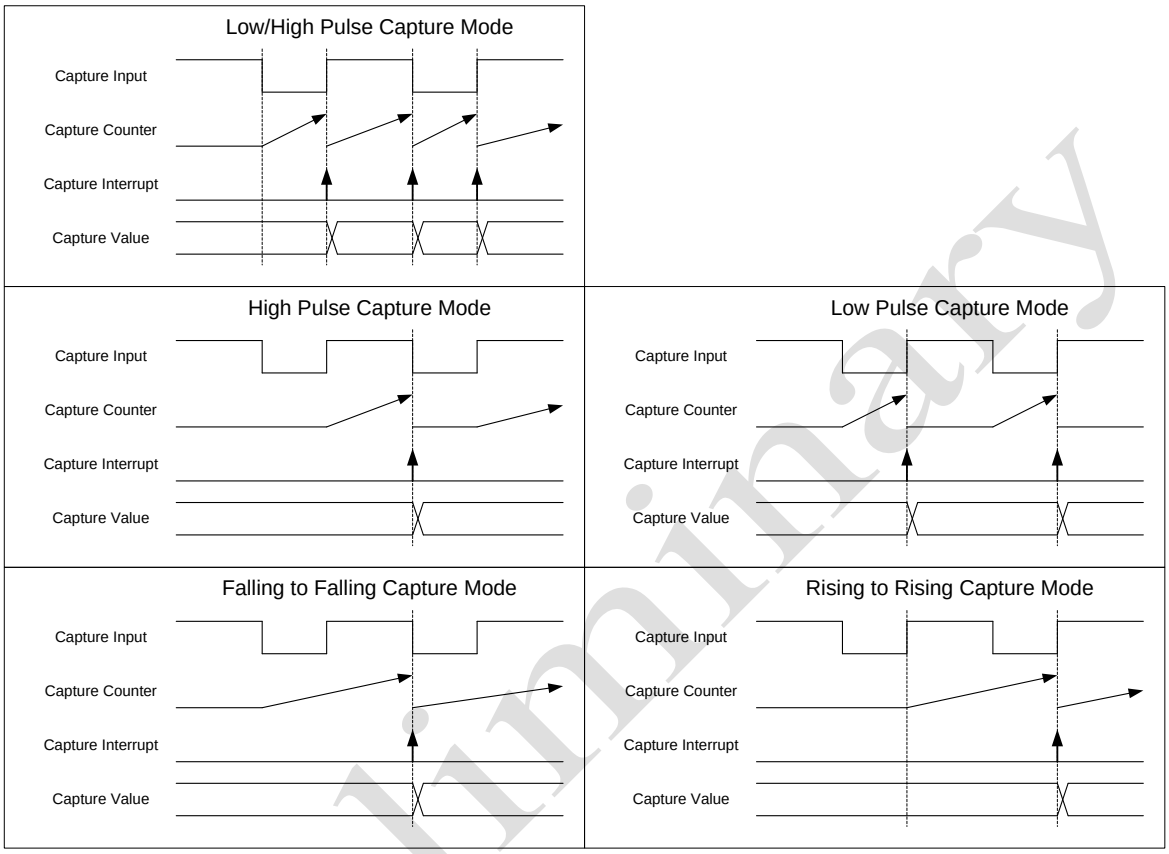


Figure 11-4 Capture Mode Operation

Calculating the period of captured pulses follows the below euqation.

$$Capture\ \ Signal\ \ Width\ \ Time = \frac{1}{Clock\ \ Source\ \ Frequency} \times \frac{1}{\Pr e - scaler\ \ Factor} \times (OCA + 1)\ \ [\sec]$$

Capture Time Example :
- Clock Source Frequency : 12MHz System Clock
- Pre-scaler Factor : 1 / 1024
- Capture Value : 9

=> 1/12MHz X 1024 X 10 = 0.853msec

To run in capture mode, following registers should be configured.

- TPxCTRL: choose the clock input of pre-scaler. Also, can clear pre-scaler
- TMxCTRL's TMOD: Change into capture mode
- TMxCTRL's CAPMOD: decide the mode of pulse capturing
- TMxCTRL's PFSEL: choose the clock for capturing
- TMxCTRL's TMEN: enable capturing

Following procedure is required to run capturing.

- Set TPxCTRL
- Set TMxCTRL
- Set the CNTCLR bit of TPxCTRL register if necessary
- Check the period of capturing by reading TMxDUT
- Check overflow by reading OVST of TMxCTRL register

11.3 Register Description

11.3.1 Timer Pre-scale Control Registers (TPxCTRL)

Address : 0x8002_0400 / 0x8002_0420

Bit	R/W	Description	Default Value
31 : 2	R	Reserved	-
1	R/W	CNTCLR : Pre-scale Counter and Timer Counter Reset When this bit is “1”, the Timer Pre-scale and Counter will be reset.	0
0	R/W	CLKSEL : Pre-scale Clock Selection 0 : apb clock 1 : CAPx	0

* Each Timer channel has a CAPx.

11.3.2 Timer Control Registers (TMxCTRL)

Address : 0x8002_0404 / 0x8002_0424

Bit	R/W	Description	Default Value
31 : 19	R	Reserved	-
18	R/W	HALTEN : Core Halt Enable bit 0: Disable 1: Enable If the core stopped by Halt3, counting is also stopped. (set 1) If the core is active by wakeup the WDT counter resume continuously.	0
17	R/W	BRKEN : Core Break Enable bit 0: Disable 1: Enable If the core stopped by Debugger, counting is also stopped. (set 1) If the core is active, WDT counter resume continuously.	0
16	R/W	DMAREQEN : Timer request(DMA) Enable bit 0: Timer request only interrupt every configured cycle. 1: If Timer occured every configured cycle, DMA request the ‘request signal’.	0
15 : 14	R/W	TMOD : Timer/Counter Mode 00 : Timer 01 : PWM 1x : Capture	00
13	R	Reserved	-
12	R	OVST : Capture Overflow Status bit If user read this bit, Overflow status bit will be cleared.	0
11	R	Reserved	0
10 : 8	R/W	CAPMOD : Capture Mode Selection 00x : Low/High Pulse Capture mode 010 : Low Pulse Capture mode 011 : High Pulse Capture mode 10x : Failing to Failing Period Capture mode 11x : Rising to Rising Period Capture mode	000
7	R/W	IUE : Immediately Update Enable 0: If user write data at Counter Register, it applied end of previously set Period. 1: If user write data at Counter Register, it applied immediately.	1
6	R/W	PWMO : PWM Output One Period Generation 0 : Disable 1 : Enable	0
5	R/W	PWML : PWM Output Start Level 0 : Start Level is Low 1 : Start Level is High	0
4	R/W	TMOUT : Timer Wave Output Generation 0 : Disable 1 : Enable	0
3 : 1	R/W	PFSEL : Pre-scale Factor Selection 000 : 1/2 001 : 1/8 010 : 1/32 011 : 1/128 100 : 1/512 101 : 1/2048 110 : 1/8192 111 : 1/32768	111
0	R/W	TMEN : Timer/Counter or PWM Enable 0 : Disable 1 : Enable	0

* PWM Output One Period Generation: Decide the number of period to be generated in PWM mode. After the number, PWM is automatically disabled.
* Timer Wave Output Generation: Decide whether output or not the toggled wave form on every period in Timer mode.
* Immediately Update : If user configure initial Timer counter value, IUE bit must be set 1.

11.3.3 Timer Counter / PWM Period Registers (TMxCNT)

Address : 0x8002_0408 / 0x8002_0428

Bit	R/W	Description	Default Value
31 : 0	R/W	(Timer mode) - Write : Timer Counter Value - Read : Current Up-counter Value (PWM mode) - Read/Write : PWM Period Value	0xFFFFFFFF

11.3.4 Capture Counter Registers / PWM Duty Registers (TMxDUT)

Address : 0x8002_040C / 0x8002_042C

Bit	R/W	Description	Default Value
31 : 0	R/W	(Capture mode) - Read : Result value of counting at the sampling period (PWM mode) - Read/Write : PWM Duty Value	0xFFFFFFFF

* PWM Duty : First Halt Duty of PWM Pulse

11.3.5 PWM Pulse Count Registers (TMxPUL)

Address : 0x8002_0410 / 0x8002_0430

Bit	R/W	Description	Default Value
31 : 0	R/W	(PWM mode) - Read/Write : PWM Pulse Number Value	0xFFFFFFFF

12 REAL TIMER CLOCK

adStar-L RTC operates on a separate power supply. User can configure year, month, day, hour, minute, second register using 32.768kHz clock. And user can read current clock. RTC interrupt can configure 1/4s,1/2s, 1s, 2s, 4s, 1m, 2m, 4m, 1h, 2h, 4h, 24h unit. RTC alarm can configure second, minute, hour, day, month unit.

12.1 RTC Features

- Independent power
- Leap support
- Periodic interrupt generation: 1/4s ~ 24h
- Alarm support (second, minute, hour, day, month)
- Compensation available for Crystal error. (calibration mode support)

When user supply 3V at RTC_VDD and 32.768kHz clock at RTC_XIN, RTC begin at 2004.01.01.

※RTC calibration
Calibration mode is existed at RTC. It compensated Crystal error maximum 1day per ±1sec.

- If user want to detect error of 32.768kHz Crystal, user must use another timer resource. If user detected error, user have to configure sub_mode, pul_mode after calibration mode enable state. Calibration compare value is only available in calibration mode.

12.2 RTC diagram

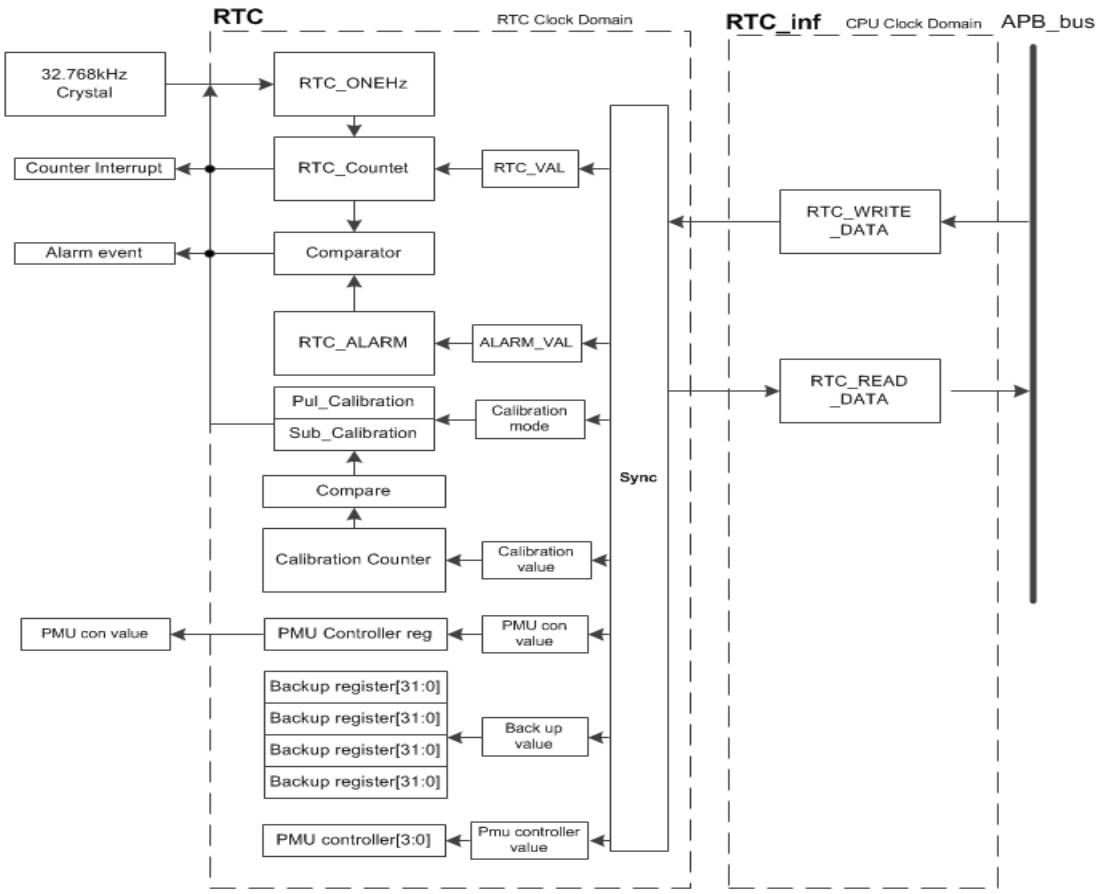


Figure 12-1 RTC Block Diagram

12.3 RTC Calibration (function diagram)

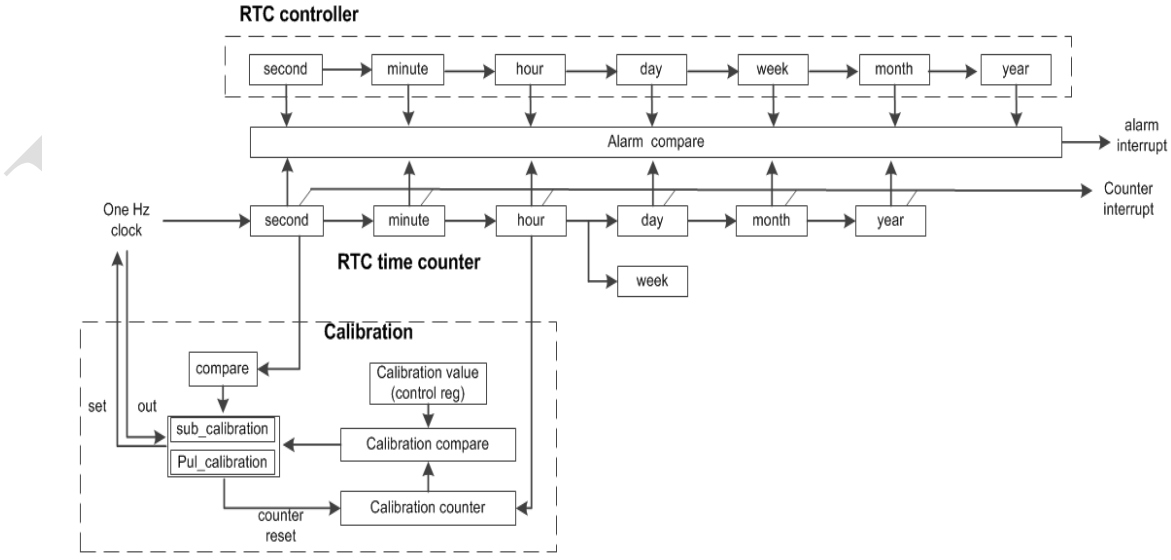


Figure 12-2 Calibration Function Diagram

12.4 Real Time Counter Control Register

12.4.1 Real Time Counter Control Register (RTCCON_1)

Address : 8002_3800h

Bit	R/W	Description	Default Value
7	RW	RTC Calibration Subtraction. 0 : Disable 1 : Calibration Plus If Crystal is faster than existed time. (It compensated 1day per -1sec.)	0
6	RW	RTC Calibration Puls. 0 : Disable 1 :Calibration Subtraction If Crystal is slower than existed time. (It compensated 1day per +1sec.)	0
5	RW	RTC Calibration Mode. 0 : Disable 1 : Calibration Mode If user in Calibration mode, It compensated Crystal error	0
4	RW	Test Mode 0 : Normal Mode 1 : RTC Test Mode(Fast)	0
3 : 0	RW	RTC Interrupt Select 0000 : No Interrupt 0001 : Alarm Interrupt 0010 : 1/4 Sec Period 0011 : 1/2 Sec Period 0100 : 1 Sec Period 0101 : 2 Sec Period 0110 : 4 Sec Period 0111 : Reserved 1000 : 1 Min Period 1001 : 2 Min Period 1010 : 4 Min Period 1011 : Reserved 1100 : 1 Hour Period 1101 : 2 Hour Period 1110 : 4 Hour Period 1111 : 24 Hour Period	0000

* If user want to compensate Crystal error, user have to enable Calibration Mode Bit

12.4.2 Real Time Counter Control Register (RTCCON_2)

Address : 8002_3804h

Bit	R/W	Description	Default Value
7:6	R	Reserved	-
5	R	RTC alarm interrupt state bit This bit is cleared by PMUCON read. 0 : no interrupt 1 : alarm interrupt Occurs.	0
4	R	RTC interrupt state bit. This bit is cleared by PMUCON read. 0 : no interrupt 1 : interrupt Occurs.	0
3:0	RW	RTC Calibration compare value(Base 1 day) 0001 : 1sec , 0010 : 0.5sec , 0011 : 0.33sec , 0100 : 0.25sec , 0101 : 0.2sec , 0110 : 0.16sec , 0111 : 0.14sec , 1000 : 0.12sec, 1001 : 0.11sec , 1010 : 0.1sec , 1011 : 0..09sec , 1100 : 0.08sec , 1101 : 0.076sec , 1110 : 0.071sec, 1111 : 0.06sec, User can choose Crystal error correction value. During 1day per 0.06sec to 1 sec Correction.	0001 (1 day 1sec Correction)

* This register determine how much times to correct in Calibration Mode
(Default value is 1 day per 1sec compensation)

12.5 Real Time Counter Register

12.5.1 Real Time Counter Sec Register (RSEC)

Address : 8002_3808h

Bit	R/W	Description	Default Value
7 : 6	R	Reserved	-
5 : 0	RW	Sec (0~59)	000000

12.5.2 Real Time Counter Min Register (RMIN)

Address : 8002_380Ch

Bit	R/W	Description	Default Value
7 : 6	R	Reserved	-
5 : 0	RW	Min (0~59)	000000

12.5.3 Real Time Counter Hour Register (RHOUR)

Address : 8002_3810h

Bit	R/W	Description	Default Value
7 : 5	R	Reserved	-
4 : 0	RW	Hour (0~23)	00000

12.5.4 Real Time Counter Day Register (RDAY)

Address : 8002_3814h

Bit	R/W	Description	Default Value
7 : 5	R	Reserved	-
4 : 0	RW	Day (1~31)	00001

12.5.5 Real Time Counter Week Register (RWEEK)

Address : 8002_3818h

Bit	R/W	Description	Default Value
7 : 3	R	Reserved	-
2 : 0	RW	Week (0~6)	100

12.5.6 Real Time Counter Week Register (RMONTH)

Address : 8002_381Ch

Bit	R/W	Description	Default Value
7 : 4	R	Reserved	-
3 : 0	RW	Month (0~11)	0001

12.5.7 Real Time Counter Year Register (RYEAR)

Address : 8002_3820h

Bit	R/W	Description	Default Value
7	R	Reserved	-
6 : 0	RW	Year (0~99)	0000100

12.6 Real Time Alarm Register

12.6.1 Real Time Alarm Register (RALM_S)

Address : 8002_3824h

Bit	R/W	Description	Default Value
7 : 6	R	Reserved	-
5 : 0	RW	Sec(0~59)	0

12.6.2 Real Time Alarm Register (RALM_M)

Address : 8002_3828h

Bit	R/W	Description	Default Value
7 : 6	R	Reserved	-
5 : 0	RW	Min(0~59)	0

12.6.3 Real Time Alarm Register (RALM_H)

Address : 8002_382Ch

Bit	R/W	Description	Default Value
7 : 5	R	Reserved	-
4 : 0	RW	Hour(0~23)	0

12.6.4 Real Time Alarm Register (RALM_D)

Address : 8002_3830h

Bit	R/W	Description	Default Value
7 : 5	R	Reserved	-
4 : 0	RW	Day(1~31)	0

12.6.5 Real Time Alarm Register (RALM_MO)

Address : 8002_3834h

Bit	R/W	Description	Default Value
7 : 4	R	Reserved	-
3 : 0	RW	Month(0~11)	0

* RTC alarm have to configure month, day, hour, minute, second.

12.7 Real Time Back up Register

12.7.1 Real Time Back up Register (BACKUP0_0)

Address : 8002_3840h

Bit	R/W	Description	Default Value
7 : 0	RW	Back up data0_0	-

12.7.2 Real Time Back up Register (BACKUP0_1)

Address : 8002_3844h

Bit	R/W	Description	Default Value
7 : 0	RW	Back up data0_1	-

12.7.3 Real Time Back up Register (BACKUP0_2)

Address : 8002_3848h

Bit	R/W	Description	Default Value
7 : 0	RW	Back up data0_2	-

12.7.4 Real Time Back up Register (BACKUP0_3)

Address : 8002_384Ch

Bit	R/W	Description	Default Value
7 : 0	RW	Back up data0_3	-

12.7.5 Real Time Back up Register (BACKUP1_0)

Address : 8002_3850h

Bit	R/W	Description	Default Value
7 : 0	RW	Back up data1_0	-

12.7.6 Real Time Back up Register (BACKUP1_1)

Address : 8002_3854h

Bit	R/W	Description	Default Value
7 : 0	RW	Back up data1_1	-

12.7.7 Real Time Back up Register (BACKUP1_2)

Address : 8002_3858h

Bit	R/W	Description	Default Value
7 : 0	RW	Back up data1_2	-

12.7.8 Real Time Back up Register (BACKUP1_3)

Address : 8002_385Ch

Bit	R/W	Description	Default Value
7 : 0	RW	Back up data1_3	-

12.7.9 Real Time Back up Register (BACKUP2_0)

Address : 8002_3860h

Bit	R/W	Description	Default Value
7 : 0	RW	Back up data2_0	-

12.7.10 Real Time Back up Register (BACKUP2_1)

Address : 8002_3864h

Bit	R/W	Description	Default Value
7 : 0	RW	Back up data2_1	-

12.7.11 Real Time Back up Register (BACKUP2_2)

Address : 8002_3868h

Bit	R/W	Description	Default Value
7 : 0	RW	Back up data2_2	-

12.7.12 Real Time Back up Register (BACKUP2_3)

Address : 8002_386Ch

Bit	R/W	Description	Default Value
7 : 0	RW	Back up data2_3	-

12.7.13 Real Time Back up Register (BACKUP3_0)

Address : 8002_3870h

Bit	R/W	Description	Default Value
7 : 0	RW	Back up data3_0	-

12.7.14 Real Time Back up Register (BACKUP3_1)

Address : 8002_3874h

Bit	R/W	Description	Default Value
7 : 0	RW	Back up data3_1	-

12.7.15 Real Time Back up Register (BACKUP3_2)

Address : 8002_3878h

Bit	R/W	Description	Default Value
7 : 0	RW	Back up data3_2	-

12.7.16 Real Time Back up Register (BACKUP3_3)

Address : 8002_387Ch

Bit	R/W	Description	Default Value
7 : 0	RW	Back up data3_3	-

12.8 Real Time PMU Controller Register (PMUCON)

Address : 8002_3880h

Bit	*R/W*	*Description*	*Default Value*
7:4	R	Reserved	-
3	R/W	Halt1 state bit 1 : power down signal occur Clear Halt1 state bit When user write 1 it will be cleared. then it turns 0 automatically	0
2	R/W	Halt0 state bit 1 : osc disable signal occur Clear Halt0 state bit When user write 1 it will be cleared. then it turns 0 automatically	0
1	R/W	Wakeup latch output signal select 0 : f/f output 1 : latch output	0
0	R/W	RTC wakeup state bit state clear 0: release 1: clear	0

* RTC consist of RTC macro block using 32kHz clock and RTC interface block using CPU clock. User have to check the update bit for the RTC clock sync, and then user can write or read data.

Ex)

```
RTCCON = 0x77;              // First data (w/r)
while (RTCCON & 0x100);     // Update bit occur
RTCCON_1 = 0x01;            // Second data (w/r)
while (RTCCON & 0x100);     // Update bit occur
```

12.9 RTC interrupt timing diagram

* RTC consist of two type of interrupt. One is alarm interrupt the other is periodically occur interrupt.

* Configure alarm interrupt using Control register[3:0], and then alarm register write, it generate interrupt on desired time. (Refer to Figure 12-3)

* Periodical interrupt occur 1cycle interrupt, except 1/4 and 1/2 interrupt.
(Refer to Figure 12-4, Figure 12-5, Figure 12-6)

12.9.1 Alarm interrupt operation

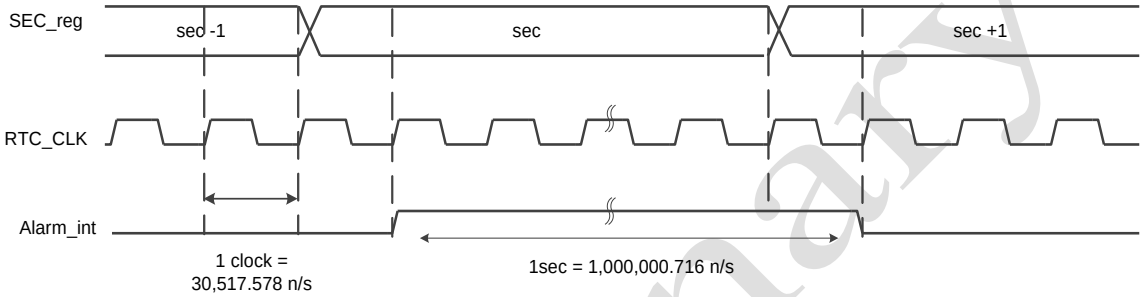


Figure 12-3 Alarm Interrupt Operation

12.9.2 1sec interrupt operation

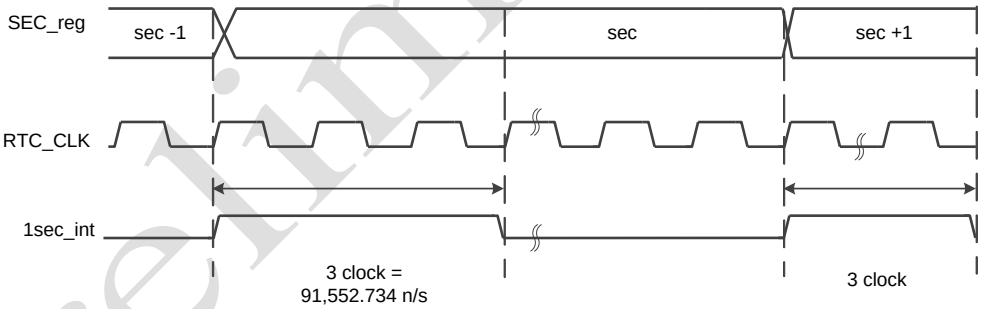


Figure 12-4 1sec Interrupt Operation

12.9.3 1/2 interrupt operation

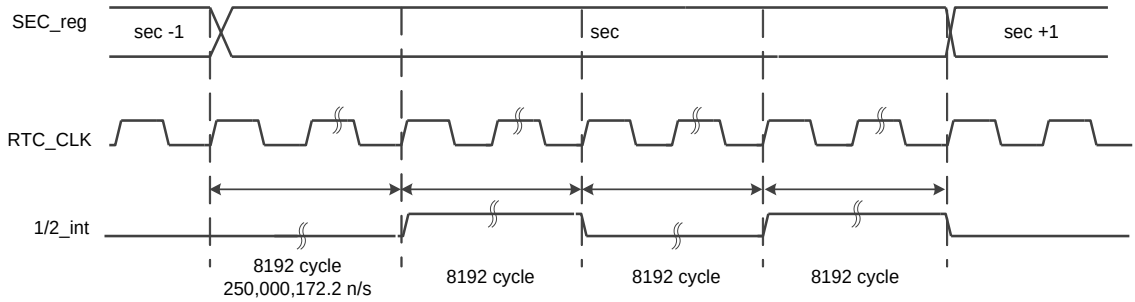


Figure 12-5 1/2 Interrupt Operation

12.9.4 1/4 interrupt operation

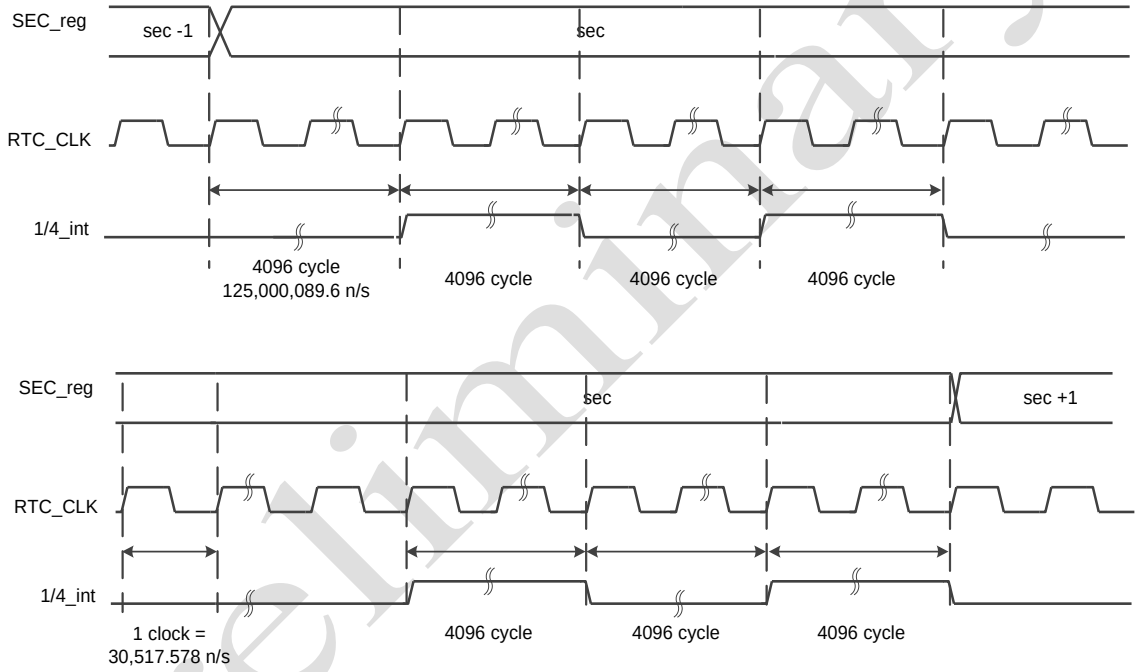


Figure 12-6 1/4 Interrupt Operation

13 COPROCESSOR

Coprocessor of *adstar-L* includes Memory Management Unit (MMU) and I-Cache, D-Cache functional blocks. It controls the functional blocks and additional blocks.

13.1 Features

- Memory Management Unit
  - Real Memory mode
- 2 Way Set Associative Harvard Cache
  - 8KBytes I-Cache
  - 8KBytes D-Cache
  - Write Through
  - 16 Bytes / Line
  - LRU Replacement
  - Cache Invalidation by Software
- 4 Words Deep Write Buffer (FIFO)

With the Real Memory mode, CPU can access reserved portion of memory space for 4GB linear memory space. The accessing address of CPU exactly matches with physical memory address.

Table 13-1 Real Memory map

Address Range	*Sector Number*	*Size*
0x0000_0000~0x000F_FFFF (Memory Bank0)	Flash	512KBytes
0x1000_0000~0x1000_07FF (Memory Bank0)	Internal SRAM for Instruction	2KBytes
0x1800_0000~0x1800_77FF (Memory Bank1)	Internal SRAM for Data	30KBytes
0x2000_0000 ~ 0x2FFF_FFFF	SDRAM	8 or 16Mbytes
0x5000_0000 ~ 0x5FFF_FFFF	External SRAM	-

13.2 Coprocessor Description

Table 13-2 Coprocessor Register Description

Register	*R/W*	*Description*
SCPR15	R	System Coprocessor Status Register
	W	Master Command Register
SCPR14	R/W	Supervisor Stack Point Register
SCPR13	R/W	User Stack Pointer
SCPR12	R/W	Vector Base Register
SCPR11	W	Invalidate Cache Line and Lock Register
SCPR10	-	Reserved
SCPR9	R/W	Memory Bank Configuration Register
SCPR8	R/W	Sub-Bank Configuration Register
SCPR7	R/W	Reserved
SCPR6	R/W	Reserved
SCPR5	R/W	Sub-Bank Address Register
SCPR4	R/W	General Access Point Data Register
SCPR3	R/W	General Access Point Index Register
SCPR2	R/W	Reserved
SCPR1	R/W	Reserved
SCPR0	R/W	Reserved

13.3 Coprocessor Control Registers

13.3.1 System Coprocessor Status Register (SCPR15)

Bit	R/W	Description	Default Value
31	R	System Co-Processor Access Right (Privileged) Coprocessor appear access permission 0 : Supervisor/User Accessible 1 : Supervisor Access only	1
30 : 28	R	Coprocessor Type	001
27 : 25	R	Coprocessor Subtype	000
24 : 19	R	Reserved	-
18	R	L1 Cache Presented 0 : Presented 1 : Not Presented	0
17	R	L1 Cache Snooping Capability 0 : Support Snooping 1 : Not support Snooping	1
16 : 7	R	Reserved	-
6	R	Misalign Correction Support for Data Access 0 : Not support Misalign Correction 1 : Support Misalign Correction	0
5 : 2	R	SCP Rending Exception Number 0000 : Inst. Fetch - Access Violation 0010 : Privilege Violation Exception 0011 : Data Access - Address Misalignment 0100 : Data Access – Access Violation 1000 : Inst. Fetch - Address Misalignment 1111 : N/A	1111
1	R	SCP Pending Exception status 0 : No Pending Exception 1 : Pending Exception Exist	0
0	R	Reserved	-

13.3.2 Master Command Register (SCPR15)

Bit	R/W	Description	Default Value
31 : 6	W	Reserved	-
5 : 2	W	End of Exception 0000 : Inst. Fetch - Access Violation 0010 : Privilege Violation Exception 0011 : Data Access - Address Misalignment 0100 : Data Access – Access Violation 1000 : Inst. Fetch - Address Misalignment 1111 : Privilege Violation Exception	1111
1 : 0	W	Reserved	-

13.3.3 Supervisor Stack Point Register (SCPR14)

Bit	R/W	Description	Default Value
31 : 2	R/W	Supervisor Stack Pointer	0x0000_0000
1 : 0	R/W	Always 0	00

13.3.4 User Stack Point Register (SCPR13)

Bit	R/W	Description	Default Value
31 : 2	R/W	User Stack Pointer	0x0000_0000
1 : 0	R/W	Always 0	00

13.3.5 Vector Base Register (SCPR12)

Bit	R/W	Description	Default Value
31 : 2	R/W	Vector Base for Exception	0x0000_0000
1 : 0	R/W	Always 0	00

13.3.6 Invalidate Cache Line and Lock Register (SCPR11)

Bit	R/W	Description	Default Value
31 : 7	W	Invalidation Target Address/Way	-
6 : 4	W	Invalidation Target Address/Way	-
3	W	Invalidation Mode 0 : Address Based Invalidation 1 : Way Based Invalidation	-
2	W	Copy-back Selection in Invalidation 0 : Invalidation without Copy-back 1 : Invalidation with Copy-back if need	-
1	W	Cache Line Locking in Invalidation 0 : Invalidation without Locking 1 : Invalidation with Locking	-
0	W	Cache Type in Invalidation 0 : I-Cache 1 : D-Cache	-

13.3.7 Memory Bank Configuration Register (SCPR9)

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	0
15	R/W	Always 0	0
14	R/W	Memory Bank 3 Access Right 0 : Supervisor only Accessible 1 : Supervisor/User Accessible	0
13 : 12	R/W	Memory Bank 3 Cache Configuration 00 : Disable Cache 01 : Reserved 10 : Enable Cache with Write-through 11 : N/A	00
11	R/W	Always 0	0
10	R/W	Memory Bank 2 Access Right 0 : Supervisor only Accessible 1 : Supervisor/User Accessible	0
9 : 8	R/W	Memory Bank 2 Cache Configuration 00 : Disable Cache 01 : Reserved 10 : Enable Cache with Write-through 11 : N/A	00
7	R/W	Always 0	0
6	R/W	Memory Bank 1 Access Right 0 : Supervisor only Accessible 1 : Supervisor/User Accessible	0
5 : 4	R/W	Memory Bank 1 Cache Configuration 00 : Disable Cache 01 : Reserved 10 : Enable Cache with Write-through 11 : N/A	00
3	R/W	Always 0	0
2	R/W	Memory Bank 0 Access Right 0 : Supervisor only Accessible 1 : Supervisor/User Accessible	0
1 : 0	R/W	Memory Bank 0 Cache Configuration 00 : Disable Cache 01 : Reserved 10 : Enable Cache with Write-through 11 : N/A	00

13.3.8 General Access Point Data Register (SCPR4)

Bit	R/W	Description	Default Value
31 : 0	R/W	General Access Point Data Register value that is configured at SCPR3	0x0000_0000

13.3.9 General Access Point Index Register (SCPR3)

Bit	R/W	Description	Default Value
31 : 0	R/W	General Access Point Index - Core Debugging Information 0x0000_0000 : Backup IR 0x0000_0001 : Backup ER 0x0000_0002 : Backup PC 0x0000_0010 : Backup EAD - System Coprocessor Debugging Information 0x0000_0303 : Inst. Bus Error Address 0x0000_0304 : Data Bus Error Address - Cache Lock Information 0x0000_0500 : Inst. Lock Condition 0x0000_0501 : Data Lock Condition - Memory Bank Management Information 0x0000_0600 : Inst. MBMB Violation Address 0x0000_0601 : Data MBMB Violation Address - Internal SRAM Configuration Information 0x0000_0700 : Global Control Reg. Address Local Control Registers 0x0000_0701 : Local I-Control Reg.0 Address 0x0000_0711 : Local I-Control Reg.1 Address 0x0000_0721 : Local I-Control Reg.2 Address 0x0000_0731 : Local I-Control Reg.3 Address 0x0000_0704 : Local D-Control Reg.0 Address 0x0000_0714 : Local D-Control Reg.1 Address 0x0000_0724 : Local D-Control Reg.2 Address 0x0000_0734 : Local D-Control Reg.3 Address Local Start Address Registers 0x0000_0702 : Local I-Start Reg.0 Address 0x0000_0712 : Local I-Start Reg.1 Address 0x0000_0722 : Local I-Start Reg.2 Address 0x0000_0732 : Local I-Start Reg.3 Address 0x0000_0705 : Local D-Start Reg.0 Address 0x0000_0715 : Local D-Start Reg.1 Address 0x0000_0725 : Local D-Start Reg.2 Address 0x0000_0735 : Local D-Start Reg.3 Address Local End Address Registers 0x0000_0703 : Local I-End Reg.0 Address 0x0000_0713 : Local I-End Reg.1 Address 0x0000_0723 : Local I-End Reg.2 Address 0x0000_0733 : Local I-End Reg.3 Address 0x0000_0706 : Local D-End Reg.0 Address 0x0000_0716 : Local D-End Reg.1 Address 0x0000_0726 : Local D-End Reg.2 Address 0x0000_0736 : Local D-End Reg.3 Address	0x0000_0000

14 UART

adStar-L has 2 channel UART(Universal Asynchronous Receiver/Transmitter) controller, and it allows asynchronous communication with general PC or I/O devices equipping RS-232 interface.

14.1 Features

- Compatible with standard 16450/16550 UARTs
- Fully programmable serial-interface protocols
  - 5,6,7,8-bit characters
  - Even, odd or no-parity, stick parity generation and detection
  - 1, 1.5, 2 stop bit generation
  - Baud rate generator
- Line break generation and detection
- False start bit detection
- Prioritized transmit, receive and line status control interrupts
- Independent 16 characters transmit and receive 16Bytes FIFOs
- 2 Ch. UARTs

14.2 Block Diagram

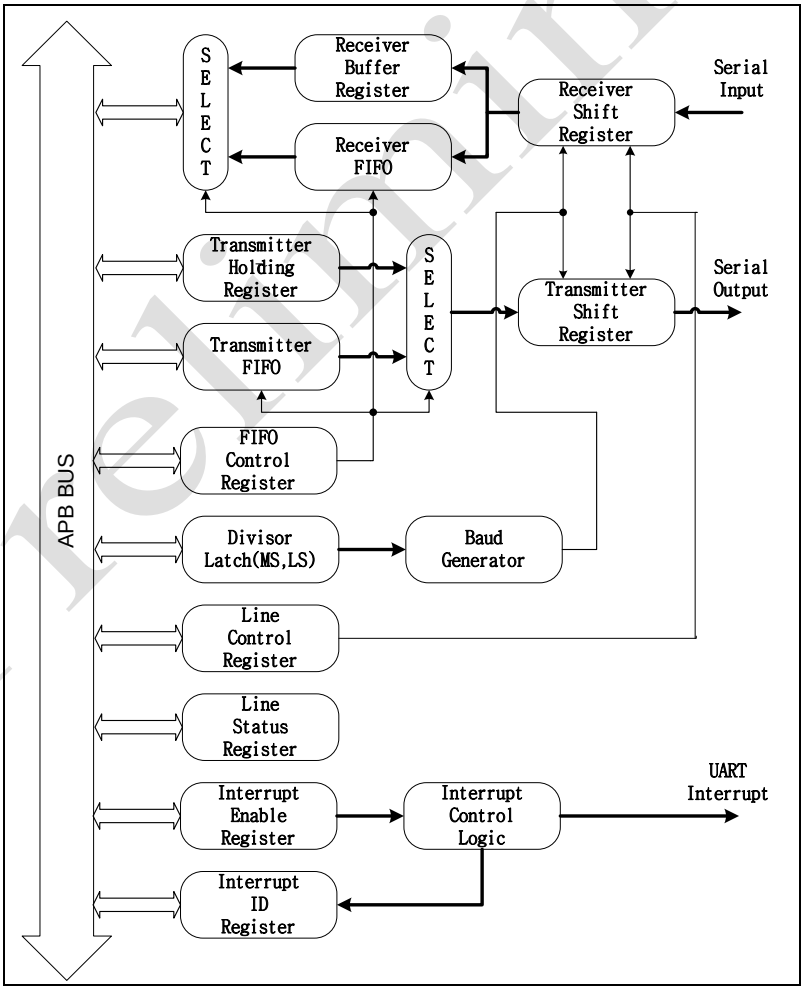
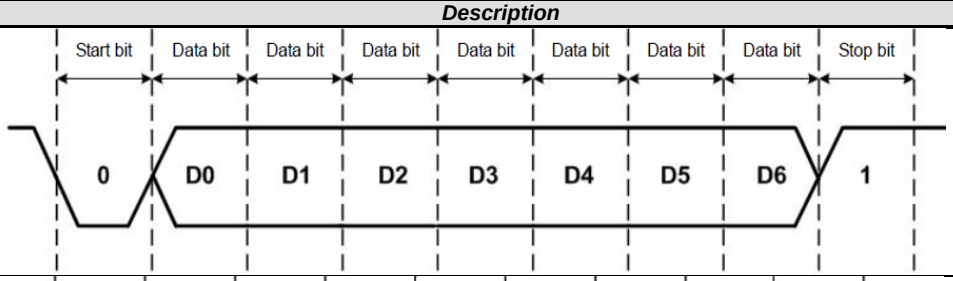
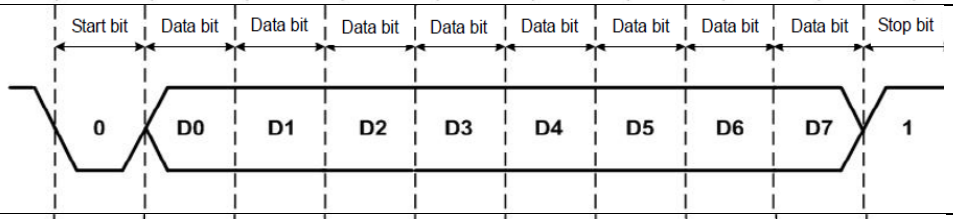
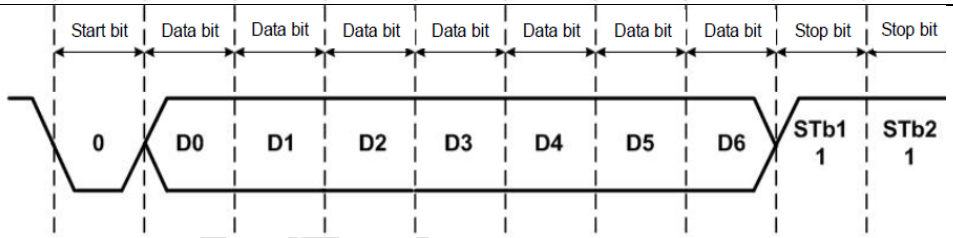
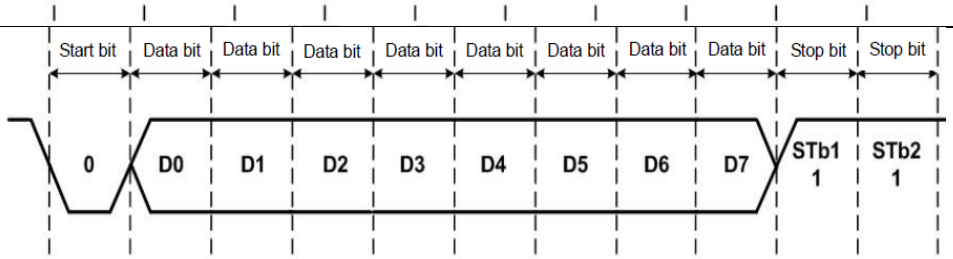
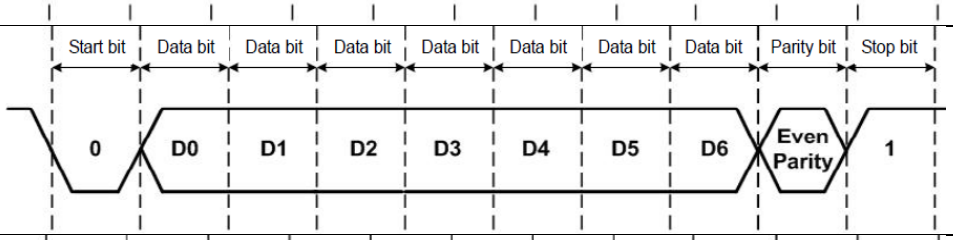
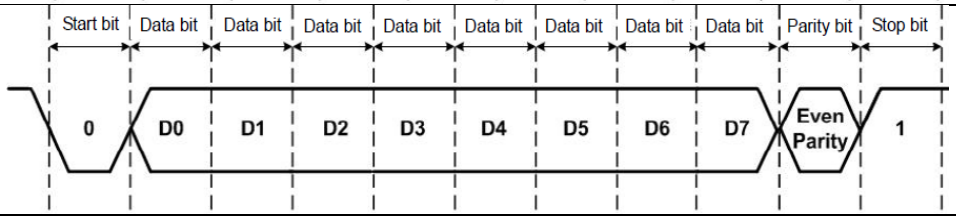


Figure 14-1 UART Block Diagram

14.3 Functional Description

14.3.1 Serial Data Format

UART of adStar-L can change the serial data format of UART communication by configuring ULCRn[4:0] bits. Following table explains available data formats.

ULCRn[4:0]	Description
00010 No Parity / 1 Stop bit / 7 Data bit	
00011 No Parity / 1 Stop bit / 8 Data bit	
00110 No Parity / 2 Stop bit / 7 Data bit	
00111 No Parity / 2 Stop bit / 8 Data bit	
11010 Even Parity / 1 Stop bit / 7 Data bit	
11011 Even Parity / 1 Stop bit / 8 Data bit	

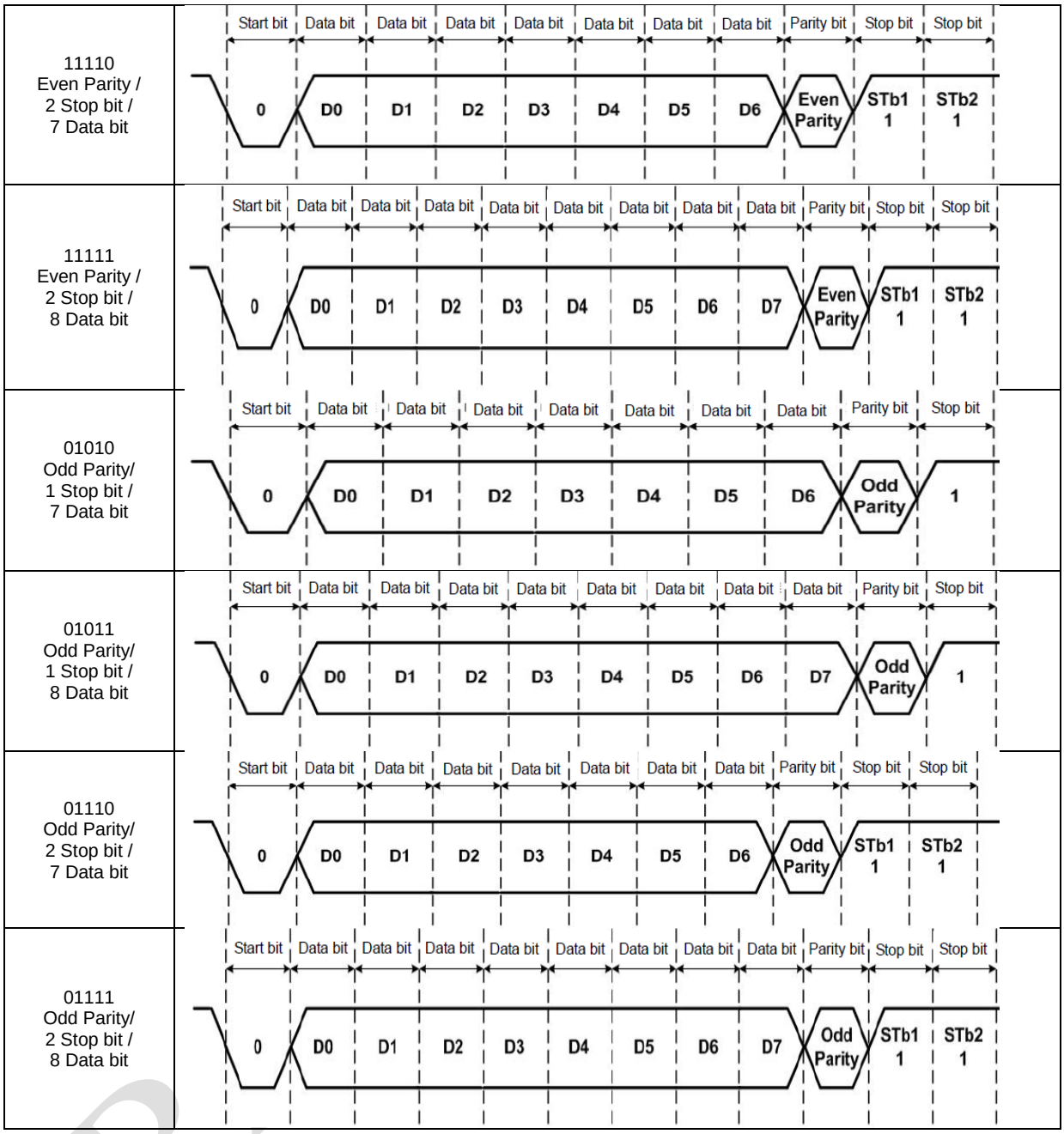


Figure 14-2 UART LCR Register Setting and Serial Data Format

14.3.2 UART Baud Rate

TX/RX Baud Rate can be calculated from the following equation.

$$UART\ \ Baud\ \ Rate = \frac{f_{PCLK}}{16\ \times\ UDL}$$

UART Divisor Latch Value (UDL) = UDLM[7:0] << 8 + UDLL[7:0]

Table 14-1 UART Baud Rate

f_{PCLK} (MHz)		1.024	2.048	5.6448	11.2896	24.0	48.0	62.0
2400 bps	UDL	27	53	147	294	625	1250	1615
	ERR(%)	1.23	0.63	0.00	0.00	0.00	0.00	0.03
4800 bps	UDL	-	27	74	147	313	625	807
	ERR(%)	-	1.23	0.68	0.00	0.16	0.00	0.04
9600 bps	UDL	-	-	37	74	156	313	404
	ERR(%)	-	-	0.68	0.68	0.16	0.16	0.09
14400 bps	UDL	-	9	25	49	104	208	268
	ERR(%)	-	1.23	2.00	0.00	0.16	0.16	0.03
19200 bps	UDL	-	-	18	37	78	156	202
	ERR(%)	-	-	2.08	0.68	0.16	0.16	0.09
38400 bps	UDL	-	-	9	18	39	78	101
	ERR(%)	-	-	2.08	2.08	0.16	0.16	0.41
57600 bps	UDL	-	-	6	12	26	52	67
	ERR(%)	-	-	2.08	2.08	0.16	0.16	1.07
115200bps	UDL	-	-	3	6	13	26	34
	ERR(%)	-	-	2.08	2.08	0.16	0.16	1.07

* UART is assumed to be unreliable when ERR is higher than 2.2%.

UART Fractional Divider Latch Value (FDL) = {(float(PCLK/16*BPS)) – (int(PCLK/16*BPS))}* 64 + 0.5

Table 14-2 UART Fractional Baud Rate

f_{PCLK} (MHz)		1.024	2.048	5.6448	11.2896	24.0	48.0	62.0
2400 bps	FDL	43	21	0	0	0	0	37
	ERR(%)	0.01	0.00	0.00	0.00	0.00	0.00	0.00
4800 bps	FDL	21	43	32	0	32	0	19
	ERR(%)	0.03	0.01	0.00	0.00	0.00	0.00	0.00
9600 bps	FDL	43	21	48	32	16	32	41
	ERR(%)	0.07	0.03	0.00	0.00	0.00	0.00	0.00
14400 bps	FDL	28	57	32	0	11	21	6
	ERR(%)	0.15	0.01	0.00	0.00	0.00	0.00	0.00
19200 bps	FDL	-	43	24	48	8	16	53
	ERR(%)	-	0.07	0.00	0.00	0.00	0.00	0.00
38400 bps	FDL	-	21	12	24	4	8	58
	ERR(%)	-	0.15	0.00	0.00	0.00	0.00	0.00
57600 bps	FDL	-	14	8	16	3	5	18
	ERR(%)	-	0.15	0.00	0.00	0.01	0.01	0.01
115200bps	FDL	-	-	4	8	1	3	41
	ERR(%)	-	-	0.00	0.00	0.04	0.01	0.01

14.4 Register Summery

Table 14-3 UART Register Summery

Bit No.	DLAB = 0 0x00	DLAB = 0 0x00	DLAB = 0 0x04	DLAB = 0 0x08	DLAB = X 0x08	DLAB = X 0x0C	DLAB = X 0x14	DLAB = 1 0x00	DLAB = 1 0x04
	Receiver Buffer Register	Transmitter Holding Register	Interrupt Enable Register	Interrupt Ident. Register	FIFO Control Register	Line Control Register	Line Status Register	Divisor Latch (LSB)	Divisor Latch (MSB)
	RBR	THR	IER	IIR	FCR	LCR	LSR	DLL	DLM
	R	R/W	R/W	R	R/W	R/W	R	R/W	R/W
0	Data Bit 0	Data Bit 0	Enable Received Data Available Interrupt	"0" if Interrupt Pending	FIFO Enable	Word Length Select Bit 0	Data Ready	Bit 0	Bit 0
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt	Interrupt ID Bit 0	RCVR FIFO Reset	Word Length Select Bit 1	Overrun Error	Bit 1	Bit 1
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt	Interrupt ID Bit 1	XMIT FIFO Reset	Number of Stop Bits	Parity Error	Bit 2	Bit 2
3	Data Bit 3	Data Bit 3	0	Interrupt ID Bit 2	0	Parity Enable	Framing Error	Bit 3	Bit 3
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select	Break Interrupt	Bit 4	Bit 4
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	Transmitter Holding Register	Bit 5	Bit 5
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled	RCVR Trigger(LSB)	Set Break	Transmitter Empty	Bit 6	Bit 6
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled	RCVR Trigger(MSB)	Divisor Latch Access Bit (DLAB)	Error in RCVR FIFO	Bit 7	Bit 7

* DLAB = LCR[7](Divisor Latch Access Bit)
* FIFO Control Register :
  - DLAB = 0 : Register Write
  - DLAB = 1 : Register Read
* Address 0x10(0x30), 0x18(0x38), 0x1C(0x3C) are reserved for compatibility with 16550 UART standard..

14.5 Register Description

14.5.1 UART Channel Receiver Buffer Registers (UxRB)

Address : 0x8002_0800 / 0x8002_0820

Bit	R/W	Description	Default Value
31: 8	R	Reserved.	-
7 : 0	R	Receive Buffer Data	-

* Accessible when DLAB is “0”.

14.5.2 UART Channel Transmitter Holding Registers (UxTH)

Address : 0x8002_0800 / 0x8002_0820

Bit	R/W	Description	Default Value
31: 8	W	Reserved.	-
7 : 0	W	Transmit Holding Data	-

* Accessible when DLAB is “0”.

14.5.3 UART Channel Interrupt Enable Registers (UxIE)

Address : 0x8002_0804 / 0x8002_0824

Bit	R/W	Description	Default Value
31: 3	R	Reserved.	-
2	RW	RLSIEN : Receiver Line Status Interrupt Enable bit 0 : Disable 1 : Enable	0
1	RW	THEIEN : Transmitter Holding Empty Interrupt Enable bit 0 : Disable 1 : Enable	0
0	RW	RDAIEN : Received Data Available Interrupt Enable bit 0 : Disable 1 : Enable	0

* Accessible when DLAB is “0”.

14.5.4 UART Channel Interrupt Identification Register (UxII)

Address : 0x8002_0808 / 0x8002_0828

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7 : 6	R	FIFOST : FIFOs Enabled Status bit. 00 : not in FIFO mode 11 : FIFO mode	00
5 : 4	R	Reserved	0
3 : 0	R	INTID : UART Interrupt ID (Note, UART Interrupt Control Function)	0001

* Accessible in read mode only when DLAB is “0”.

Table 14-4 UART Interrupt Control Function

Interrupt Identification Register				Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Condition
Bit 3	Bit 2	Bit 1	Bit 0				
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available or Trigger Level Reached	Reading the Receiver Buffer Register or the FIFO Drops Below the Trigger Level
1	1	0	0	Second	Character Timeout Indication	No Characters have been removed from or input to the RCVR FIFO during the last 4 Char. times, and there is at least 1 Char. in it during this Time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register

14.5.5 UART Channel FIFO Control Register (UxFC)

Address : 0x8002_0808 / 0x8002_0828

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7 : 6	RW	RFTL : Receiver FIFO Trigger Level 00 : 1 Byte 01 : 4 Byte 10: 8 Byte 11 : 14 Byte	00
5 : 3	R	Reserved	-
2	RW	XFR : XMIT FIFO Reset All data in XMIT FIFO is reset when XFR is “1”. However, data is shift register isn’t reset.	0
1	RW	RFR : RCVR FIFO Reset All data in RCVR FIFO is reset when RFR is “1”. However, data is shift register isn’t reset.	0
0	RW	FIFOEN : FIFO Enable Bit 0 : 16450 UART Mode1 : Enables FIFO	0

* DLAB = “0” ➔ write mode, DLAB =”1” ➔ read mode.

14.5.6 UART Channel Line Control Register (UxLC)

Address : 0x8002_080C / 0x8002_082C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7	RW	DLAB : Divisor Latch Access Bit When this bit is “1”, divisor latch register can be read/written and FIFO control register can be read.	0
6	RW	SB : Set Break When this bit is “1”, serial data output pin outputs logic “0”. SB doesn’t affect internal transmitter logic. It only affects serial output.	0
5	RW	SP : Stick Parity 0 : Disables Stick Parity 1 : PEN, EPS, and SP are “1” ➔ Parity bit=”0” PEN and SP are “1”, EPS is “0” ➔ Parity bit=”1”	0
4	RW	EPS : Even Parity Select 0 : Select Odd Parity 1 : Select Even Parity	0
3	RW	PEN : Parity Enable Bit 0 : Disables Parity 1 : Enables Parity	0
2	RW	STB : Number of Stop Bit 0 : 1 Stop bit 1 : 2 Stop bits (If WLS bit is set to 00(=5bits/character), it will be 1.5 instead of 2	0
1 : 0	RW	WLS : Word Length Select 00 : 5 Bits/Character 01 : 6 Bits/Character 10 : 7 Bits/Character 11 : 8 Bits/Character	00

14.5.7 UART Channel Line Status Register (UxLS)

Address : 0x8002_0814 / 0x8002_0834

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7	R	EIRF : Error in RCVR FIFO If not in FIFO mode, EIRF is always “0”. In FIFO mode, EIRF become “1” if any of OE, PE, FE, or BI of RCVR FIFO is set “1”. EIRF is cleared (=”0”) when LSR register is read and FIFO doesn’t have consecutive errors.	0
6	R	TEMP : Transmitter Empty If not in FIFO mode, TEMT become “1” when both transmitter holding register (THR) and Transmitter shift register (TSR) are empty. If either of THR or TSR has data, it is cleared. In FIFO mode, it is set when both of transmitter FIFO and TSR are empty.	1
5	R	THRE : Transmitter Holding Register Empty If not in FIFO mode, THRE is set when THR become empty by transmitting data to TSR. At this moment, THR can be written new data to transmit. In FIFO mode, THRE is set when transmit FIFO is empty, and cleared when any byte is written into transmit FIFO. If both THRE interrupt (ETHREI) and THRE are “1”, interrupt raises.	1
4	R	BINT : Break Interrupt : BI is set when input data is “0” during the full word transmission time. Full word transmission time is the sum of start, data, parity, and stop bit transmission time. In FIFO mode, this error applies to each byte inside FIFO, and FIFO are cleared when BI happens. This bit is cleared when CPU reads LSR.	0
3	R	FERR : Framing Error FE is set when input data doesn’t have valid stop bit. In FIFO mode, this error applies to each byte inside FIFO. It is cleared when CPU reads LSR.	0
2	R	PERR : Parity Error PE is set when input data doesn’t coincide with parity bit chosen by LCR register. In FIFO mode, this error applies to each byte inside FIFO. It is cleared when CPU read LSR.	0
1	R	OERR : Overrun Error In not FIFO mode, OE is set when new data is written before data inside RBR is read. In FIFO mode, it is set if a new full word comes to receiver shift register (RSR) when FIFO is full. In this case, RSR is updated; however, FIFO doesn’t transmit. It is cleared when CPU reads LSR.	0
0	R	DRDY : Data Ready DR is set when received data is written on RBR or FIFO. It is cleared when every data inside RBR or FIFO is read.	0

14.5.8 UART Channel Divisor Latch LSB Register (UxDLL)

Address : 0x8002_0800 / 0x8002_0820

Bit	R/W	Description	Default Value
31: 8	R	Reserved.	-
7 : 0	RW	Divisor Latch Least Significant Byte	0x00

* Accessible when DLAB is “1”.

14.5.9 UART Channel Divisor Latch MSB Register (UxDLM)

Address : 0x8002_0804 / 0x8002_0824

Bit	R/W	Description	Default Value
31: 8	R	Reserved.	-
7 : 0	RW	Divisor Latch Most Significant Byte	0x00

* Accessible when DLAB is “1”.

14.5.10 UART Channel Fractional Divider Register (UxFDR)

Address : 0x8002_081C / 0x8002_082C

Bit	R/W	Description	Default Value
7	RW	0: Normal divider baud rate mode 1: Fractional divider baud rate mode	0
6	R	Reserved	-
5:0	RW	Fractional Divider Bit	00000

15 DMA

15.1 Features

- Compatibility with AMBA AHB Specification

- Provides 6 channels. Each channels supports DMA.

- 16-port DMA Request.
DMAC provides 16-port DMA Request signal for Peripherals.

- Provides Single Request and Burst Request.
DMA request that provides to peripherals supports both Single Request and Burst Request.

- 4 types of DMA communication
DMA provides memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral communications.

- Provides Scatter and Gather by using Auto Reload functionality.

- Provides Scatter and Gather by using Linked list

- Priority of the DMA channel is fixed by hardware. Channel 0 has the highest priority and channel 7 has the lowest priority.

- Provides Multi-Layer AHB Bus by embedding 2 AHB Master.

- Provides Programmable Burst Size. In order to achieve higher efficiency of DAM transmit, user can configure Burst Size. The Burst Size is generally configured as half size of that of FIFO which is embedded in Peripheral.

- Each channel has 4 Word FIFO.

- Each channel has separated DMA Error Interrupt and DMA Terminal Count Interrupt.

- Supports Interrupt Enable.
DMA has an enable bit for both DMA Error Interrupt and DMA Terminal Count Interrupt.

15.2 Block Description

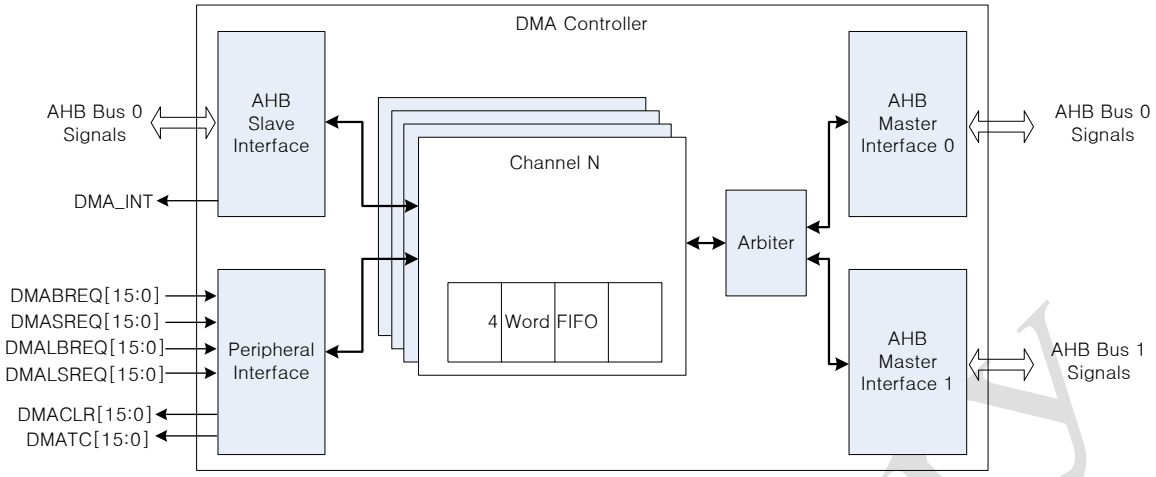


Figure 15-1 DMA Block Diagram

DMA has 6-channel. Each channel controls data flow that one-direction transfers from Source Peripheral to Destination Peripheral and contains 4x4 byte FIFO.

AHB Master Interface is responsible for data transmit from/to AHB Bus after receive data transfer requests from each channel. Inside the DMA Controller, because there are 2 AHB Master Interface, the DMA Controller can connect to other bus interface. Due to that reason, in spite of both Source Peripheral and Destination Peripheral connect to other bus, they can transfer data.

The Arbiter transmits data to AHB Master Interface0 or AHB Master Interface1 according to priority of data transfer request. It is determined by data address which AHB Master Interface should be use.

AHB Slave Interface is responsible for configures registers of each channel and requests interrupt.

Peripheral Interface receives DMA Request signal from Peripherals and send a signal to the corresponding channel according to Peripheral Selection bit. The Peripheral Interface can receive maximum 16 DMA Request signals. The channel can receive 2 DMA request signals Source DMA Request signal and Destination DMA Request signal.

15.3 Functional Description

15.3.1 DMA Operation

- **Transfer Hierarchy**

DMA transfer has 3-layer hierarchy as Figure 15-2.

The highest layer is called DMA Transfer. DMA Transfer indicates total size of data that is transferred by DMA. The size of transmit is determined by Transfer size of Control register.

The second layer is called Burst Transaction. Amount of data that is transferred from Burst Transaction is determined by Burst Size of Control register. Generally, the size is set to FIFO size of peripherals. Because the peripherals cannot transfer all of data at one time, the peripherals separates data in the unit of FIFO size and sends it.
** The burst size of control register is not AMBA Burst Transfer's burst size.

The lowest layer is called AMBA Burst Transfer. The Burst Transaction is divided into AMBA Burst Transfer unit. In this layer, data transfer is controller by hardware not user.

User can configure smaller Transfer Size than Burst Size. In that case, the Burst Transaction sends data with configured Transfer size.

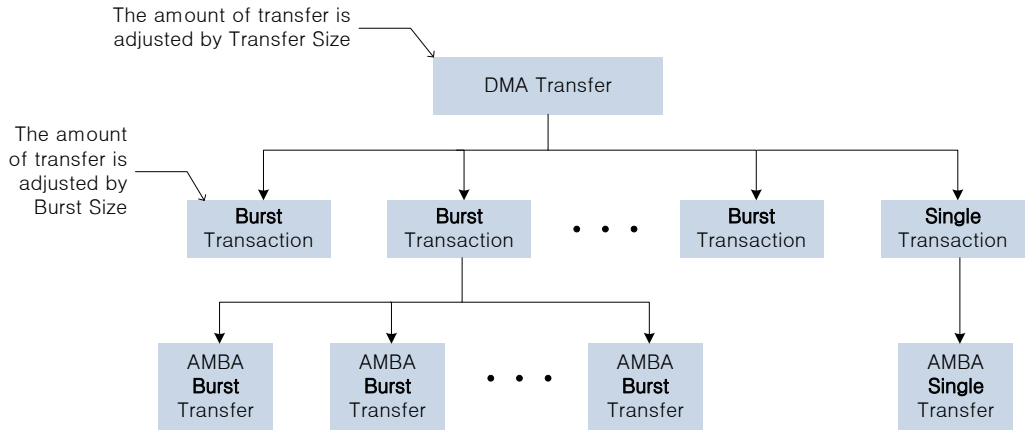


Figure 15-2 DMA Transfer hierarchy

- **Transfer type**
  User should specify that Transfer type in DMA configuration. The transfer type is one of following 4 types.

1. Memory to Memory
2. Memory to Peripheral
3. Peripheral to Memory
4. Source Peripheral to Destination Peripheral

Memory to Memory type indicates that a source address is Memory and also a destination address is memory. Memory to Peripheral type indicates that a source address is Memory and Destination address is Peripheral. In order words, with this type, DMA transfers data from Memory to Peripheral buffer.

The reason that user should specify the Transfer type is informing to DMA that whether handshake process is necessary or not. DMA uses handshake method when transfers data between peripherals not memory. To transfer data between peripherals not memory, the peripherals needs preparation and time. Also, the size of transmit is limited. With the handshake method, DMA Controller transfers data only when the data is ready. However, in the case of the peripheral is memory, it is not necessary that handsake process, because Memory can be accessed anytime. Therefore, user should specify the transfer type and inform to DMA Controller that data transmit is handshake method or not.

- **Flow Controller**

Flow Controller is a module that determines DMA Transfer size. Flow Controller is DMA Controller or one of Peripherals. If DMA Controller is Flow Controller, then the DMA data transfer size is determined as configured Transfer Size.
Also, a peripheral can be Flow Controller. In this case, DMA Controller transfers data according to request signal of Peripheral and ignores configured Transfer size. In order to finish DMA Transmit, when Flow Controller requires the last data, DMA Controller sends Last Request. Once the DMA Controller receives Last Request, the DAM transmit is finished after sending the last data.

15.3.2 Linked List Operation

- **LLI**

LLI (Linked List Item) is a data structure that contains basic information to DMA transmits. The contents of LLI are Source Address, Destination Address, Next LLI Address, and Control information. Linked List Operation is that reading first LLI and updates internal registers. After that, the operation does DMA Transfer. When the DMA transfer is finished, the operation reads the next LLI according to the next LLI address. Following Figure 15-3 depicts LLI structure

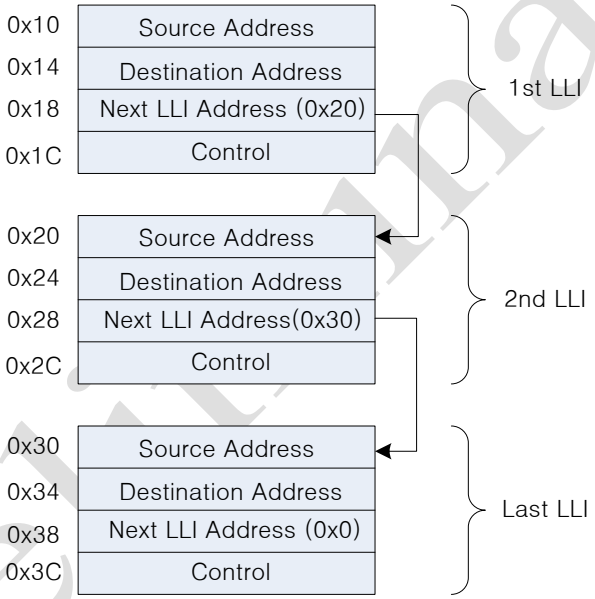


Figure 15-3 Linked list

The next LLI address of the last LLI is reserved as 0. If DMA Controller confirms the Next LLI address is 0, the DMAC can know the LLI is the last. Therefore, if an address of LLI is 0, the LLI operation cannot be executed.

- **Multi Block Transfer**

Transfers data that is described as LLI structure is called Multi Block Transfer. In order words, LLI data is defined as Block. The number of LLI refers to the number of Block. Also, the size of Block is defined as Control register's Transfer Size. The following Figure 15-4 shows hierarchical view of Multi Block Transfer.

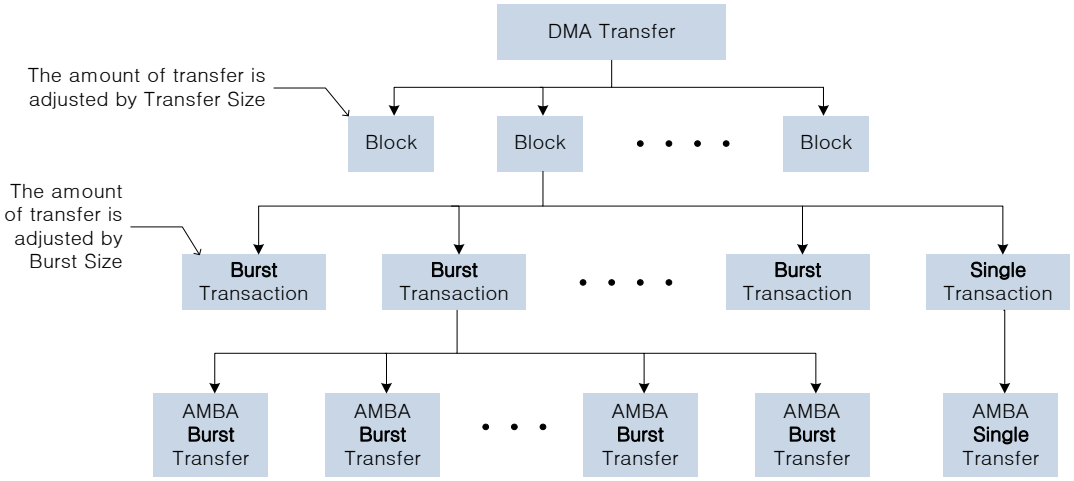


Figure 15-4 Multi Block Transfer

- **Scatter & Gather with Liked list**

Scatter indicates spread data by DMA Transfer and Gather indicates that putting together the separated data. User can the Scatter and Gather operations by using LLI.

The following Figure 15-5 shows an example for Gather operation by using LLI. In the figure, data is depicted as rectangle and the data is copied into peripheral.

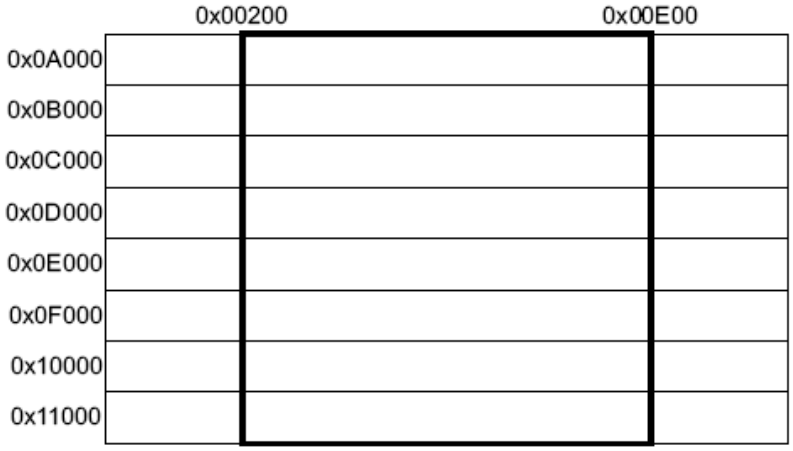


Figure 15-5 Gathering by using LLI

LLI starts from address 0x20000

The contents of the first LLI
Source Address: 0x0A200
Destination Address: Peripheral Address
Source and Destination transfer width: 8bit
Source and Destination burst Size: 16 burst
Transfer Size: 3072 byte, 0xC00
Next LLI Address: 0x20010

The contents of the second LLI
Source Address: 0x0B200
Destination Address: Peripheral Address
Source and Destination transfer width: 8bit
Source and Destination burst Size: 16 burst
Transfer Size: 3072 byte, 0xC00
Next LLI Address: 0x20020

The Contents of the last LLI
Source Address: 0x11200
Destination Address: Peripheral Address
Source and Destination transfer width: 8bit
Source and Destination burst Size: 16 burst
Transfer Size: 3072 byte, 0xC00
Next LLI Address: 0x0

15.3.3 Auto Reload Operation

The basic operation of Auto Reload Operation is when DMA Transfer is finished; reload Control register value to repeat DMA Transfer. The number of repeat count is determined by Auto Reload Count Register. The value of Auto Reload Count decreases by 1 when Auto Reload is occurred. If the value is 0, the Auto Reload Operation is stopped. The Auto Reload Operation is not necessary to mode configuration additionally. When finish DMA Transfer, if the value of Auto Reload Count Register is not 0, the Auto Reload Operation does not operate.

- **Transfer Hierarchy**

Auto Reload Operation is categorized in Multi Block Transfer like as Linked List Operation. The number of Block is Auto Reload Count + 1, and the size of data transferred is set to Transfer Size.

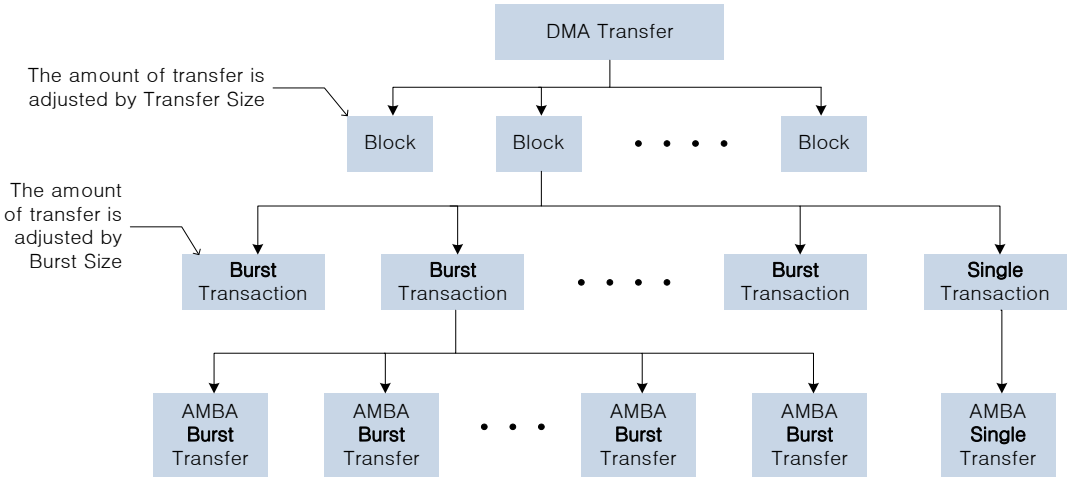


Figure 15-6 Auto Reload Operation Transfer Hierarchy

- **Scatter with Auto reload**

The following Figure 15-7shows an example for Scatter with Auto Reload Operation. Whenever finishing Block data transfer, Destination Scatter Address indicates uniform size of space between Destination Blocks' start address. User can separate between Blocks and can implement Scatter operation by using the Destination Block Address Register.

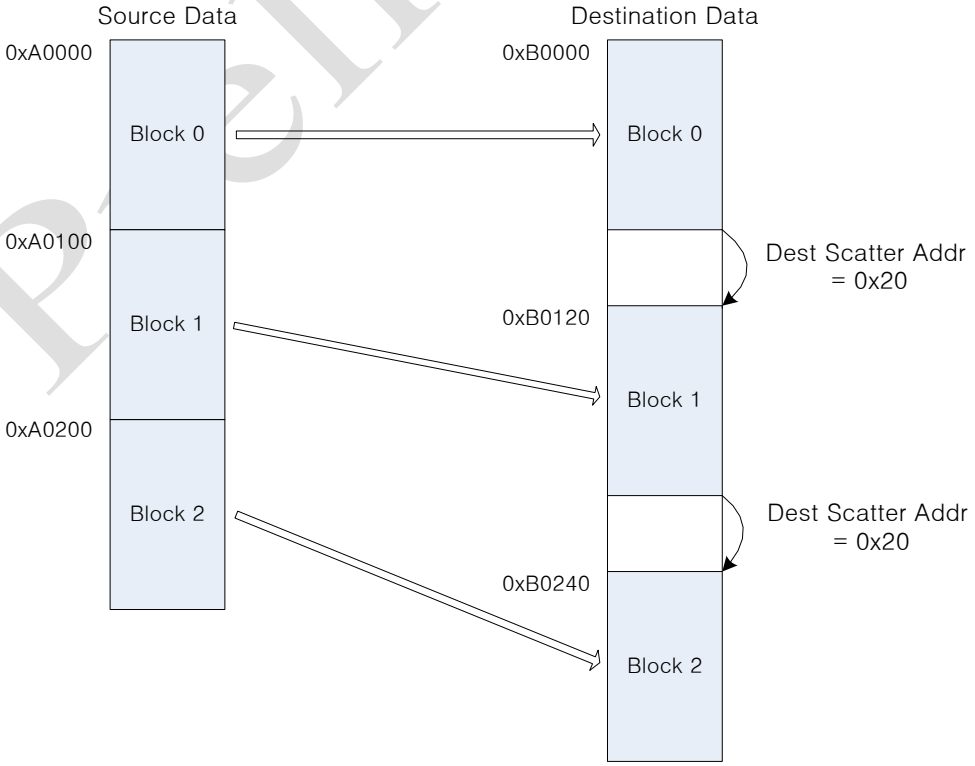


Figure 15-7 Scatter with Auto Reload Operation

Register Configuration
Source Address: 0xA0000
Destination Address: 0xB0000
Source and Destination transfer width: 32bit
Source and Destination burst Size: 4 burst
Transfer Size: 0x40
Auto Reload Count: 2
Destination scatter Address: 0x20

- **Gather with Auto reload**

The following Figure 15-8shows an example for Gather with Auto Reload Operation. Whenever finishing Block data transfer, Source Gather Address indicates uniform size of space between Source Blocks' start address. User can separate between Blocks and can implement Gather operation by using the Source Block Address Register.

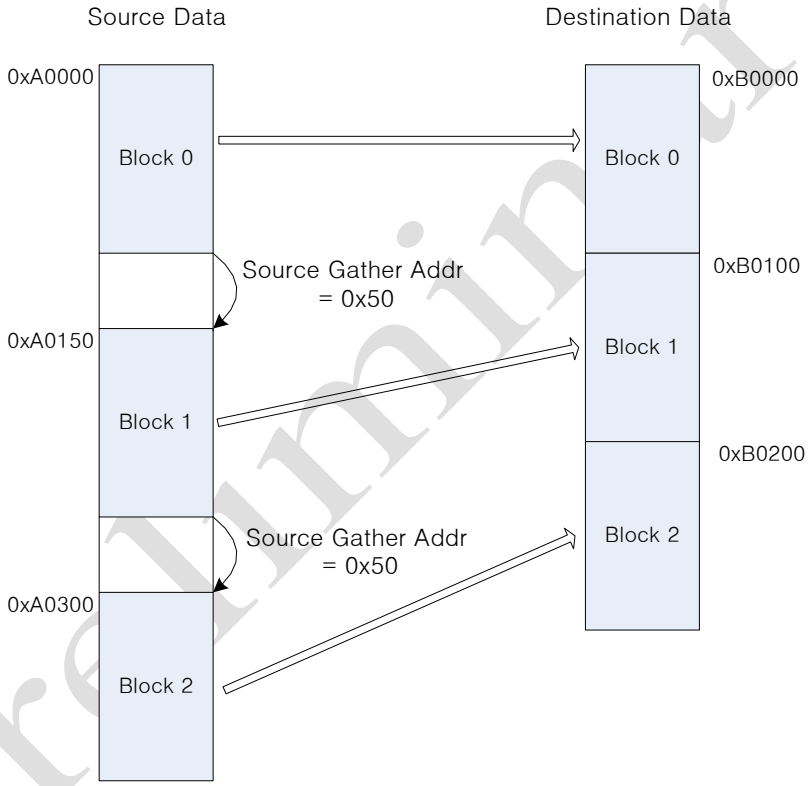


Figure 15-8 Gather with Auto Reload Operation

Register Configuration
Source Address: 0xA0000
Destination Address: 0xB0000
Source and Destination transfer width: 32bit
Source and Destination burst Size: 4 burst
Transfer Size: 0x40
Auto Reload Count: 2
Source gather Address: 0x50

15.3.4 Peripheral Interface

- ***Hand Shake Signals***

DMA Request signal and DMA Clear signal is used for Handshake DMA data transfer between Peripherals not memory.

Four DMA Request signals are used when peripheral requests data transfer to DMA Controller (Refer to Figure 15-9). Peripheral selects one signal of the 4, and requests. It is not allow to select multiple signal at the same time.

DMA Clear signal is a response of DMA Request. DMA Controller sends the signal to Peripheral.

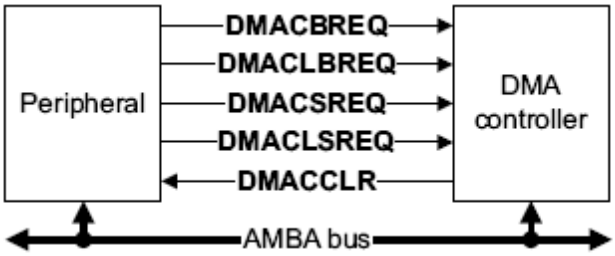


Figure 15-9 DMA Handshake Signals

- DMABREQ
  Burst Request signal. If the signal is activated, DMA Data Transfer becomes Burst Transaction by DMA Controller and the size of data is determined by Burst Size.

- DMASREQ
  Single Request signal. If the signal is activated, DMA Data Transfer becomes Single Transaction.

- DMALBREQ
  Last Burst Request. When peripheral is Flow Controller, this signal is used for informing that data is the last DMA Burst Request. If DMALBREQ is activated, the last Burst Transaction is operated and DMA Transfer is finished.

- DMALSREQ
  Last Single Request. When peripheral is Flow Controller, this signal is used for informing that data is the last DMA Single Request. If DMALBREQ is activated, the last Single Transaction is operated and DMA Transfer is finished.

- DMACLR
  DMA Clear signal. With this signal, all of the Requests from peripheral are inactivated.

- **Time diagram of DMA Request**

If peripheral send request to DMA Controller, the DMA Controller programed transfer data amount of Burst Size, and then send DMA Clear signal. At that time, when all of data transfer is finished, DMATC (DMA Terminal Count) signal is activated. With the signal, peripheral can check whether the DMA data transfer is finished or not.

When peripheral receives DMA Clean signal (DMACLR), DMA Request signal is inactivated. If peripheral inactivates DMA Request before receives DMA Clear signal, it can be a problem. Also, peripheral tries to send Next DMA Request signal, it is possible only when the current DMA Clear signal is inactivated.

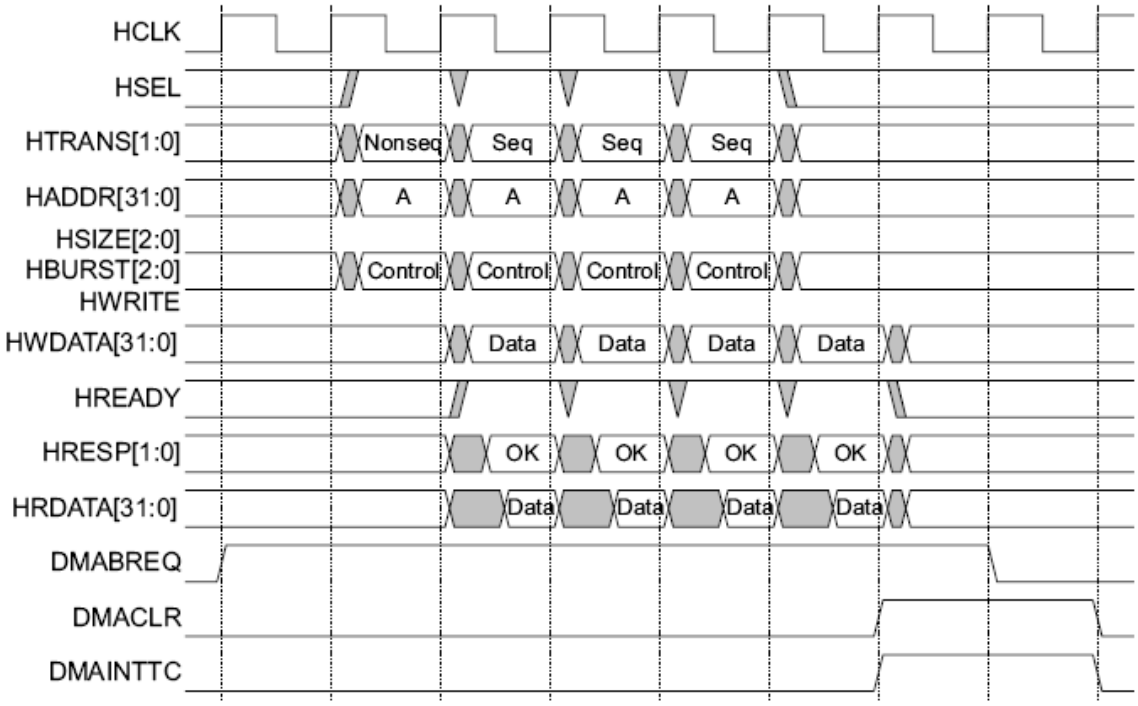


Figure 15-10 Time Diagram of DMA Request

15.4 Register Description

15.4.1 DMA Interrupt Status (DMAIntStatus)

Address: 8000_1400

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R	Interrupt Status of Channel This register indicates interrupt request status from each channel. ex) If bit 0 is set, interrupt is occurred from channel 0. If bit 1 is set, interrupt is occurred from channel 1. Because there are 2 types of interrupt, user should check interrupt type by reading DMATCIS and DMATCIC registers.	0

15.4.2 DMA Terminal Count Interrupt Status (DMATCIntStatus)

Address: 8000_1404

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R	Terminal Count Interrupt Status of Channel This register indicates whether Terminal Count Interrupt is occurred or not from each channel.	0

15.4.3 DMA Terminal Count Interrupt Clear (DMATCIntClr)

Address: 8000_1408

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	W	Terminal Count Interrupt Clear Each bit of this register has responsible for clear Terminal count interrupt. If the bit is set, a correspond channel's interrupt is cleared.	0

15.4.4 DMA Error Interrupt Status (DMAErrorIntStatus)

Address: 8000_140C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R	Error Interrupt Status of Channel The register indicated that whether the DMA Transfer error interrupt is occurred or not.	0

15.4.5 DMA Error Interrupt Clear (DMAErrorIntClr)

Address: 8000_1410

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	W	Error Interrupt Clear Each bit has responsible for clearing DMA Transfer error interrupt. If the bit is set, the corresponding channel's interrupt is cleared.	0

15.4.6 DMA Block Interrupt Status (DMABlockIntStatus)

Address: 8000_1414

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R	Block Interrupt Status of Channel With this register, user can know whether DMA Block interrupt is occurred or not.	0

15.4.7 DMA Block Interrupt Clear (DMABlockIntClr)

Address: 8000_1418

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	W	Block Interrupt Clear Each bit has responsible for clearing DMA Block interrupt. If the bit is set, the corresponding channel's interrupt is cleared.	0

15.4.8 DMA Raw Terminal Count Interrupt Status (DMARawTCIntStatus)

Address: 8000_141C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R	Raw Terminal Count Interrupt Status of Channel This register informs that each channel's Terminal Count Interrupt is occurred when the channel is disabled by interrupt Enable bit.	0

15.4.9 DMA Raw Error Interrupt Status (DMARawErrorIntStatus)

Address: 8000_1420

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R	Error Interrupt Status of Channel This register informs that each channel's Error Interrupt is occurred.	0

15.4.10 DMA Enabled Channel Status (DMAEnbldChn)

Address: 8000_1424

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R	Enabled Channel Status Enabled Channel Status Each bit informs that DAM is Enabled or Disabled.	0

15.4.11 DMA Software Burst Request (DMASoftBReq)

Address: 8000_1428

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	
15 : 0	RW	Software Burst Request The register generates DMA Burst Request signal in software. If user write 1 to correspond bit, DMA Burst Request signal is sent and Clear is automatically operates	0

15.4.12 DMA Software Single Request (DMASoftSReq)

Address: 8000_142C

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	
15 : 0	RW	Software Single Request The register generates DMA Single Request signal in software. If user writes 1 to corresponding bit, DMA Single Request signal is sent and Clear is automatically operates.	0

15.4.13 DMA Software Last Burst Request (DMASoftLBReq)

Address: 8000_1430

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	
15 : 0	RW	Software Last Burst Request The register generates DMA Last Burst Request signal in software. If user writes 1 to correspond bit, DMA Last Burst Request signal is sent and Clear is automatically operates.	0

15.4.14 DMA Software Last Single Request (DMASoftLSReq)

Address: 8000_1434

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	
15 : 0	RW	Software Last Single Request The register generates DMA Last Single Request signal in software. If user writes 1 to correspoing bit, DMA Last Single Request signal is sent and Clear is automatically operates.	0

15.4.15 Channel Source Address Register (ChnSrcAddr)

Address: 8000_1500 / 8000_1520 / 8000_1540 / 8000_1560
8000_1580 / 8000_15A0

Bit	R/W	Description	Default Value
31 : 0	RW	Source Address This register sets Source Address of each channel. The configured address value should fit alignment according to Source transfer width. Source Address automatically increases as data transfer. Due to this reason, this register should hold data address to send always. However, the source address value during a channel operation (Data transfer) is insignificant. Because the channel keeps operating data transfer, even though program reads the source address. But, after finishing the channel's data transmit, if user checks the register, user can confirm that all of data is read or not.	0

15.4.16 Channel Destination Address Register (ChnDstAddr)

Address: 8000_1504 / 8000_1524 / 8000_1544 / 8000_1564
8000_1584 / 8000_15A4

Bit	R/W	Description	Default Value
31 : 0	RW	Destination Address This register sets Destination Address of each channel. The configured address value should fit alignment according to Destination transfer width. Destination Address automatically increases as data transfer. Due to this reason, this register should hold data address to send always. However, the destination address value during a channel operation (Data transfer) is insignificant. Because the channel keeps operating data transfer, even though program reads the source address. But, after finishing the channel's data transmit, if user checks the register, user can confirm that all of data is read or not.	0

15.4.17 Channel Linked List Item Register (ChnLLI)

Address: 8000_1508 / 8000_1528 / 8000_1548 / 8000_1568
8000_1588 / 8000_15A8

Bit	R/W	Description	Default Value
31 : 2	RW	Linked List Item Address This register specifies start address of Linked List Item of each channel. If the value of the register is not 0x0 and the channel is enabled, DMA Controller loads Linked List Item from the start address. After that, DMA Controller updates internal registers and executes Linked List Operation. With the default value (0x0) of the register DMA Controller does not executes Linked List Operation.	0
1 : 0	R	Reserved	0

15.4.18 Channel Control Register (ChnCntl)

Address: 8000_150C / 8000_152C / 8000_154C / 8000_156C
8000_158C / 8000_15AC

Bit	R/W	Description	Default Value
31 : 30	R	Reserved	-
29	RW	Destination Increment If set this bit, destination address is automatically increased according to data transfer.	0
28	RW	Source Increment If set this bit, source address is automatically increased according to data transfer.	0
26 : 24	RW	Destination transfer width 000 : 8bit 100 : Reserved 001 : 16bit 101 : Reserved 010 : 32bit 110 : Reserved 011 : Reserved 111 : Reserved This bit configures data width of destination. It can be set differently from source transfer width. If the destination transfer width is smaller than source transfer width, user should carefully configure Transfer size. (Refer to Program Consideration)	0
23	R	Reserved	
22 : 20	RW	Source transfer width 000 : 8bit 100 : Reserved 001 : 16bit 101 : Reserved 010 : 32bit 110 : Reserved 011 : Reserved 111 : Reserved This bit configures data width of source.	0
19	R	Reserved	
18 : 16	RW	Destination burst size 000 : 1 100 : 32 001 : 4 101 : 64 010 : 8 110 : 128 011 : 16 111 : 256 This bits configures Burst Transaction Size of destination peripheral. It is almost same as AHB Burst Size, but it is upper level transaction that includes the AHB Burst Size. (Refer to Transfer Hierarchy). In the case of the destination is memory, the register works same manner.	0
15	R	Reserved	
14 : 12	RW	Source burst size 000 : 1 100 : 32 001 : 4 101 : 64 010 : 8 110 : 128 011 : 16 111 : 256 This bits configures Burst Transaction Size of source peripheral. It is almost same as AHB Burst Size, but it is upper level transaction that includes the AHB Burst Size. (Refer to Transfer Hierarchy). In the case of the source is memory, the register works same manner.	0
11 : 0	RW	Transfer Size When DMA Controller is Flow Controller, this register indicates the total size of transferred data from DMA channel. The unit of transfer is not Byte but Source Transfer Width. In order words, the total size of data transfer is calculated as (Transfer size) x (source transfer width) This value is decreased as 1 when transfers data. Once the value is 0, DMA Transfer is finished. Therefore, user can know remain data size to transfer if user reads the value. If DMA Controller is not Flow Controller, the value is ignored but the value should be 0 in Program.	000

15.4.19 Channel Configuration Register (ChnCfg)

Address: 8000_1510 / 8000_1530 / 8000_1550 / 8000_1570
8000_1590 / 8000_15B0

<table>
<tr><th>Bit</th><th>R/W</th><th>Description</th><th>Default Value</th></tr>
<tr><td>31 : 22</td><td>R</td><td>Reserved</td><td>0</td></tr>
<tr><td>21</td><td>RO</td><td>FIFO Active
0: FIFO is empty
1 : FIFO has data</td><td>-</td></tr>
<tr><td>20</td><td>RW</td><td>Halt
0 : enable DMA request
1 : ignore DMA request.
User can disable DMA channel by using this bit and clears out FIFO</td><td>0</td></tr>
<tr><td>19</td><td>RW</td><td>Lock
If this bit is set, Locked transfer is operated.</td><td>0</td></tr>
<tr><td>18</td><td>RW</td><td>Block Interrupt Enable
Interrupt Enable bit when Block transfer is finished with Multi Block Transfer. If Block Interrupt is occurred, DMA does not transfer Next Block until the Block Interrupt is cleared.</td><td></td></tr>
<tr><td>17</td><td>RW</td><td>Terminal count interrupt Enable
Enable bit for DMA Transfer finish interrupt.</td><td>0</td></tr>
<tr><td>16</td><td>RW</td><td>Interrupt error Enable
Enable bit for DMA Error Interrupt.</td><td>0</td></tr>
<tr><td>15</td><td>R</td><td>Reserved</td><td>0</td></tr>
<tr><td>14 : 12</td><td>RW</td><td>Flow Control
<table>
<tr><th>Value</th><th>Transfer type</th><th>Flow controller</th></tr>
<tr><td>000</td><td>Memory-to-Memory (Default)</td><td>DMA</td></tr>
<tr><td>001</td><td>Memory-to-Peripheral</td><td>DMA</td></tr>
<tr><td>010</td><td>Peripheral-to-Memory</td><td>DMA</td></tr>
<tr><td>011</td><td>Source peripheral-to-destination peripheral</td><td>DMA</td></tr>
<tr><td>100</td><td>Source peripheral-to-destination peripheral</td><td>Dst. Peri.</td></tr>
<tr><td>101</td><td>Memory-to-Peripheral</td><td>Peripheral</td></tr>
<tr><td>110</td><td>Peripheral-to-Memory</td><td>Peripheral</td></tr>
<tr><td>111</td><td>Source peripheral-to-Destination peripheral</td><td>Src. Peri.</td></tr>
</table>
This bit determines both Transfer type and Flow Controller.</td><td></td></tr>
<tr><td>11 : 8</td><td>RW</td><td>Destination Peripheral
This bit selects one of the 16 DMA Requests.
0000: NAND Flash TX 0001: SDHC
0010: Reserved 0011: Reserved
0100: USB Device Bulk In 0101: Mixer Play CH0 0110: Mixer Play CH1 0111: Mixer Play CH2 1000: Mixer Play CH3
1001: Reserved
1010: ADC 1011: TIMER REQ[0] 1100: TIMER REQ[1] 1101: LCD
1110: Reserved 1111: Reserved</td><td>0</td></tr>
<tr><td>7 : 4</td><td>RW</td><td>Source Peripheral
This bit selects one of the 16 DMA Requests.
0000: Reserved 0001: SDHC
0010: NAND Flash RX 0011: USB Device Bulk out
0100: Reserved 0101: Mixer Play CH0 0110: Mixer Play CH1 0111: Mixer Play CH2 1000: Mixer Play CH3
1001: Reserved
1010: ADC 1011: TIMER REQ[0] 1100: TIMER REQ[1] 1101: LCD
1110: Reserved 1111: Reserved</td><td>0</td></tr>
<tr><td>3 : 1</td><td>R</td><td>Reserved</td><td>0</td></tr>
<tr><td>0</td><td>RW</td><td>Channel Enable

Channel can be activated by this bit. In order to do DMA Transfer, user sets this bit. If the bit is set to 1, DMA Transfer is started with configuration. If the DMA Transfer is finished, this bit is automatically cleared.
Auto Clear conditions are following.
Finish DMA Transfer
Finish Linked List Operation
Finish Auto Reload Operation
Finished by Error

User can finish the activated channel manually by clearing the Enable bit.</td><td>0</td></tr>
</table>

		However, in this case, all of channel FIFO data is removed.	

15.4.20 Channel Source Gather Address Register (ChnSrcGaAddr)

Address: 8000_1514 / 8000_1534 / 8000_1554 / 8000_1574
8000_1594 / 8000_15B4

Bit	R/W	Description	Default Value
31 : 17	R	Reserved	-
16	RW	Auto Reload Source Address If this bit is set, Source Address is reloaded with initially configured source address when Auto Reload.	
15 : 0	RW	Source Gather Address When Auto Reload is operated, the Source Address is added with Source Gather Address.	0

15.4.21 Channel Destination Scatter Address Register (ChnDstScaAddr)

Address: 8000_1518 / 8000_1538 / 8000_1558 / 8000_1578
8000_1598 / 8000_15B8

Bit	R/W	Description	Default Value
31 : 17	R	Reserved	-
16	RW	Auto Reload Destination Address If this bit is set, Destination Address is reloaded with initially configured source address when Auto Reload.	
15 : 0	RW	Destination Scatter Address When Auto Reload is operated, the Destination Address is added with Destination Scatter Address.	0

15.4.22 Channel Auto Reload Count Register (ChnAutoReloadCnt)

Address: 8000_151C / 8000_153C / 8000_155C / 8000_157C
8000_159C / 8000_15BC

Bit	R/W	Description	Default Value
31 : 22	R	Reserved	-
21	RW	Uncountable Auto Reload If this bit is set, Auto Reload is operated regardless of Auto Reload Count..	
20 : 0	RW	Auto Reload Count User can specify Auto Reload Count to this bits and can repeat DMA Transfer. The Auto Reload count is decreased when Block transfer is finished (Transfer Size becomes 0). If the value becomes 0, Auto Reload Operation is finished.	0

15.5 Program Guide

15.5.1 Sumary of Register

Name	Address	Type	Description
DMAIntStatus	0x000	R	DMA Interrupt Status
DMATCIntStatus	0x004	R	DMA Terminal Count Interrupt Status
DMATCIntClr	0x008	W	DMA Terminal Count Interrupt Clear
DMAErrorIntStatus	0x00C	R	DMA Error Interrupt Status
DMAErrorIntClr	0x010	W	DMA Error Interrupt Clear
DMABlockIntStatus	0x014	R	DMA Block Interrupt Status
DMABlockIntClr	0x018	W	DMA Block Interrupt Clear
DMARawTCIntStatus	0x01C	R	DMA Raw Terminal Count Interrupt Status
DMARawErrorIntStatus	0x020	W	DMA Raw Error Interrupt Status
DMAEnbldChns	0x024	R	DMA Enabled Channels
DMASoftBReq	0x028	RW	DMA Software Burst Request
DMASoftSReq	0x02C	RW	DMA Software Single Request
DMASoftLBReq	0x030	RW	DMA Software Last Burst Request
DMASoftLSReq	0x034	RW	DMA Software Last Single Request
ChnSrcAddr	0x100	RW	Channel Source Address
ChnDestAddr	0x104	RW	Channel Destination Address
ChnLLI	0x108	RW	Channel Linked List Item
ChnCntl	0x10C	RW	Channel Control
ChnCfg	0x110	RW	Channel Configuration
ChnSrcGaAddr	0x114	RW	Channel Source Gather Address
ChnDestScatAddr	0x118	RW	Channel Destination Scatter Address
ChnAutoReloadCnt	0x11C	RW	Channel Auto Reload Count

15.5.2 Programming Sequence

- **DMA Operation (Memory to Memory)**
- Choose a channel to transfer
- Configures Source Address of the channel (ChnSrcAddr Register)
- Configures Destination Address of the channel (ChnDstAddr Register)
- Configures Transfer Width of source and destination (ChnCntl Register)
- Configures Burst Size of source and destination (ChnCntl Register)
- Configures Transfer Size (DMA Transfer size) (ChnCntl Register)
- Enables the Channel (ChnCfg Register)
- Check the DMA Transfer is finished (DMAEnbldChns Register)
- Finish

- **DMA Operation (Memory to Peripheral)**
  1. Choose a channel to transfer
  2. Configures Source Address of the channel (ChnSrcAddr Register)
  3. Configures Destination Address of the channel (ChnDstAddr Register)
  4. Configures Transfer Width of source and destination (ChnCntl Register)
  5. Configures Burst Size of source and destination (ChnCntl Register)
  6. Configures Transfer Size (DMA Transfer size) (ChnCntl Register)
  7. Configures Transfer Type (ChnCfg Register)
  8. Enables the Channel (ChnCfg Register)
  9. Check the DMA Transfer is finished (DMAEnbldChns Register)
  10. Finsh

- **Linked List Operation (Memory to Memory)**
  Assumes that the Linked List Item is already prepared.
  1. Choose a channel to operate
  2. Configures the first LLI address (ChnLLI Register)
  3. Enables the channel (ChnCgf Register)
  4. Checks the operation is finished (DMAEnbldChns Register)
  5. Finish

- **Auto Reload Operation Program (Memory to Memory)**
- Choose a channel to operate
- Configures Source Address of the channel (ChnSrcAddr Register)
- Configures Destination Address of the channel (ChnDstAddr Register)
- Configures Transfer Width of source and Destination (ChnCntl Register)
- Configures Burst Size of source and destination (ChnCntl Register)
- Configures Transfer Size (DMA Transfer size) (ChnCntl Register)
- Specifies Auto Reload Size (ChnAutoReloadCnt Register)
- Enables the Channel (ChnCfg Register)
- Check the DMA Transfer is finished (DMAEnbldChns Register)
- Finsh

15.5.3 Program Consideration

User program should consider following restrictions.

1. User should not change the channel's register value after the channel is enabled. Because DMA Transfer is operated after the channel is enabled, modifying register value may induce problem. Due to that reason, user should check whether the channel is enabled or disabled to modify register value.

2. DMA Transfer size is set to times of Destination transfer width if source transfer width is smaller than destination transfer width. DMA Transfer size is calculated with the size of read data in source (Source width x Transfer size). If the DMA Transfer size does not match with Destination width x N, the size of written data in destination is smaller or larger.

3. Linked List Item does not allocate in address 0x0.

16 LOCAL MEMORY CONTROLLER

16.1 Register Description

16.1.1 SDRAM Control Register (MEMCON)

Address : 0x8000_0400

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 8	R	Reserved	-
7 : 6	R/W	Row Address Line Number 00 : 11 bit 01 : 12 bit 10 : 13 bit 11 : 14 bit	11b
5 : 4	R/W	Column Address Line Number 00 : 8 bit 01 : 9 bit 10 : 10 bit 11 : 11 bit	11b
3	R/W	Timing Constraint Select (0 : Upper 100MHz, 1 : Under 100 MHz) 0 : tRCD = 3 Clock, tRP = 3 Clock, tRAS = 7 Clock, tRC = 10 Clock 1 : tRCD = 2 Clock, tRP = 2 Clock, tRAS = 5 Clock, tRC = 7 Clock	0b
2	R/W	CAS Latency 0 : 2 Clock 1 : 3 Clock	0b
1 : 0	R/W	This bit determine data bus width 00 : 8 bit 01 : 16 bit 10 : 32 bit 11 : Reserved	01b

< Register Bit field description >

1. Bit [7:6]: Selects the number of SDRAM Row Address.
2. Bit [5:4]: Selects the number of SDRAM Column Address.
3. Bit [3]: It determines Timing condition to operate SDRAM.
   If the clock frequency is upper 100MHz, the bit is set to 0, otherwise 1.
4. Bit [2]: Selects CAS Latency Cycle of SDRAM operation.
5. Bit [1:0]: It determines SRAM Data Bus Width of its bank.

16.1.2 SDRAM Clock Delay Register (MEMCLKCON)

Address : 0x8000_0404h

Bit	R/W	Description	Default Value
31 : 12	R	Reserved	-
11 : 8	R/W	Local SDRAM Clock Generation (Clock delay) 0000 : CLOCK 1000 : Invert CLOCK 0001 : CLOCK+1ns 1001 : Invert CLOCK+1ns 0010 : CLOCK+2n 1010 : Invert CLOCK+2ns 0011 : CLOCK+3ns 1011 : Invert CLOCK+3ns 0100 : CLOCK+4ns 1100 : Invert CLOCK+4ns 0101 : CLOCK+5ns 1101 : Invert CLOCK+5ns 0110 : CLOCK+6ns 1110 : Invert CLOCK+6ns 0111 : CLOCK+7ns 1111 : Invert CLOCK+7ns	0h
7 : 0	R/W	1Mhz Clock generation Divider Value	FFh

< Register bit field description >

1. Bit [11:8]: It determines delay of SDRAM Feedback Clock for SDRAM Data read operation.
2. Bit [7:0]: It configures Clock generation Divider value to generate1MHz frequency. Because its value is (Main Clock/(n+1)), divider value should be set to n-1.

16.1.3 SDRAM Refresh Control Register (MEMREFCON)

Address : 0x8000_0408h

Bit	*R/W*	*Description*	*Default Value*
31 : 10	R	Reserved	-
9	R/W	Refresh Period < Refresh Source : 1Mhz > 0 : 15 usec 1 : 30 usec	0b
8	R/W	Number of Refresh Cycle / Period < Refresh Source : 1Mhz > 0 : 1 Cycle 1 : 2 Cycle	0b
7 : 1	R	Reserved	-
0	R/W	0: Auto Refresh 1: Self Refresh	0b

< Register bit field description >

1. Bit [9]: It determines Refresh Period when Refresh Source frequency is 1MHz.
2. Bit [8]: It determines the number refresh cycle per period.
3. Bit [0]: Refresh Mode Select.

17 NAND FLASH CONTROLLER

NAND Flash controls data transfer of 8-bit I/O NAND Flash Memory.

17.1 Features

- 8bit I/O support
- 3-cycle/4-cycle/5-cycle Address support
- 1bit for SLC and 4bit/24bit ECC for MLC
- Auto ECC Decoding support

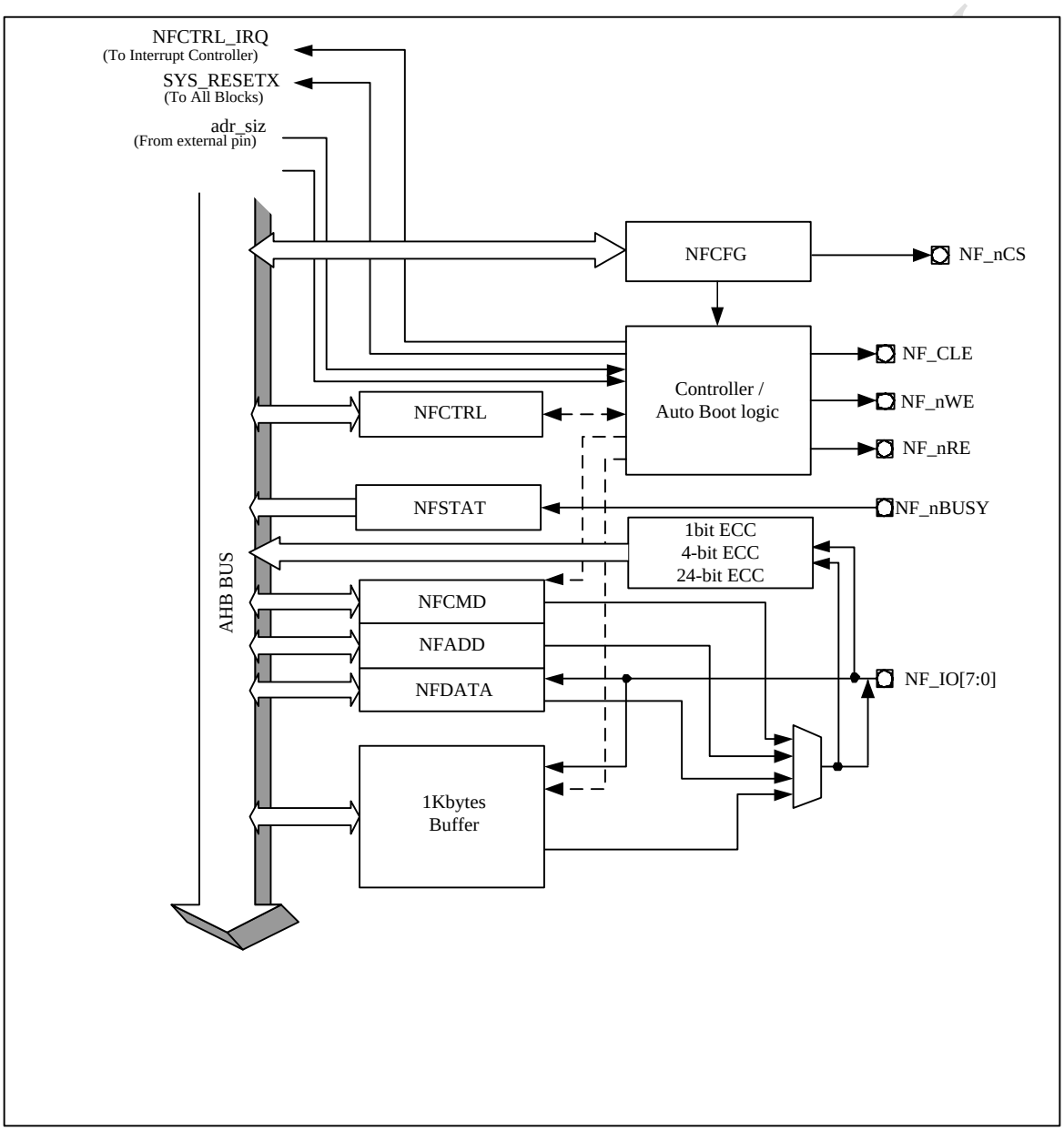


Figure 17-1 NAND Flash Controller Block Diagram

17.2 Functional Description

17.2.1 Data Read/Write

1. Configures timing for data transfer to NFCFG register.
2. Configures NAND Flash Memory Command to NFCMD register.
3. Configures NAND Flash Memory address for access to NFADR register. At that time, repeatedly configures the register as Address cycle to NAND Flash access.
4. Operates Read/Write by NFCPUDATA. Before/After read data, user should check NDFL_nBUSY.

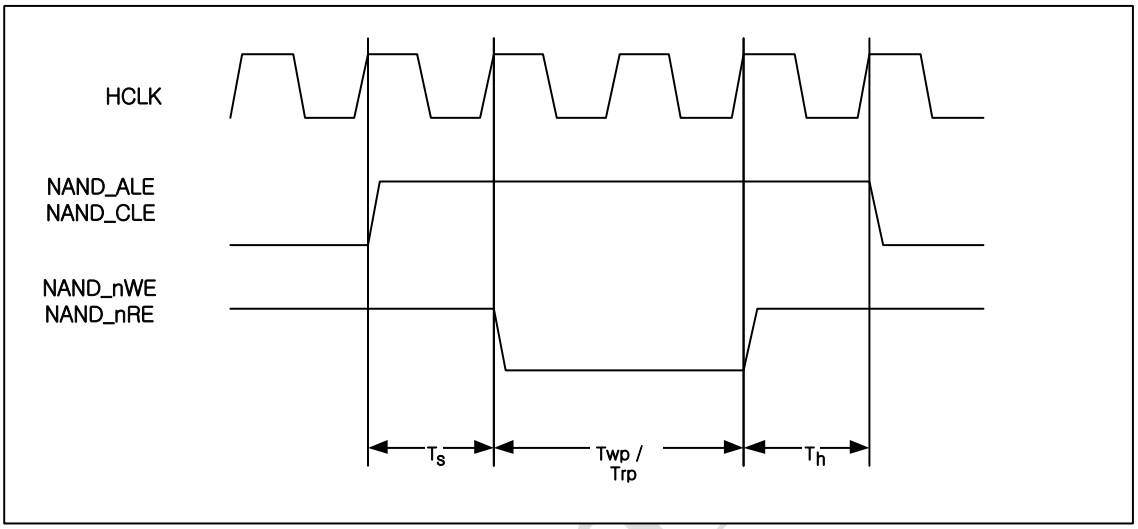


Figure 17-2 Read/Write Timing Diagram of NAND Flash Memory

17.2.2 DMA Operation

NAND Flash controller supports DMA Data Transfer. First of all, configures DMA Controller, then configures NAND Flash controller. If User configures DMA operation by NFCTRL register, NAND Flash Memory starts to DMA data transfer. In the case of the NAND Flash Memory is Large type (second generation), user can configures maximum 2Kbytes data transfer unit. In the case of the NAND Flash Memory is Small type (first generation), user can configures maximum 512Bytes for data transfer

17.3 ECC Operation

adStar-L provides not only SLC type, but MLC type NAND Flash. Because MLC type NAND Flash has higher error probability than SLC type, programmer should correct the error.

NAND Flash Controller generates Parity bit by using BCH algorithm. With the parity bit, *adStar-L* can correct data error. *adStar-L* provides error detection and error correction in 4-bit error for 512Bytes data and 24-bit error for 1Kbytes data.

17.3.1 ECC Encoding

1. After configures NFCFG register to use NAND Flash, Command and Address are sent.
2. After read NFECC1 register, clears ECC status and ECC registers.
3. Set ECC GEN bit of NFCTRL register to 1. (ECC Generation Enable)
4. Send 512Bytes or 1024Bytes data. Whenever data is transmitted, 52-bit or 336-bit Parity bits are generated and stored into NFECCn registers.
5. After finish sending data, reads the data in the order of NFECC0 register, NFECC1 register and stores into memory.
6. In order to continue to 512Bytes or 1024Bytes data transfer, repeats step 2~5.
7. If the1-page data transfer is finished, sets ECC GEN bit of NFCTRL register to 1. (ECC Generation disable)
8. Stores Parity bits of 512Bytes or 1024Bytes data in memory into spare space of NAND Flash.

17.3.2 ECC Decoding by S/W

1. After configures NFCFG register to use NAND Flash, Command and Address are sent.
2. After read NFECC1 register, clears ECC status and ECC registers.
3. Selects 4-bit or 24-bit ECC mode form NFCTRL register, then sets ECC GEN bit to 1. (ECC Decoding enable)
4. Reads 512Bytes or 1024Bytes data.
5. After read the data, accesses spare space and read parity bits.
6. After read the parity bits, automatically starts decoding. User can check the decoding is finished and succeeded by read NFSTAT register.
7. After finish decoding, NFERRLOC0~3 or NFERRLOC23 register holds error location, and NFERRPTN0~3 or NFERRPTN23 register holds 8-bit error pattern.
8. Correcting error data by Exclusive-OR Error location of NFERRLOCn register and error pattern of NFERRPTNn.
9. Repeats step 2~8 until finish reading 1-page.

17.3.3 ECC Decoding by H/W (Auto ECC Decoding)

1. After configures NFCFG register to use NAND Flash, Command and Address are sent.
2. After read NFECC10 register, clears ECC status and ECC registers.
3. Selects 4-bit or 24-bit ECC mode from NFCTRL register, and set Auto ECC Decode bit to 1, then automatically reads data and parity from NAND Flash.
4. Check the Auto ECC Done bit of NFSTAT register is 1.
5. Reads error correction data from NFECD register

Repeats step 2~5 until finish reading 1-page.

17.4 Register Description

17.4.1 NAND Flash Memory Control Register (NFCTRL)

Address: 0xA000_0C00

Bit	R/W	Description	Default Value
31:17	R	Reserved	-
16	R/W	Auto ECC Enable bit 0: Auto ECC done 1: Auto ECC Start If the bit is set, Auto ECC is stated, and automatically clear when finished.	0
15	R/W	4-bit ECC Mode Set bit 0: 24-bit ECC Mode 1: 4-bit ECC Mode	1
14:13	R	Reserved	-
12	R/W	ECC Generation Enable bit 0 : Disable 1 : Enable	0
11	R/W	Endian Select bit 0 : Little Endian 1 : Big Endian	0
10	R/W	Data Swap Size 0 : 8bit 1 : 16bit	0
9	R/W	DMA Write Request bit 0 : DMA Write Request Clear 1 : DMA Write Request If the bit is set, DMA Transfer is stated, and automatically clear when finished.	0
8	R/W	DMA Read Request bit 0 : DMA Read Request Clear 1 : DMA Read Request If the bit is set, DMA Transfer is stated, and automatically clear when finished.	0
7	R/W	Busy End Interrupt Enable bit 0 : Interrupt Disable 1 : Interrupt Enable	0
6	R/W	DMA Clear Interrupt Enable bit 0 : Interrupt Disable 1 : Interrupt Enable	0
5	R/W	BCH ECC Decoding Done Interrupt Enable bit 0 : Interrupt Disable 1 : Interrupt Enable	0
4	R/W	Auto ECC Done Interrupt Enable bit 0 : Interrupt Disable 1 : Interrupt Enable	0
3:0	R/W	Reserved	0

17.4.2 NAND Flash Memory Command Set Register (NFCMD)

Address: 0xA000_0C04

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R/W	NAND Flash Memory Command	00h

17.4.3 NAND Flash Memory Address Register (NFADR)

Address: 0xA000_0C08

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R/W	NAND Flash Memory Address	00h

17.4.4 NAND Flash Memory Data Register (NFDATA)

Address: 0xA000_0C0C

Bit	R/W	Description	Default Value
31 : 0	R/W	NAND Flash Memory Read/Program Data 32/16/8-bit accessible	0000_0000h

17.4.5 NAND Flash Memory Operation Status Register (NFSTAT)

Address: 0xA000_0C14

Bit	R/W	Description	Default Value
31 : 17	R	Reserved	-
16:12	R	Error bit count The number of Error bit when ECC is finished.	0
11	R	Read data not FF Flag After erase, this bit is used for check all data for NAND Flash is 0xFF. If the read data is not 0xFF, this bit is set to 1. After read the register, this bit is cleared.	0
10	R	Reserved	-
9	R	DMA Write Done It is set when DMA Write is finished. After read the register, this bit is cleared.	0
8	R	DMA Read Done It is set when DMA Read is finished. After read the register, this bit is cleared.	0
7	R	BCH Decoding Done Status It is set when ECC Decoding is finished. After read the register, this bit is cleared.	0
6 : 4	R	Reserved	-
3	R	BCH Decoding Result 0 : Decoding Fail 1 : Decoding Success	0
2	R	Auto ECC Done bit If the value of the bit is set, it indicates Auto ECC is finished. After read the register, this bit is cleared.	0
1	R	NAND Flash Memory nBusy Level 0 : Busy 1 : Ready	nBUSY Level
0	R	NAND Flash Memory Busyx Rising Edge Status If Ready/Busyx signal changes low to high, this bit is set to 1. After read the register, this bit is cleared.	0

17.4.6 NAND Flash Memory ECC(Error Correction Code) Register (NFECC)

Address: 0xA000_0C18

Bit	R/W	Description	Default Value
31 : 24	R	Reserved	-
23 : 16	R/Clear	ECC2 (~P4, ~P4', ~P2, ~P2', ~P1, ~P1', ~P2048, ~P2048')	FFh
15 : 8	R/Clear	ECC1 (~P1024, ~P1024', ~P512, ~P512', ~P256, ~P256', ~P128, ~P128')	FFh
7 : 0	R/Clear	ECC0 (~P64, ~P64', ~P32, ~P32', ~P16, ~P16', ~P8, ~P8')	FFh

***** P1~P4 : Column Parity , P8~P2048 : Row Parity

* ~ : Logically inverse operation

17.4.7 NAND Flash Memory Configuration Register (NFCFG)

Address: 0xA000_0C1C

Bit	R/W	Description	Default Value
31 : 21	R	Reserved	-
20	R/w	Read data Latch timing Adjust bit. Configure as system clock. 0 : Minimum ~ 60Mhz 1 : 40Mhz ~ Maximum	1
19 : 17	R	Reserved	-
16	R/W	NDFL_nCS Control 0 : Chip Enable 1 : Chip Disable	1
15	R	Reserved	-
14 : 12	R/W	Ts : NDFL_ALE/NDFL_CLE Set-up Time 000 : 1 Clock 001 : 2 Clocks 010 : 3 Clocks 011 : 4 Clocks 100 : 5 Clocks 101 : 6 Clocks 110 : 7 Clocks 111 : 8 Clocks	111
11	R	Reserved	-
10 : 8	R/W	Twp : NDFL_nWE Pulse Width 000 : 1 Clock 001 : 2 Clocks 010 : 3 Clocks 011 : 4 Clocks 100 : 5 Clocks 101 : 6 Clocks 110 : 7 Clocks 111 : 8 Clocks	111
7	R	Reserved	-
6 : 4	R/W	Trp : NDFL_nRE Pulse Width 000 : 1 Clock 001 : 2 Clocks 010 : 3 Clocks 011 : 4 Clocks 100 : 5 Clocks 101 : 6 Clocks 110 : 7 Clocks 111 : 8 Clocks	111
3	R	Reserved	-
2 : 0	R/W	Th : NDFL_ALE/ NDFL_CLE/ NDFL_nCS Hold Time 000 : 1 Clock 001 : 2 Clocks 010 : 3 Clocks 011 : 4 Clocks 100 : 5 Clocks 101 : 6 Clocks 110 : 7 Clocks 111 : 8 Clocks	111

17.4.8 NAND Flash Memory ECC Code for LSN data (NFECCL)

Address: 0xA000_0C20

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 8	R	S_ECC1 (1, 1, 1, 1, 1, 1, ~P4_s, ~P4'_s)	FFh
7 : 0	R	S_ECC0 (~P2_s, ~P2'_s, ~P1_s, ~P1'_s, ~P16_s, ~P16'_s, ~P8_s, ~P8'_s)	FFh

* P1_s~P4_s : Column Parity, P8_s~P16_s : Row Parity
* ~ : Logically inverse operation

17.4.9 NAND Flash Memory Error Corrected Data Register (NFECD)

Address: 0xA000_0C24

Bit	R/W	Description	Default Value
31 : 0	R	Automatically Error Corrected Data	-

17.4.10 NAND Flash Memory Spare Address Register (NFSPADR)

Address: 0xA000_0C28

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 0	R/W	Spare address to access during Auto ECC	0000h

17.4.11 NAND Flash Memory MLC ECCn Register (NFECCn)

Address: 0xA000_0C2C / 0xA000_0C30 / 0xA000_0C34 / 0xA000_0C38 / 0xA000_0C3C / 0xA000_0C40 / 0xA000_0C44 / 0xA000_0C48 / 0xA000_0C4C / 0xA000_0C50 / 0xA000_0C54

Bit	R/W	Description	Default Value
31 : 0	R	4-bit ECC Parity Value 52-bit parity[31:0] / 52-bit parity[52:32] 24-bit ECC Parity Value 336-bit parity[31:0] , 336-bit parity[63:32], 336-bit parity[95:64] , 336-bit parity[127:96], 336-bit parity[159:128], 336-bit parity[191:160], 336-bit parity[223:192], 336-bit parity[255:224], 336-bit parity[287:256], 336-bit parity[319:288], 336-bit parity[335:320]	0000_0000h

17.4.12 NAND Flash Memory Error Location n Register (NFERRLOCn)

Address: 0xA000_0C58 / 0xA000_0C5C / 0xA000_0C60 / 0xA000_0C64 / 0xA000_0C68 / 0xA000_0C6C / 0xA000_0C70 / 0xA000_0C74 / 0xA000_0C78 / 0xA000_0C7C / 0xA000_0C80 / 0xA000_0C84 / 0xA000_0C88 / 0xA000_0C8C / 0xA000_0C90 / 0xA000_0C94 / 0xA000_0C98 / 0xA000_0C9C / 0xA000_0CA0 / 0xA000_0CA4 / 0xA000_0CA8 / 0xA000_0CAC / 0xA000_0CB0 / 0xA000_0CB4

Bit	R/W	Description	Default Value
31 : 11	R	Reserved	-
10 : 0	R	Error byte location 1st~24th	0000h

17.4.13 NAND Flash Memory Error Pattern n Register (NFERRPTNn)

Address: 0xA000_0CB8 ~ 0xA000_0D14

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R	Error byte pattern 1st~24th	00h

17.4.14 NAND Flash Memory ID Register (NFMID)

Address: 0xA000_0D18

Bit	R/W	Description	Default Value
31 : 0	R	NAND Flash ID	0000_0000h

18 SD HOST CONTROLLER

18.1 Features

- Support SD (ver 2.0) / MMC (ver 3.31) cards
- Provides High Speed (50MHz)
- Supports 1bit/4bit data bus
- Supports DMA Transfer
- Embeds 64 byte FIFO
- 40-bit Command Register
- 136-bit Response Register

18.2 Block Diagram

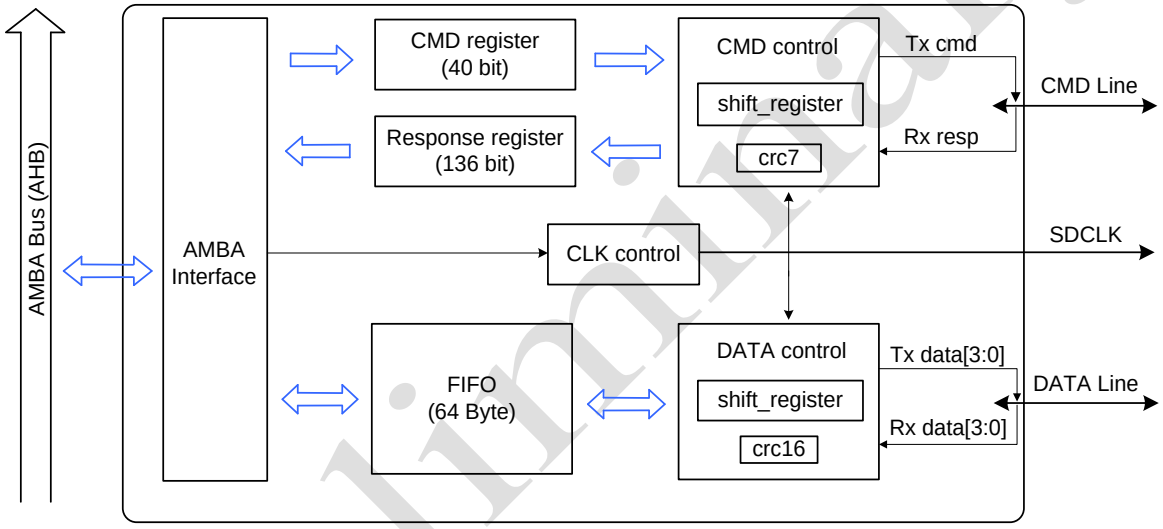


Figure 18-1 SDHC Block Diagram

18.3 SD Card Protocol

Communication between SD card and SD host is started with start bit and is stopped with stop bit based on Command, response, and data.

Command: Host (Controller) sends command line to SD Card. The commands can be categorized as Broadcast command that transfers data to multiple SD card, and Addressed command that transfers data to one SD cared.

Response: A response of host command. The selected SD Card send the response with command line.

Data: The data is sent from SD card to SD card or from SD card to host with Data line in the unit of Block. Generally the block size is 512byte or 1024byte.

For reliability of data transfer, SD Card protocol checks Command, Response, and Data within CRC7 and CRC16. The CRC code generation and error detection is automatically done by H/W.

18.4 Register Description

18.4.1 SDHC Control Register (SDHCCON)

Address : 0xA000_1000h

Bit	R/W	Description	Default Value
31 : 6	R	Reserved	-
5	R/W	MMC/SD HC Enable 0 : Disable (Controller is initialized) 1 : Enable Enable bit for HOST. If this bit is disabled, the status of controller is initialized and inside buffers are cleared.	0b
4 : 3	R/W	Memory access type 00 : byte align 01 : short align 10 : word align 11 : not use This bit determines alignment of data that stored in SD card.	00b
2	R/W	DMA mode selection 0 : Normal mode (data transfer by CPU) 1 : DMA mode (data transfer by DMA) Provides high speed data transfer via DMA.	0b
1	R/W	Bus width Selection 0 : 1bit data bus 1 : 4bit data bus	0b
0	R/W	MMC/SD clock enable 0 : Disable 1 : Enable	0b

18.4.2 SDHC Status Register (SDHCSTAT)

Address: 0xA000_1004h

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15	R	Card_Insertion 0 : No card insertion detection 1 : card insert detected This bit indicates that SD Card is inserted into a slot via Data line [3]. To use the bit, data line[3] should be connected with weak-pull-down resistance.	0b
14	R	Card_Removal 0 : No card removal detection 1 : card remove detected This bit indicates that SD Cared is removed from a slot via Data line [3].	0b
13	R	FIFO full This bit indicates 64-byte data FIFO is full or not.	0b
12	R	FIFO half full This bit indicates 64-byte data FIFO is half full.	0b
11	R	FIFO empty This bit indicates 64-byte data FIFO is empty.	1b
10	R/C	Command & response transaction done 0 : Command and response transaction is in progress 1 : Command and response transaction is done This bit informs that SD card received response when Host sent command. If the response does not reach, this bit is set to 1 by occurring Time out error.	0b
9	R/C	Data Write operation done 0 : Write operation is in progress or incomplete 1 : Write operation complete This bit informs that Data write operation is done. In the case of Data CRC error is occurred, the write operation is finished and then this bit is set to 1.	0b
8	R/C	Read operation done 0 : Read operation is in progress or incomplete 1 : Read operation complete This bit informs that Data write operation is done. In the case of Read Data CRC error is occurred, the read operation is finished and then this bit is set to 1.	0b
7 :6	R/C	Write CRC error code 00 : No CRC Error 01 : CRC Error (CRC error in data block) 10 : No CRC response (Ignored data block in SD card) 11 : Reserved During write operation, this bit informs CRC test result from SD Card. SD Card test CRC every time when Host sends one block data and send the result of CRC to the Host.	00b
5	R/C	Response CRC error 0 : No error 1 : Response CRC error occurred This bit informs CRC error occurred in response.	0b
4	R/C	Read data CRC error 0 : No error 1 : Read data CRC error occurred This bit informs that CRC error occured in read data from SD Card.	0b
3	R/C	Write data CRC error 0 : No error 1 : Write data CRC error occurred This bit informs that CRC error occured in write data to SD Card.	0b
2	R/C	Response time out error 0 : No error 1 : Command response was not received in time Specified This bit informs that command response is not received in time.	0b
1	R/C	Read data time out error 0 : No error 1 : The expected data from card was not received in time Specified This bit informs that read data from SD card is not received in time.	0b
0	R	Memory busy state 0 : Memory is ready 1 : Memory is busy This bit indicates busy status of SD Card.	0b

R/C indicates Read/Clear. In order to clear specific bit of status, writes 1 to corresponding bit.
Status [15:8] is an interrupt source. If one of the bits is set to 1, an interrupt is occurred and keeps requesting interrupt until the bit is cleared.

18.4.3 SDHC Clock Divide Register (SDHCCD)

Address : 0xA000_1008h

Bit	R/W	Description	Default Value
31 : 10	R	Reserved.	-
9 : 0	R/W	MMC/SD clock Divide Register $f_{SDCLK} = \frac{f_{AHB\_Clock}}{2 + Divide\ [9:0]}$	200h

18.4.4 SDHC Response Time Out Register (SDHCRTO)

Address: 0xA000_100Ch

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R/W	Response time out. This register is configured in maximum wait time for response after sending command. If the response does not reach in the specified time, response time out error is occurred. The unit of time is based on the clock of SD Card, and if the last bit of command is transferred, the clock count begins. 01h : 1 clock count 02h : 2 clock counts ... FFh : 255 clock counts	FFh

18.4.5 SDHC Read Data Time Out Register (SDHCRDTO)

Address: 0xA000_1010h

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 8	R/W	Data read time out. This register is configured in maximum wait time for read data after sending read command. User can configure upper 8-bit and lower 8-bit is fixed with 00h. Generally, FF00h is recommended.	FFh
7 : 0	R	Reserved.	00h

18.4.6 SDHC Block Length Register (SDHCBL)

Address: 0xA000_1014h

Bit	R/W	Description	Default Value
31 : 12	R	Reserved	-
11 : 0	R/W	Block length. This register determines the size of data block.	200h

18.4.7 SDHC Number of Block Register (SDHCNOB)

Address: 0xA000_1018h

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 0	R/W	This register specifies the number of blocks to transfer when using Multi-block command. Its value is decreased when one block is transferred and if the data transfer is finished, the value becomes 0.	0000h

18.4.8 SDHC Interrupt Enable Register (SDHCIE)

Address : 0xA000_101Ch

Bit	R/W	Description	Default Value
31 : 8		Reserved	-
7	R/W	Card insert detection Interrupt enable 0 : disable 1 : enable	0b
6	R/W	Card remove detection Interrupt enable 0 : disable 1 : enable	0b
5	R/W	FIFO full Interrupt enable 0 : disable 1 : enable	0b
4	R/W	FIFO half full Interrupt enable 0 : disable 1 : enable	0b
3	R/W	FIFO empty Interrupt enable 0 : disable 1 : enable	0b
2	R/W	End command response Interrupt enable 0 : disable 1 : enable	0b
1	R/W	Write operation done Interrupt enable 0 : disable 1 : enable	0b
0	R/W	Read operation done Interrupt enable 0 : disable 1 : enable	0b

SDHCSTAT [15:8] is an interrupt source, and SDHCIE register is an interrupt enable signal. If an interrupt is occurred, interrupt service routine is executed and sets to 0 in SDHCSTAT [15:8] according to the interrupt source. However, because card insert detection interrupt and card remove detection interrupt are not cleared in SDHCSTAT [15] and SDHCSTAT [14], interrupt enable bit is set to 0 in the interrupt service routine (Interrupt disable).

18.4.9 SDHC Command Control Register (SDHCCMDCON)

SDHCCMDCON register is used for sending command. Once user writes to SDHCCMDCON register, user command is sent to SD card as the register configuration.

Address: 0xA000_1020h

Bit	R/W	Description	Default Value
31 : 11	R	Reserved	-
10	R/W	This bit determines that a command type needs response or not. In the case of the configuration is No response, response does not be stored into response buffer. 0 : no response 1 : wait response	0b
9 : 8	R/W	This bit determines response type. Because the response type can be changed according to the command, user should select the right response type. 00 : short response (response size : 48bit) 01 : short response with busy (response size : 48bit ,) 10 : long response (response size : 136bit)	00b
7	R/W	This bit determines a command uses data stream or not. In the case of read command or write command, this bit should be 1. 0 : without data 1 : with data	0b
6	R/W	This bit determines a direction of Data FIFO In/Out. In the case of read command, the bit is set to 0. In the case of write command, the bit is set to 1. 0 : read data 1 : write data	0b
5 : 0	R/W	This bit specifies command number. The command number of MMC and SD card is different. Refer to MMC and SD Card specification. 00h = CMD0 01h = CMD1 ... 3Fh = CMD63	00h

18.4.10 SDHC Command Argument Register (SDHCCMDA)

Address: 0xA000_1024h

Bit	R/W	Description	Default Value
31 : 0	R/W	Command argument. It configures argument of command token.	0000 0000h

18.4.11 SDHC Response FIFO Access Register (SDHCRFA)

Address: 0xA000_1028h

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 0	R/W	FIFO size to store response. the size is 8x16 bit.	0000h

18.4.12 SDHC Data FIFO Access Register (SDHCDFA)

Address: 0xA000_102Ch

Bit	R/W	Description	Default Value
31 : 0	R/W	Data FIFO size. (16x32bit)	-

19 SPI LCD CONTROLLER

19.1 Features

- Support Normal SPI transfer with 9bit
  (Not support falling SCK data sampling)
- Support bidirectional SDO mode for 3 wire transaction
- Support 24 bit format color and 32bit reserved format color
- External clock for SCK
- 16byte FIFO for Tx , Rx data

19.2 Register Description

19.2.1 SPI LCD control Register (CTRL)

Address : 0xA000_0800

Bit	*R/W*	*Description*	*Default Value*
31 : 8	R	Reserved	-
7	R/W	Enable : Operation Enable 0 : Operation is disabled. 1 : Operation is enabled	0
6	R/W	SDO Direction 0 : Output 1 : Input	0
5	R/W	Lower Byte First If this bit is set, the lower byte of 16bit, 24bit, 32bit are transmitted.	0
4	R/W	SCK Polarity	0
3	R/W	Level of D/C bit	0
2	R/W	Transmit mode 0 : 8bit transmit 1 : 9 bit transmit (add D/C bit to MSB)	0
1 : 0	R/W	Data Size 0 : 8 bit data transfer. 1 : 16 bit data transfer. 2 : 24 bit data transfer, 3 : 32 bit data transfer, If configured 24 bit data transfer mode, it read 32 bit data and transfer lower 24 bit.	1

- Connection with LCD module in 8 bit mode

Figure 19-1 8bit mode pin connection

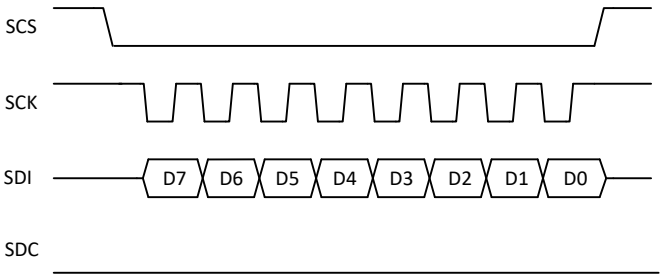


Figure 19-2 8bit mode timing diagram

- Connection with LCD module in 9 bit mode

Figure 19-3 9bit mode pin connection

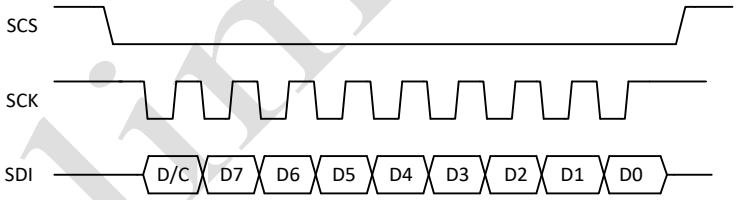


Figure 19-4 9bit Mode timing diagram

19.2.2 SPI LCD Baud Rate Register (BAUD)

Address : 0xA000_0804

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7 : 0	R/W	Serial Clock Baud Rate $SCK = \frac{f_{DOTCLK}}{2 \times (SPIBR + 1)}$	0xFF

19.2.3 SPI LCD DMA Configuration Register (SPI_LCD_DMA)

Address : 0xA000_0808

Bit	R/W	Description	Default Value
31 : 1	R	Reserved	-
0	RW	DMA Enable The transmission rate of the DMA is configured by trans count of DMA block.	0

19.2.4 SPI LCD ChipSelect Register (CSx)

Address : 0xA000_0810

Bit	R/W	Description	Default Value
31 : 1	R	Reserved	-
0	RW	CSx : CSx Output Level	1

19.2.5 SPI LCD Status Register (SPI_LCD_STAT)

Address : 0xA000_0814

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	R	SPIF : SPI Finished Flag 0 : Transfer is not finished. 1 : Transfer is finished.	0
6	R	STXHF : Tx FIFO Is Half Empty 0 : The Empty space is less than Half 1 : The Empty space is more than Half	0
5	R	STXF : TX FIFO Full Status bit 0 : TX FIFO is not full 1 : TX FIFO is full	0
4	R	STXE : TX FIFO Empty Status bit 0 : TX FIFO is not empty 1 : TX FIFO is empty	0
3	R	Reserved	0
2	R	SRXHF : RX FIFO Half Full Status bit 0 : The Remain Data in Rx FIFO is less than Half 1 : The Remain Data in Rx FIFO is more than Half	0
1	R	SRXF : RX FIFO Full Status bit 0 : FIFO_RX is not full 1 : FIFO_RX is full	0
0	R	SRXE : RX FIFO Empty Status bit 0 : FIFO_RX is not empty 1 : FIFO_RX is empty	0

19.2.6 LCD Data Register (SPI_LCD_DATA)

Address : 0xA000_0818

Bit	R/W	Description	Default Value
31 : 0	R/W	16 byte FIFO It is possible to access with 8, 16, 32 bit	0x0000_0000

19.2.7 LCD Interrupt Mask Register (SPI_LCD_INT)

Address : 0xA000_081C

Bit	R/W	Description	Default Value
31 : 8	R/W	Reserved	-
7	R/W	SPIF : SPI finished Interrupt enable	0
6	R/W	STXHF : Tx fifo half empty interrupt enable	0
5	R/W	STXF : Tx fifo full status interrupt enable	0
4	R/W	STXE : Tx fifo empty status Interrupt enable	0
3	R/W	Reserved	0
2	R/W	STXHF : Rx fifo half full interrupt enable	0
1	R/W	SRXF : Rx fifo Full interrupt enable	0
0	R/W	SRXE : Rx fifo empty interrupt enable	0

20 SPI (SERIAL PERIPHERAL INTERFACE)

adStar-L includes SPI which exchanges data with external devices and other CPUs through synchronized serial bus. This SPI is compatible with the SPI of M16HC11, M68HC05, and MC68HC16 series of Motorola, and supports full duplex 3-wire or half duplex 2-wire transmission.

For high speed SPI transmission, the SPI of adStar-L has FIFO of 8 bytes. The FIFO allows several Mbps of transmission rate without imposing overhead on CPU.

The SPI of *adStar-L* supports both master mode and slave mode.

20.1 Features

- Full duplex mode. Three-wired synchronous Transfer
- Master or Slave Operation
- Programmable clock polarity and phase
- End of transmission interrupt flag
- Write collision flag protection
- Master-master mode fault protection capability
- 8Bytes FIFO

20.2 Block Diagram

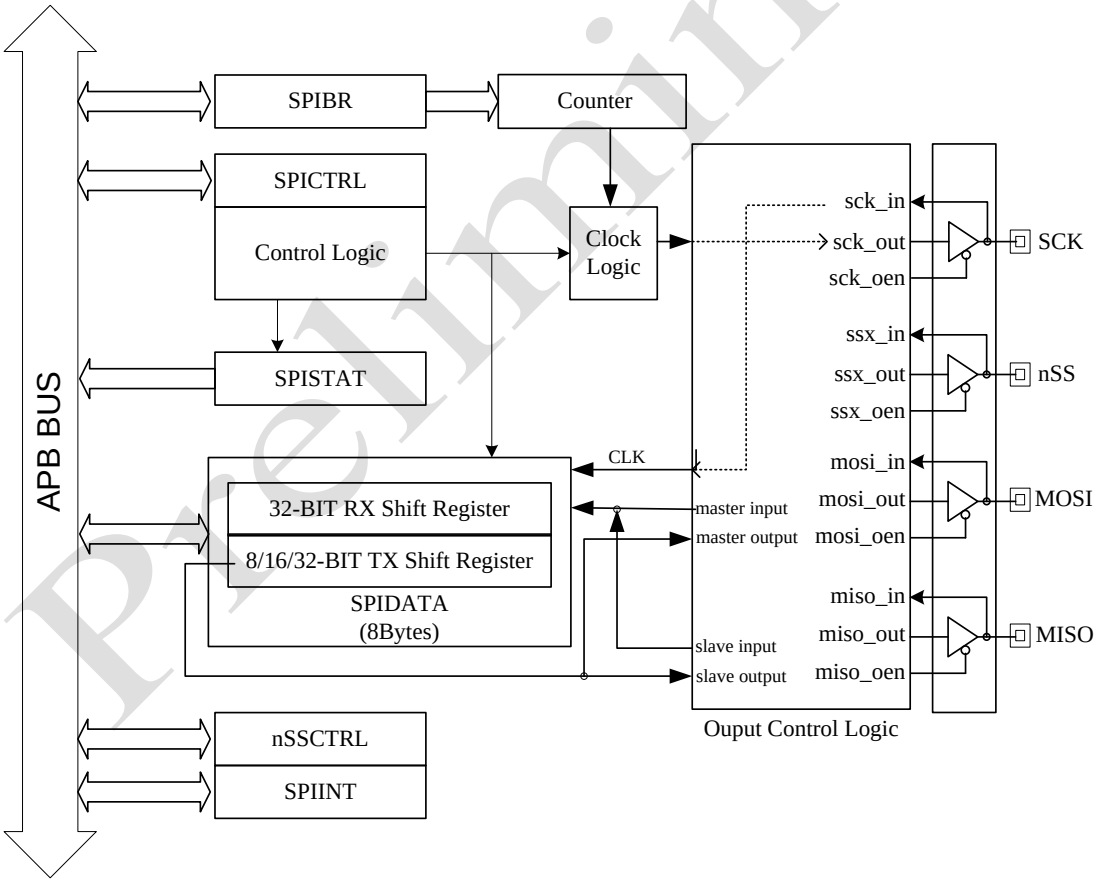


Figure 20-1 SPI Block Diagram

20.3 Functional Description

The clock control circuit of the SPI can adjust its polarity and protocol so as to communicate with most of synchronized serial peripherals. When the SPI is set as a master, it can generate 256 various serial clocks in software.

The SPI can transmit and receive data at the same time. Sampling and shifting of two serial data lines are synchronized by serial clock line. Slave select line(nSS) can choose which SPI device to use. Unselected SPI devices don't affect SPI bus. The nSS line can be used to notify conflict among multiple masters in master SPI mode.

Error detection circuit is used to connect processes. When shifter register is written during transmission operation, it is a conflict. Multiple master mode failure detector disables output driver when more than one CPUs try to become bus master.

20.3.1 SPI Pins

SPI has four bi-directional pins: MISO, MOSI, SCK, and nSS. WOMP bit of SPI control register decides the output operation mode of each pins. Possible output operation modes are open drain and CMOS.

MSTR bit of SPI control register decides whether the SPI will operat as a master or a slave, and pins also follow the decision.

Table 20-1 SPI Pin Functions

Pin Name	*Mode*	*Function*
Master in, slave out(MISO)	Master	Provides serial data input to the SPI
	Slave	Provides serial data output from the SPI
Master out, slave in (MOSI)	Master	Provides serial output from the SPI
	Slave	Provides serial input to the SPI
serial clock(SCK)	Master	Provides clock output from the SPI
	Slave	Provides clock input to the SPI
Slave select(nSS)	Master	Output : Selects slave devices
	Slave	Input : chip select for SPI

20.3.2 SPI Operating Modes

SPI can become either master or slave. When its CPU controls data transmission, its mode is master. On the other hand, when a external device controls the data transmission, its mode is slave. MSTR bit of control register decides the mode.

Master Mode

If the MSTR bit of SPICTRL is set, SPI operates as master mode. Master can initialize serial transmission, and doesn't respond to initialization from external side.

In master mode, MISO pin is used for serial data input, and MOSI pin is used for serial data output. Depending on application area, one or two of these can be used.

Following procedure is required to use SPI in master mode.

1. Set BAUD, CPHA, CPOL, SIZE, MSBF, and WOMP of SPICTRL register.
2. MSTR bit should be set for master mode.
3. Set SPIEN bit to enable SPI.
4. Enable slave device.
5. Write proper data on SPIDATA register to begin transmission.
6. When the transmission finishs, SPIF flag of SPISTAT register is set by hardware, and it raises interrupt request. SPIF flag will be cleared automatically after reading SPISTAT and read or write SPIDATA register.

Data transmission is synchronized with internal serial clock(SCK). CPHA and CPOL bits of SPICTRL register controls phase and polarity of the clock. The clock is used for both transmiting data into MOSI pin and latching data from MISO pin.

Slave Mode

If MSTR bit of SPICTRL register is set to "0", the SPI becomes slave mode. In slave, SPI cannot initialize serial transmission. Transmissions are only initialized by external bus master. The slave mode is used when there are multiple masters on SPI bus because only one device can become the bus master at a time.

In slave mode, MISO pin is used for serial data output, and MOSI pin is used for data input. Depending on its application area, one or both of these can be used. SCK is input serial clock, and nSS signal is required to become active.

Data register should be written for data transmission. In slave mode, SCK, MOSI, and nSS pin are input, and MISO pin is output. CPHA, CPOL, SIZE, MSBF, and WOMP should be written. MSTR bit should be cleared for slave mode. SPIEN should be set to enable SPI. In slave mode, BAUD value doesn't affect SPI's operation.

When SPIEN is set and MSTR is cleared, "LOW" status of nSS pin initialize the operation of slave mode. nSS pin is only input.

After transmitting a byte or a word, SPI sets SPIF flag. If SPIF is set when SPIE is "1", a interrupt request raises.

Transmission is synchronized with external SCK. CPHA and CPOL are used to latch data from MOSI pin or to decide clock edge of outgoing data through MISO pin.

20.3.3 Data Transfer Timing

Following Figure 20-2 shows data transmission timing diagram when CPHA is '0' and MSB is comes first. It shows two form of SCK. One is when CPOL is '0', and the other is when CPOL is '1'. It can be a diagram of both master and slave because they share SCK, MISO, and MOSI lines. MISO signal is a output of slave, and MOSI signal is output of master. nSS signal is chip select.

If master write data on SPDR, transmission is initialized. Slave is initialized when nSS sees a falling edge. SCK signal remains inactive until the half period of SCK cycle.SPIF bit which represent the end of a transmission is set at the eighth SCK cycle. When CPHA is '0', nSS toggles from low to high after transmiting a byte. If a slave write on data register when nSS is low, write collision error raises.

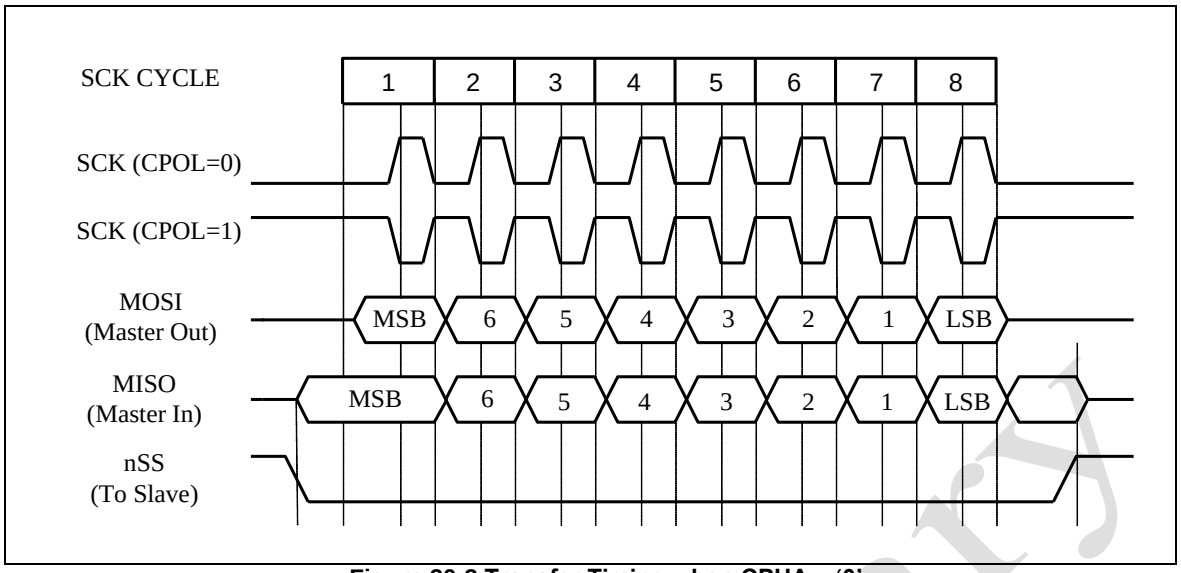


Figure 20-2 Transfer Timing when CPHA = '0'

The next Figure 20-3 is for CPHA='1'. SCK become inactive at the half period of the eighth cycle. SPIF bit is set at the end of the eighth SCK cycle. Because the last edge is generated at the middle of the eighth SCK cycle, slave finishes receving after samping the last data. nSS keeps "low" state during enough time after transmitting 1 byte.Thus, if CPU continuously sends data, nSS keeps low state.

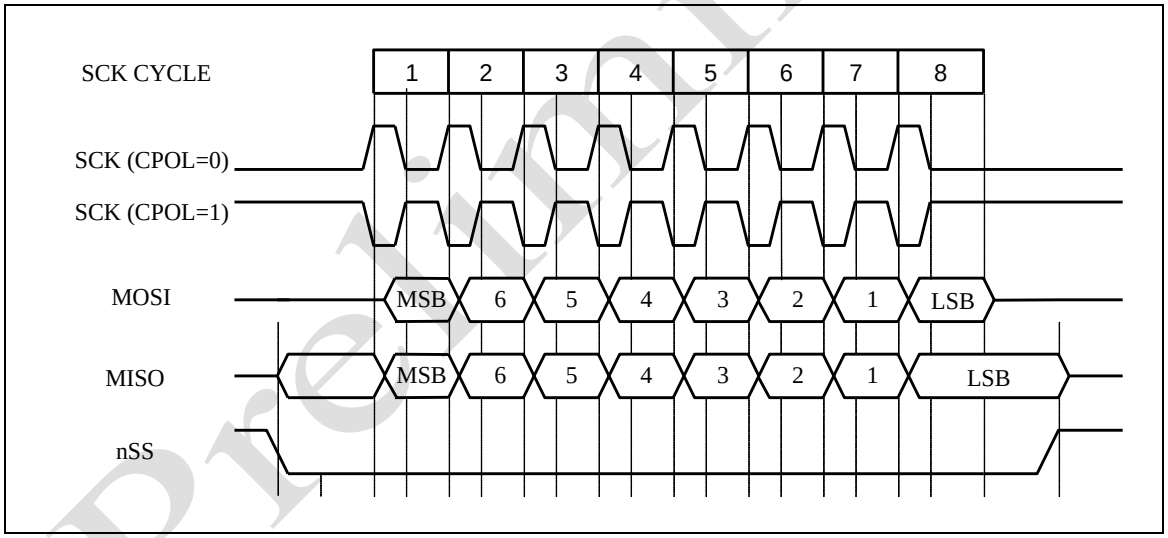


Figure 20-3 Transfer Timing when CPHA = '1'

20.3.4 SCK Phase and Polarity Control

Two bits of control register decide the phase and polarity of SCK. CPOL bit decides the polarity of the clock(high or low). CPHA bit decide the phase of transmission which affects the timing of transmission. The polarity and phase of master and slave should be same. However, in some cases, Master can communicate with slave with different polarity and phase by changing them during a transmission. This flexibility of SPI allows it direct connection with most of synchrnoized serial peripherals.

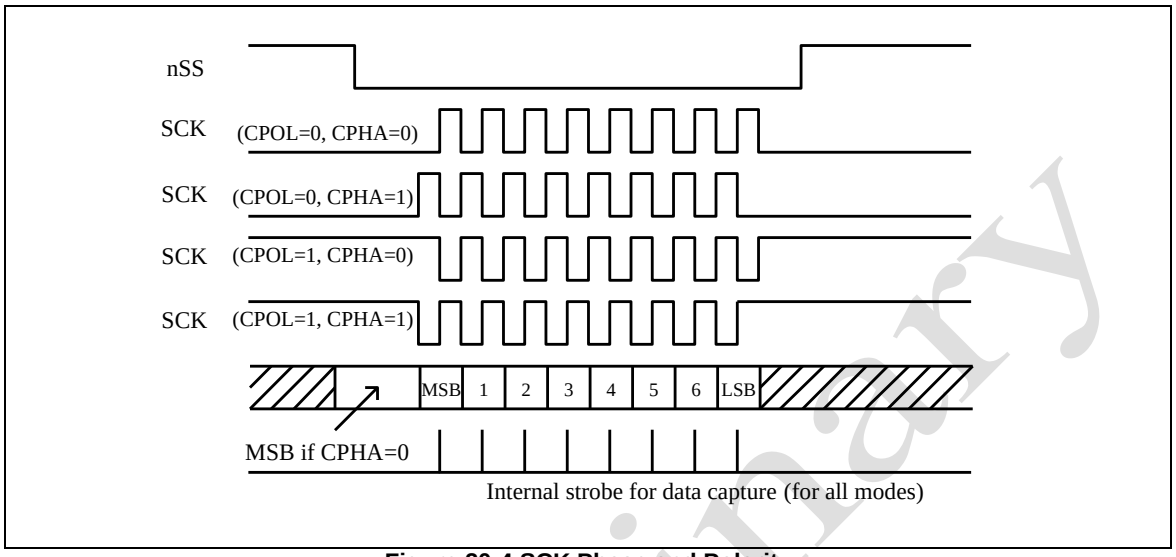


Figure 20-4 SCK Phase and Polarity

20.3.5 SPI Serial Clock Baud Rate

SPI Baud rate can be set between 1 to 255 by writing SPBR register. In slave mode, SCK is given by external SPI master; therefore, So SPIBRR register value is ignored. However, its maximum speed is limited by system clock.

$$SCK\ Baud\ Rate = \frac{f_{PCLK}}{2 \times (SPIBR + 1)}$$

or

$$SPIBR = \frac{f_{PCLK}}{2 \times SCK\ Baud\ Rate} - 1$$

20.3.6 Open-Drain Output for Wired-OR

Unless there are multiple SPI masters, SPI bus output doesn't need to support open-drain. When open-drain output is necessary, WOMP bit of SPICTRL register should be set. Pull-up register is necessary for each open-drain output line

20.3.7 Transfer Size and Direction

SPISIZE bit of SPICTRL register decide the transfer size of SPI: 8, 16, or 32bit. MSBF bit of SPICTRL reigster decides which bit to transfer first (MSB or LSB).

20.3.8 Write Collision

Write collision raises if one try to write SPIDATA register during a transmission.

20.3.9 MODE Fault

If mode fault error happens when SPI is set to master mode and nSS signal input line is asserted, MODF bit of SPISTAT is set. MODF can be set only under master mode, and it happens when other SPI device tries to become a master.

20.3.10 Interrupt

SPIF Interrupt

It is raised when both FIFO and TX shift register become empty, and this means SPI transmission is complete.

MODF Interrupt

It is raised when mode fault happens. Mode fault happens when more than one master try to transmit data.

nSS Interrupt

It is raised when nSS port signal changes.

TX_FIFO_FULL, TX_FIFO_EMPTY, RX_FIFO_FULL, RX_FIFO_EMPTY

- TX_FIFO_FULL: Means the internal 8 byte FIFO became full. If more data are added to FIFO when it's full, data transmission will be corrupted.
- TX_FIFO_EMPTY: Means every data in the FIFO are transmitted. However, because TX shift register can be not empty yet, so this interrupt doesn't mean SPI transmission is completed.
- RX_FIFO_FULL: means RX_FIFO is full.
- RX_FIFO_EMPTY: means RX_FIFO is empty.

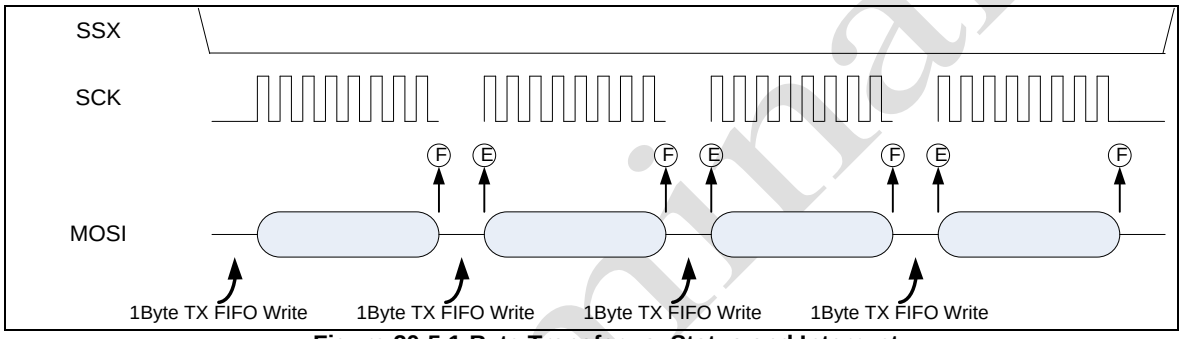


Figure 20-5 1-Byte Transfer vs. Status and Interrupt

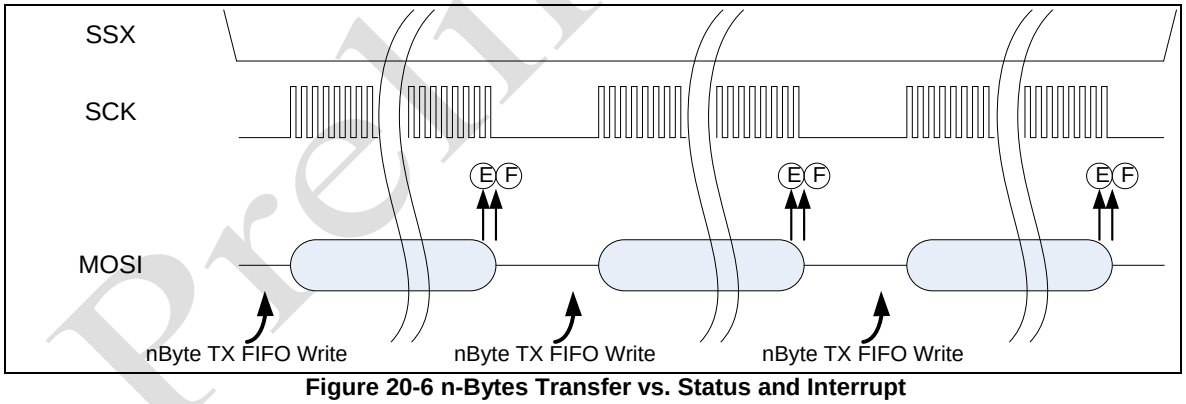


Figure 20-6 n-Bytes Transfer vs. Status and Interrupt

20.4 Register Description

20.4.1 SPI Control Register (SPICTRL)

Address : 0xA002_1000

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	R/W	SPIEN : SPI Enable 0 : SPI is disabled. 1 : SPI is enabled	0
6	R/W	WOMP : Wired-OR Mode for SPI Pins 0 : Outputs have normal CMOS drivers. 1 : Open-drain drivers	0
5	R/W	MSTR : Master/Slave Mode Select 0 : Slave operation 1 : Master operation	0
4	R/W	CPOL : Clock Polarity 0 : The inactive state value of SCK is logic level zero 1 : The inactive state value of SCK is logic level one.	0
3	R/W	CPHA : Clock Phase 0 : Data captured on the leading edge of SCK and changed on the trailing edge of SCK. 1 : Data is changed on the leading edge of SCK and captured on the trailing edge of SCK.	0
2	R/W	MSBF : Most Significant Bit First 0 : Serial data transfer starts with LSB. 1 : Serial data transfer starts with MSB.	0
1 : 0	R/W	SPISIZE : Transfer Data Size 00 : 8-bit data transfer. 01 : 16-bit data transfer. 10 : 32-bit data transfer.	0

20.4.2 SPI Baud Rate Register (SPIBR)

Address : 0xA002_1004

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7 : 0	R/W	Serial Clock Baud Rate $SCK = \frac{f_{PCLK}}{2 \times (SPIBR + 1)}$ Master Mode SCK ≤ APB Clock / 2 Slave Mode SCK ≤ APB Clock / 4	0xFF

20.4.3 SPI Status Register (SPISTAT)

Address : 0xA002_1008

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	R	SPIF : SPI Finished Flag 0 : SPI is not finished. 1 : SPI is finished.	0
6	R	WCOL : Write Collision 0 : No attempt to write to the SPDR happened during the serial transfer. 1 : Write collision occurred.	0
5	R	MODF : Mode Fault Flag 0 : Normal operation 1 : Another SPI node requested to become the network SPI master while the SPI was enabled in master mode	0
4	R	nSS : Slave Select Flag 0 : Current Value of nSS port is low 1 : Current Value of nSS port is high	0
3	R	STXF : TX FIFO Full Status bit 0 : FIFO_TX is not full 1 : FIFO_TX is full	0
2	R	STXE : TX FIFO Empty Status bit 0 : FIFO_TX is not empty 1 : FIFO_TX is empty	0
1	R	SRXF : RX FIFO Full Status bit 0 : FIFO_RX is not full 1 : FIFO_RX is full	0
0	R	SRXE : RX FIFO Empty Status bit 0 : FIFO_RX is not empty 1 : FIFO_RX is empty	0

20.4.4 SPI Data Register (SPIDATA)

Address : 0xA002_100C

Bit	R/W	Description	Default Value
31 : 0	R/W	SPI Data At 32-bit transfer mode - MSB of Data is SPDR[31] At 16-bit transfer mode - MSB of Data is SPDR[15] At 8-bit transfer mode - MSB of Data is SPDR[7] LSB of Data (received or transmit) is SPDR[0] in any transfer mode	0x0000_0000

20.4.5 SPI nSS Control Register (nSSCTRL)

Address : 0xA002_1010

Bit	R/W	Description	Default Value
31 : 1	R	Reserved	-
0	RW	nSSCON : nSS Output Level	1

20.4.6 SPI Interrupt Mask Register (SPIINT)

Address : 0xA002_1014

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	RW	SPIFE : SPIF Interrupt en/disable SPIF Interrupt occurs when transfer has completed. 0 : SPIF interrupt is disabled 1 : SPIF is enabled	0
6	RW	MODFE : MODFI Interrupt en/disable MODFI Interrupt occurs when two more master use data line. 0 : MODFI interrupt is disabled 1 : MODFI is enabled	0
5	R	Reserved	0
4	RW	nSSEN : nSS Interrupt en/disable nSS Interrupt occurs when nSS signal has changed. 0 : nSS Interrupt is disabled 1 : nSS Interrupt is enabled	0
3	RW	STXFE : FIFO_TX_FULL Interrupt en/disable FIFO_TX_FULL Interrupt occurs when FIFO_TX is full 0 : FIFO_TX_FULL Interrupt is disabled 1 : FIFO_TX_FULL Interrupt is enabled	0
2	RW	STXEE : FIFO_TX_EMPTY Interrupt en/disable FIFO_TX_EMPTY Interrupt occurs when FIFO_TX is empty 0 : FIFO_TX_EMPTY Interrupt is disabled 1 : FIFO_TX_EMPTY Interrupt is enabled	0
1	RW	SRXFE : FIFO_RX_FULL Interrupt en/disable FIFO_RX_FULL Interrupt occurs when FIFO_RX is full 0 : FIFO_RX_FULL Interrupt is disabled 1 : FIFO_RX_FULL Interrupt is enabled	0
0	RW	SRXEE : FIFO_RX_EMPTY Interrupt en/disable FIFO_RX_EMPTY Interrupt occurs when FIFO_RX is empty 0 : FIFO_RX_EMPTY Interrupt is disabled 1 : FIFO_RX_EMPTY Interrupt is enabled	0

21 TWI (TWO WIRED INTERFACE)

adStar-L has a TWI controller to interface with general TWI bus. TWI has two signals: SCL and SDA.

21.1 Features

- Master transmitter mode
- Master receive mode
- Slave transmitter mode
- Slave receive mode
- Software programmable clock frequency
- Software programmable acknowledge bit
- Interrupt driven data-transfers
- Start/Stop/Repeated Start/Acknowledge generation
- Multi master operation

21.2 Block Diagram

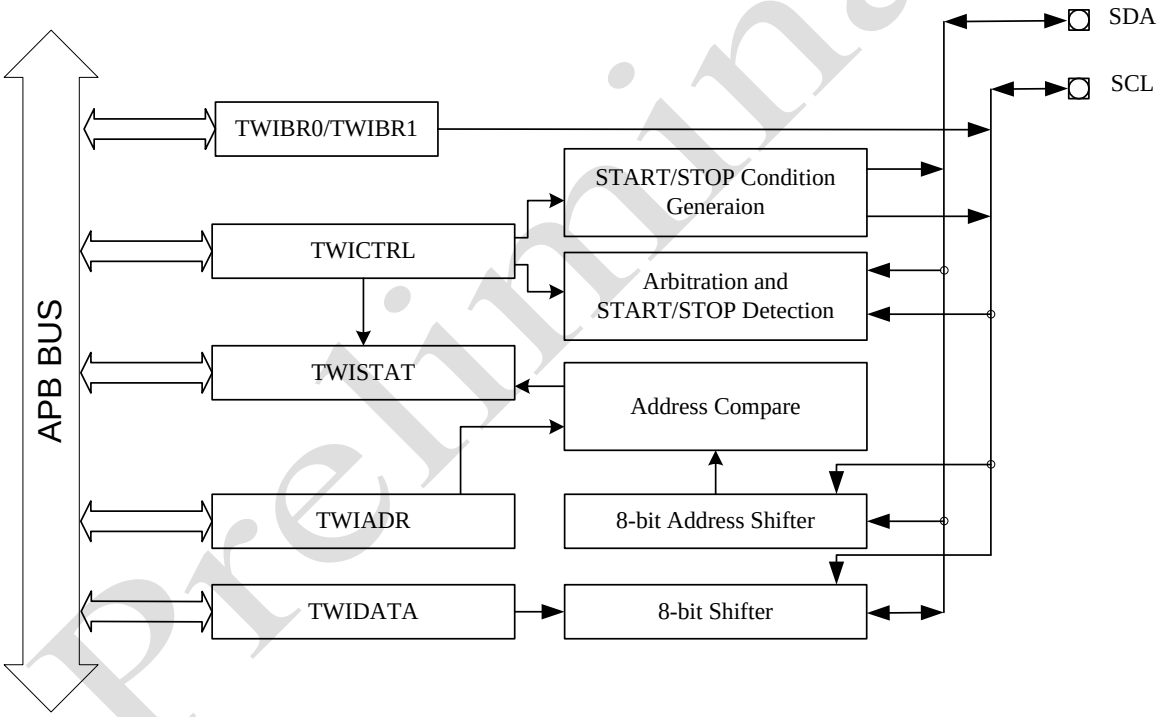


Figure 21-1 TWI Block Diagram

21.3 Functional Description

21.3.1 DATA TRANSFER FORMAT

Every data on SDA line has 8bit width. The number of byte for a transfer is not limited. The first byte after start condition is address field. When TWI bus is in master mode, the master sends the address field. Every bytes are followed by ACK bit. And always MSB bits are tranfered first.

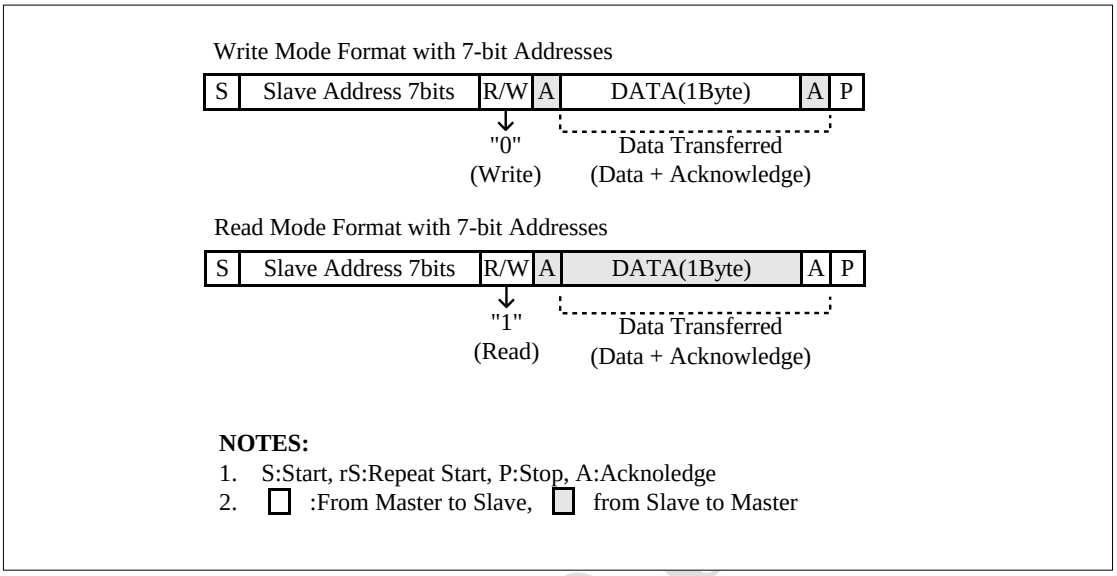


Figure 21-2 TWI-Bus Interface Data Format

21.3.2 START AND STOP CONDITION

Start condition initalizes a transfer, and stop condition finishes it. Start condition is the transition of SDA line from high-to-low during SCL line is high. Stop condition is the transition of SDA line from low-to-high when SCL is high. If a start condition happens, TWI bus become busy. After a stop condition, TWI bus become free.

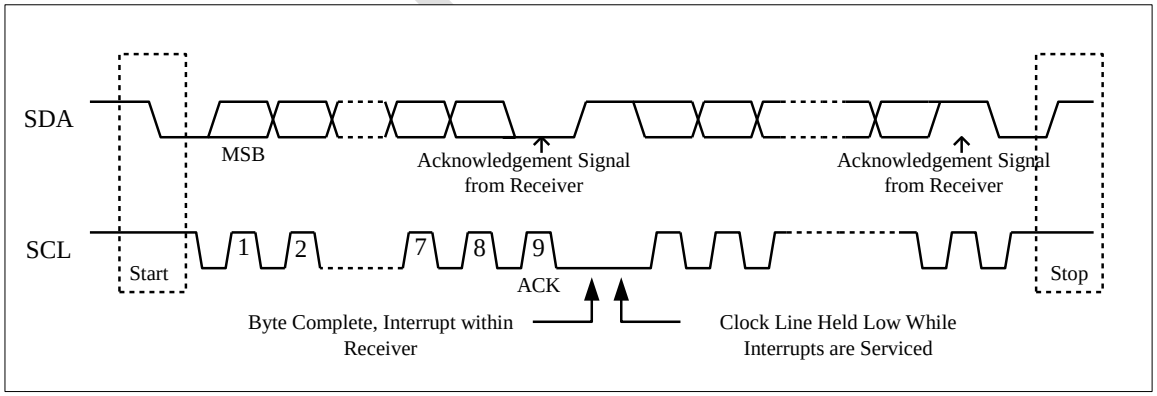


Figure 21-3 Data Transfer on the TWI-Bus

21.3.3 ACK SIGNAL TRANSMISSION

To finish a byte transfer, receiver should send a ACK bit to its sender. ACK pulse should happen at the ninth clock of SCL line. So we need 9 clocks to transfer a byte. Master should generate clock pulses fot ACK bit reception.

Sender should release SDA line to receive a ACK clock pulse. Receiver should should lower SDA line at ninth SCL period to change SDA line into “low”.

Software can set ACK bit can be ACK or NACK by setting TXACK bit of control register.

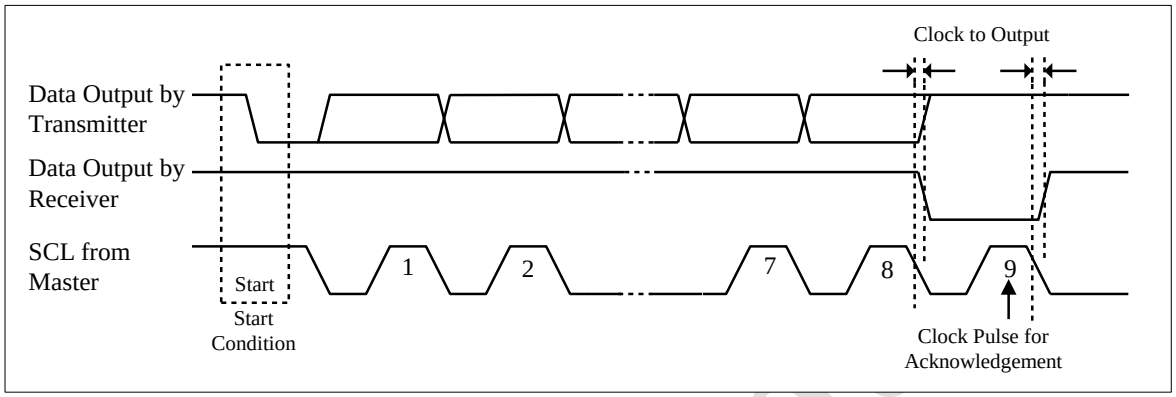


Figure 21-4 Acknowledgement of TWI

21.3.4 READ-WRITE OPERATION

In sending operation mode, TWI bus interface should wait until data shifter register become ready after transfering data. Until data writing completes, SCL line will be kept low. SCL is released after new data is written in shifter register.

When interruption is enabled, TWI raises interrupt after transfering current data.CPU writes new data into buffer after handling the interrupt request.

In receiving mode, TWI bus waits until TWI bus reads data after receiving data . During the reading, SCL is kept “low”. SCL is released after new data is read.

When interruption is enabled, TWI raises interrupt when data is received. The interrupted CPU reads the data.

21.3.5 BUS ARBITRATION PROCEDURES

Prevents multiple masters from controlling bus at the same time. If a master which sent high signal on SDA line senses other master's low level SDA signal, the first master recognize that multiple masters are on bus, and stops its transfer.

When two devices become master mode at the same time, to say master 1 and master 2, the SCL line is synchronized as following clock wave form.

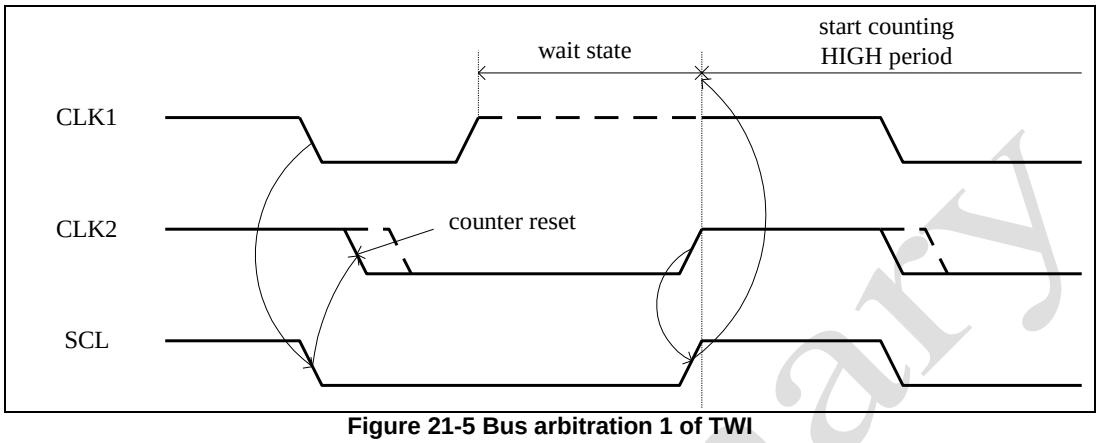


Figure 21-5 Bus arbitration 1 of TWI

In the above situation, either device 1 or device 2 will have priority depending on SDA line value as shown in the next diagram

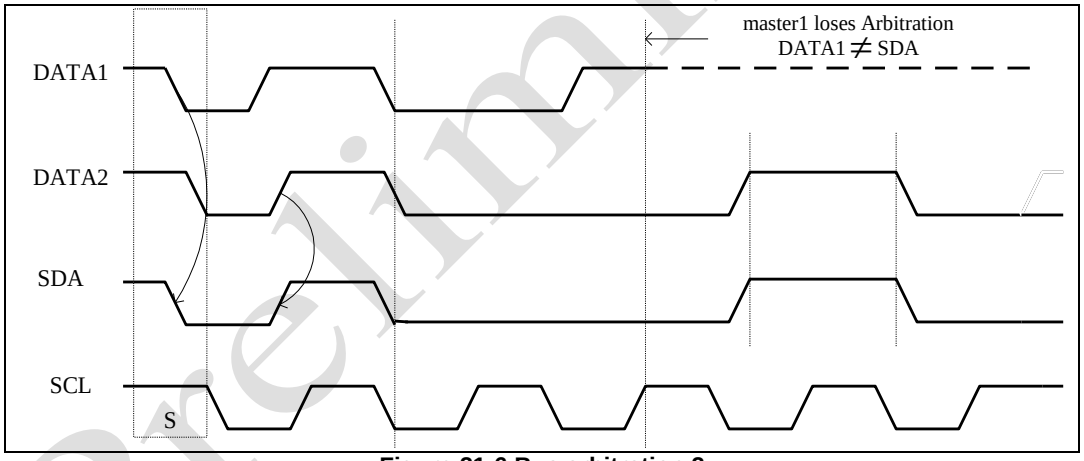


Figure 21-6 Bus arbitration 2

21.3.6 ABORT CONDITIONS

If arbitration is not occured

1. If MSTR bit of TWICTRL register is cleared, stop condition is generated.
2. No Ack generates stop condition. That is to say,SDA signal is not “low” under ACK period.

If arbitration is occured

Arbitration takes away control and clears MSTR bit, however, stop condition isn’t generated. SCL clock lasts until a byte transfer finishes, and SDA become “high”.

21.3.7 Operational Flow Diagrams

TWI initialization

First, TWI should be initialized.

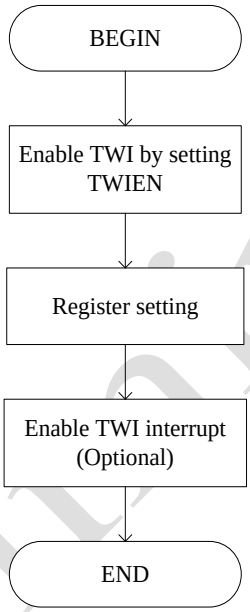


Figure 21-7 TWI Initialization Flow Char

Master Transmit / Receive

Below is the flow chart of TWI transmission and reception. For reception, additional steps are required. First, ACK bit should be set NO ACK upon the last data. This is to notify slave that master has sent its last data. Inaddition, dummy reading of TWIDATA register is required to generate SCL clock.

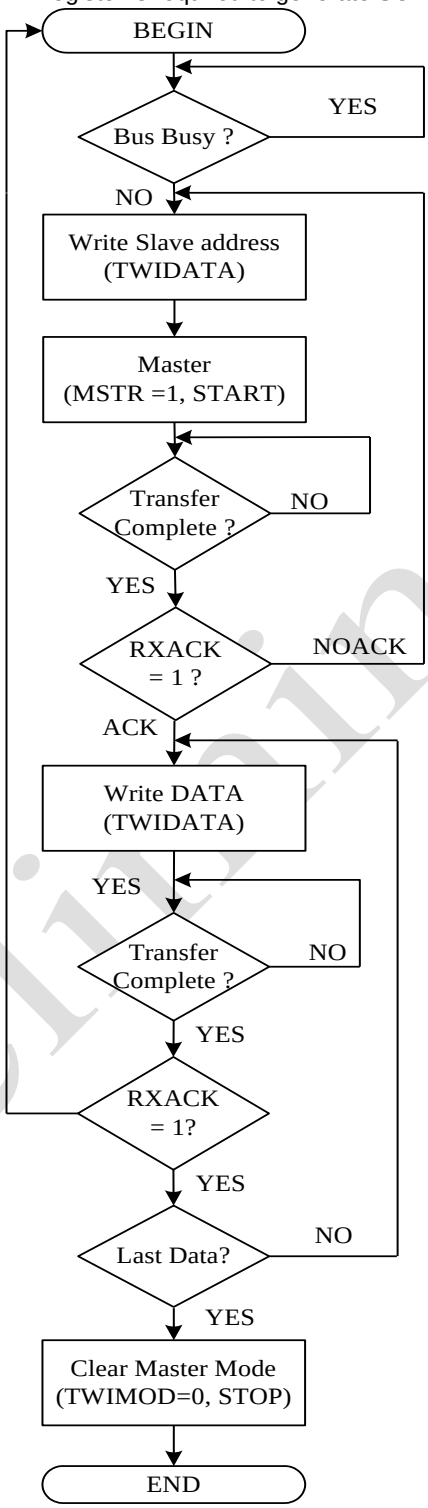


Figure 21-8 Master Transmit Flow Char

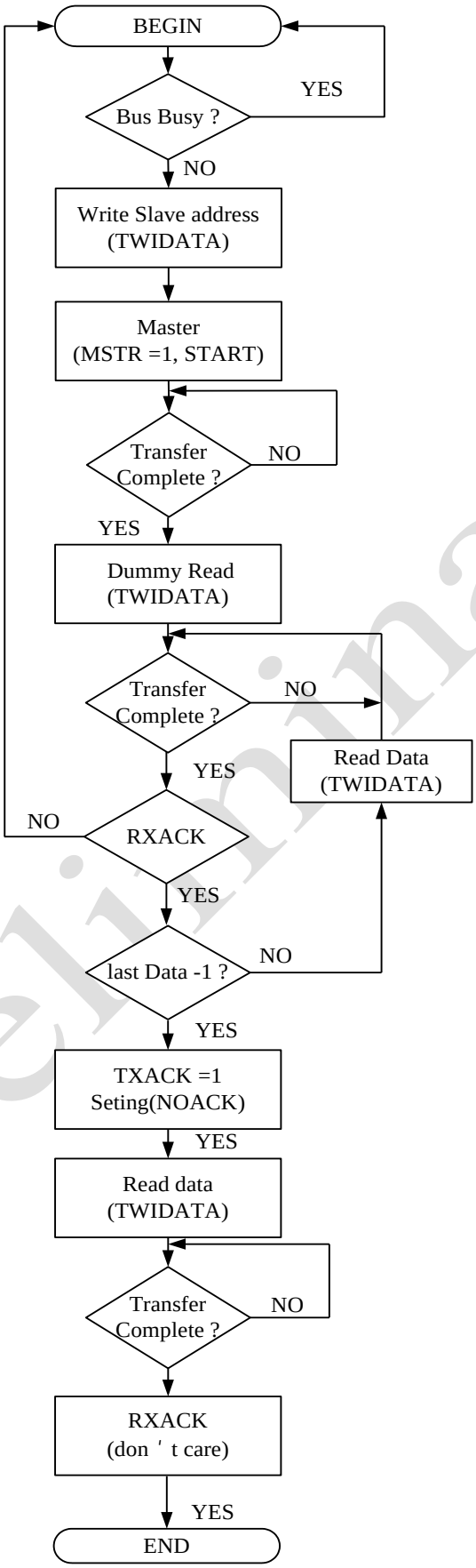


Figure 21-9 Master Receive Flow Char

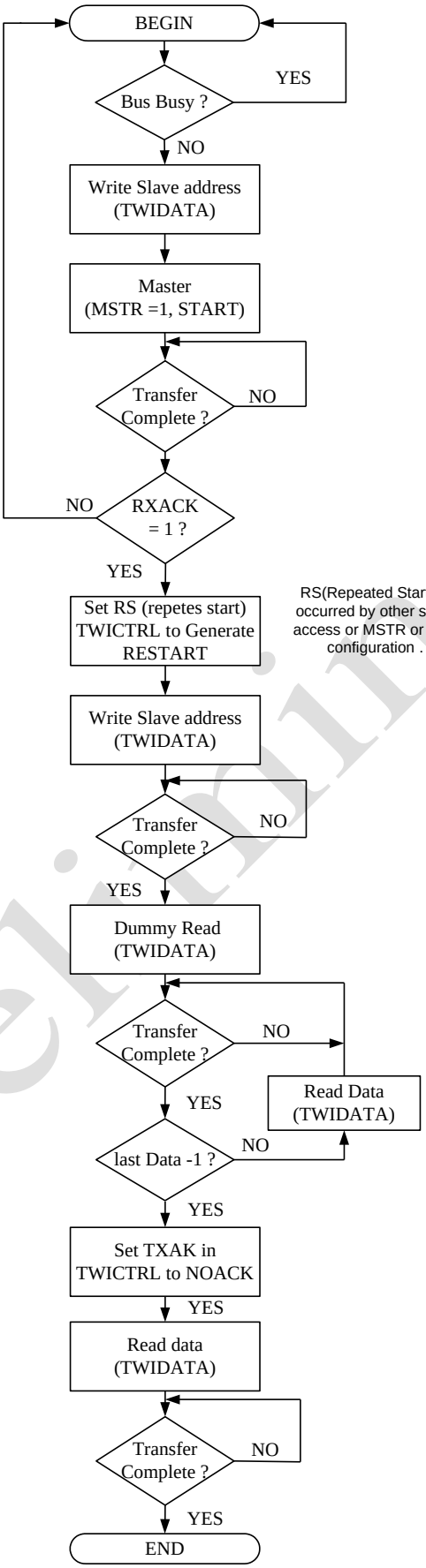


Figure 21-10 Master combined format Flow Char

Slave Mode (Polling mode)

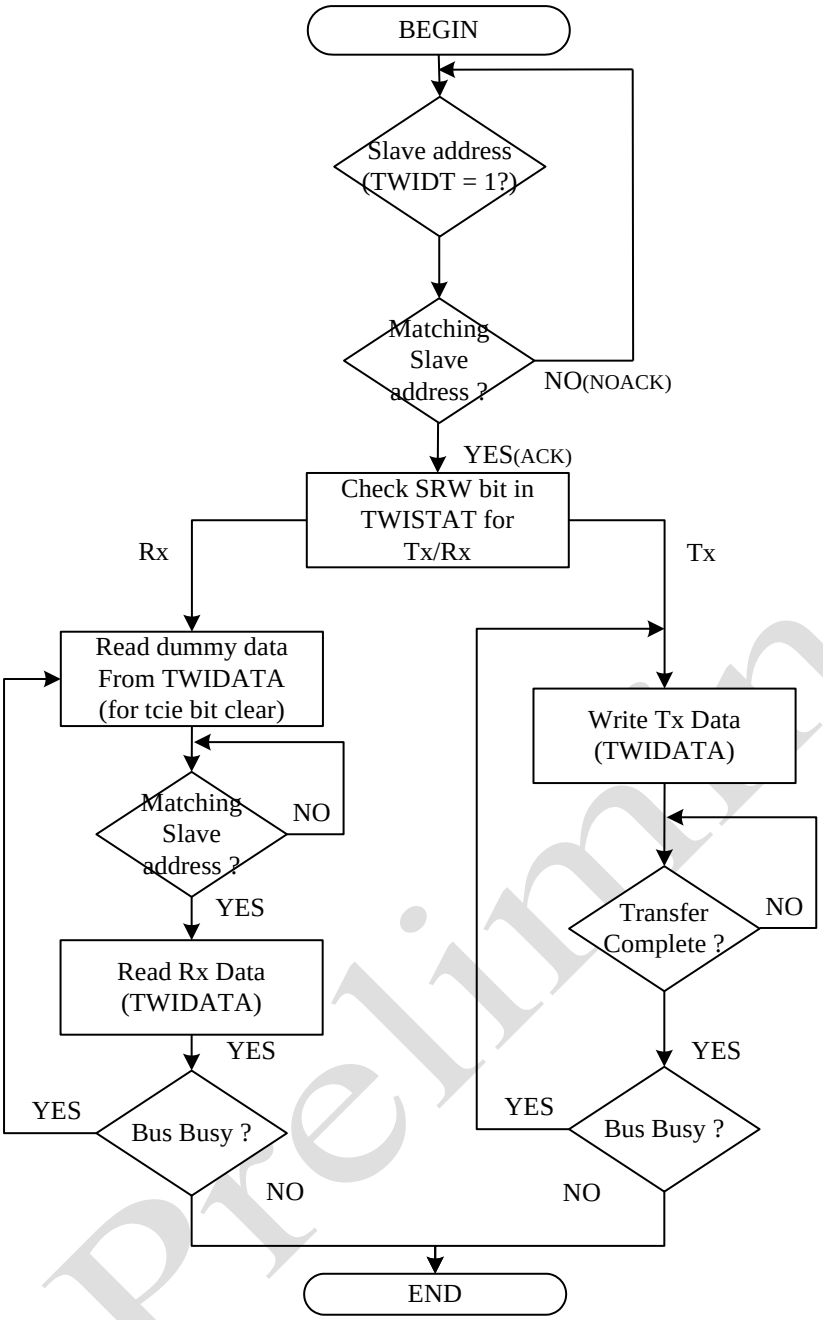


Figure 21-11 Slave Mode Flow Chart (Polling)

Slave Mode (Interrupt mode)

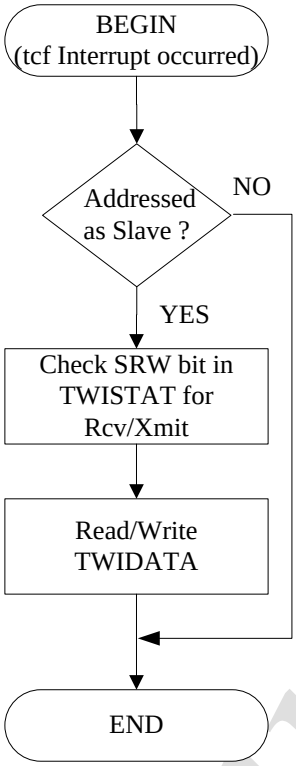


Figure 21-12 Slave Mode Flow Chart (Interrupt)

21.4 Register Description

21.4.1 TWI Control Register (TWICTRL)

Address : 0x8002_1800

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7	RW	TWIEN : TWI Controller Enable. For TWI transmission and reception, this bit should be set first. 0: Disable 1: Enable	0
6	R	Reserved.	-
5	RW	TWIMOD : Master/Slave Mode Select. When it toggles from 0 to 1, TWI enters into master mode, and START condition is generated. When it is cleared (1 to 0), STOP condition is generated, and TWI enters into slave mode. Though cleared, if TWI lost control right, STOP condition is not generated. 0: generates STOP condition 1: generates START condition	0
4	RW	TWITR : Transmit/Receive Mode Select. Decide operation in Master Mode 0: TWI Master receives 1: TWI Master transmits	0
3	RW	TWIAK : Transmit Acknowledge Enable. Decide SDA line value during ACK period. If it is in master receive mode and transmitting its last byte, NO ACK means that it is the last data transmission. After the last transmission, NO ACK generates STOP condition. 0: ACK bit = “0” – ACK (acknowledge) 1: ACK bit = “1” – NO ACK (no acknowledge)	0
2	RW	REPST : Repeated Start. If this be is set (=1) and TWI controller is in master mode, repeated START condition is generated. It is cleared after the repeated START condition is generated, 0: N/A 1: generates repeated START condition	0
1	R/W	TCIE : Transfer complete Interrupt enable bit Decide signaling interrupt or not when byte-unit transmission completes 0: Disable 1: Enable	0
0	R/W	LSTIE : Lost arbitration Interrupt enable bit Decide signaling interrupt or not when TWI lost its transmission write in master mode. 0: Disable 1: Enable	0

21.4.2 TWI Status Register (TWISTAT)

Address : 0x8002_1804

Bit	R/W	Description	Default Value
31 : 10	R	Reserved.	-
9	RW	TXEMPTY : TX Buffer Empty. Represent the status of transmitting buffer. This bit can be written when it is 0. 0: TX buffer has data to transmit 1: TX buffer is empty	1
8	RW	RXFULL : RX Buffer Full. Represent the status of receiving buffer. This bit can be written when it is 1. 0: RX buffer is empty 1: RX buffer has data to be read	0
7	R	TWIDT : Data Transferring Bit. Set whenever a byte is transmitted, and cleared when TWIDATA register is read or written. Also, writing “1” clears this bit. 0: byte is being transmitted 1:byte transmission completed	0
6	R	TWIAS : Addressed as Slave Bit. When its address and received address coincide, TWI controller become slave. This bit is cleared when TWICON register is written or when STOP condition happens. 0: Address doesn’t coincides 1: Addresses coincides	0
5	R	TWIBUSY : Bus Busy Bit. Represent the status of TWI bus. Set by START condition and cleared by STOP condition. Also, writing “0” clears this bit. 0: Bus is in idle status 1: Bus is in busy status	0
4	RW	TWILOST : Lost Arbitration Bit. This bit is set when bus loses its control in master mode. Software can clear this bit by writing “1” to this bit. 0: Lost arbitration doesn’t happen 1: Lost arbitration happen	0
3	R	TWISRW : Slave Read/Write Bit. Represent transmit or receive mode in slave mode. 0: Slave receive mode 1: Slave transmit mode	0
2	R	Reserved.	-
1	RW	RSF : Repeated start flag Represent whether repeated START condition has happened or not. Set when repeated START condition happens, and cleared when STOP condition happens. Also, writing “1” when this bit is set will clear this bit. 0: Repeated START condition didn’t happen, or STOP condition happened. 1: Repeated START condition has happened.	0
0	R	TWIRXAK : Received Acknowledge Bit. Represent SDA line value during ACK period. 0: Acknowledge received 1: No Acknowledge received	1

21.4.3 TWI Address Register(TWIADR)

Address : 0x8002_1808

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7: 0	RW	(At only slave mode) 7-bit slave address. Represent the device address of TWI controller [7:1] = Slave Address [0] = Not mapped	0x00

21.4.4 TWI Data Register (TWIDATA)

Address : 0x8002_180C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7 : 0	RW	TWI data : Represent TWI data Write – written data or the address of accessing device Read – received data	0x00

21.4.5 TWI Baud-Rate 0 Register (TWIBR0)

Address : 0x8002_1810

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7 : 0	RW	Baud-rate 0 Value. TWIBR0 ≥ 3	0x0F

21.4.6 TWI Baud-Rate 1 Register (TWIBR1)

Address : 0x8002_1814

Bit	R/W	Description	Default Value
31 : 9	R	Reserved.	-
8 : 0	RW	Baud-rate 1 Value.. TWIBR1 ≥ 0	0xFF

$$TWIBR0 = f_{PCLK} \times 700ns + 3$$

$$SCL = \frac{f_{PCLK}}{(2TWIBR1 + TWIBR0 + 7)}$$

$$TWIBR1 = \frac{f_{PCLK}}{2SCL} - \frac{TWIBR0 + 7}{2}$$

* f_{PCLK} = AMBA APB clock frequency
*SCL = TWI transmission rate
ex) If APB clock is 50MHz and TWI transmission rate is 400Kbps, (f_{PCLK} = 50MHz, SCL = 400Kbps)

$$TWIBR0 = 50MHz \times 700ns + 3 = 50 \times 10^6 \times 700 \times 10^{-9} + 3 = 38$$

$$SCL = \frac{f_{PCLK}}{(2TWIBR1 + TWIBR0 + 7)} \Rightarrow 400Kbps = \frac{50MHz}{(2TWIBR1 + 38 + 7)} \Rightarrow 400 \times 10^3 = \frac{50 \times 10^6}{(2TWIBR1 + 45)}$$

$$\text{TWIBR1} = \frac{\frac{50\ X\ 10^3}{400kbps} - (TWIBR0 + 5)}{2}$$

- 700ns: rise time, fall (fast mode, max) for the synchronization
- 3cycle: low, high duty for the synchronization of ratio

<Baud-rate Register Setting Reference Table>

f_{PCLK}	TWIBR0	TWIBR1				
		400Kbps	300Kbps	200Kbps	100Kbps	50Kbps
60Mhz	45(0x2D)	50(0x32)	75(0x4B)	125(0x7D)	275(0x113)	-
50Mhz	38(0x26)	41(0x29)	62(0x3E)	104(0x68)	228(0xE4)	-
48Mhz	37(0x25)	39(0x27)	59(0x3B)	99(0x63)	219(0xDB)	459(0x1CB)
33Mhz	26(0x1A)	26(0x1A)	40(0x28)	67(0x43)	150(0x96)	315(0x13B)
24Mhz	20(0x14)	18(0x12)	28(0x1C)	48(0x30)	108(0x6C)	228(0xE4)
12Mhz	12(0x0C)	7(0x07)	12(0x0C)	22(0x16)	52(0x34)	112(0x70)
6Mhz	7(0x07)	2(0x02)	4(0x4)	9(0x9)	24(0x18)	54(0x36)
11.2896Mhz	11(0x0B)	6(0x06)	11(0xB)	20(0x14)	48(0x30)	105(0x69)
5.6448Mhz	7(0x07)	1(0x01)	3(0x3)	8(0x8)	22(0x16)	50(0x32)

* Above table can bear some errors.
* In TWI baud rate configuration, scl Low value is more bigger than scl HIGH value for the data setup and hold time.

* TCF interrupt.
tcf_irq is interrupt signal which occured the end of data transmission(1-byte). This signal occured after scl line's toggles nine times(TCIE(Confirm Transfer complete bit)).

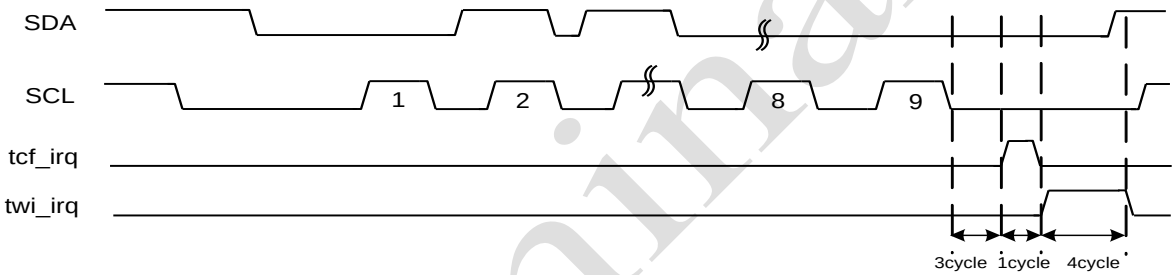


Figure 21-13 Tcf interrupt wave form

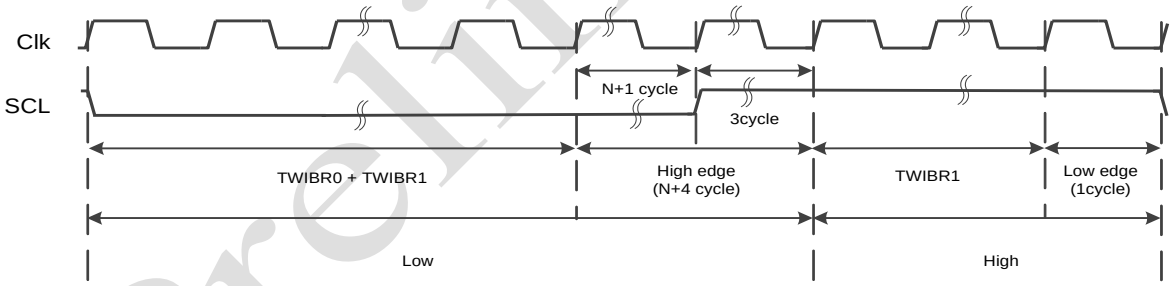


Figure 21-14 SCL Hold wave form

* Minimum high edge width is 4-cycles. Maximum high edge width is 4-cycle + α. (If TWI operate master mode and slave hold SCL low)

22 SOUND MIXER

22.1 Features

- 4-CH. Mixing
- Re-Sampler
- Gain Controller
- 32-Depth Buffer for each channel
- 1-CH PWM output for Stereo or 2-CH PWM output for mono (1-CH Digital Modulator)

22.2 Block Diagram

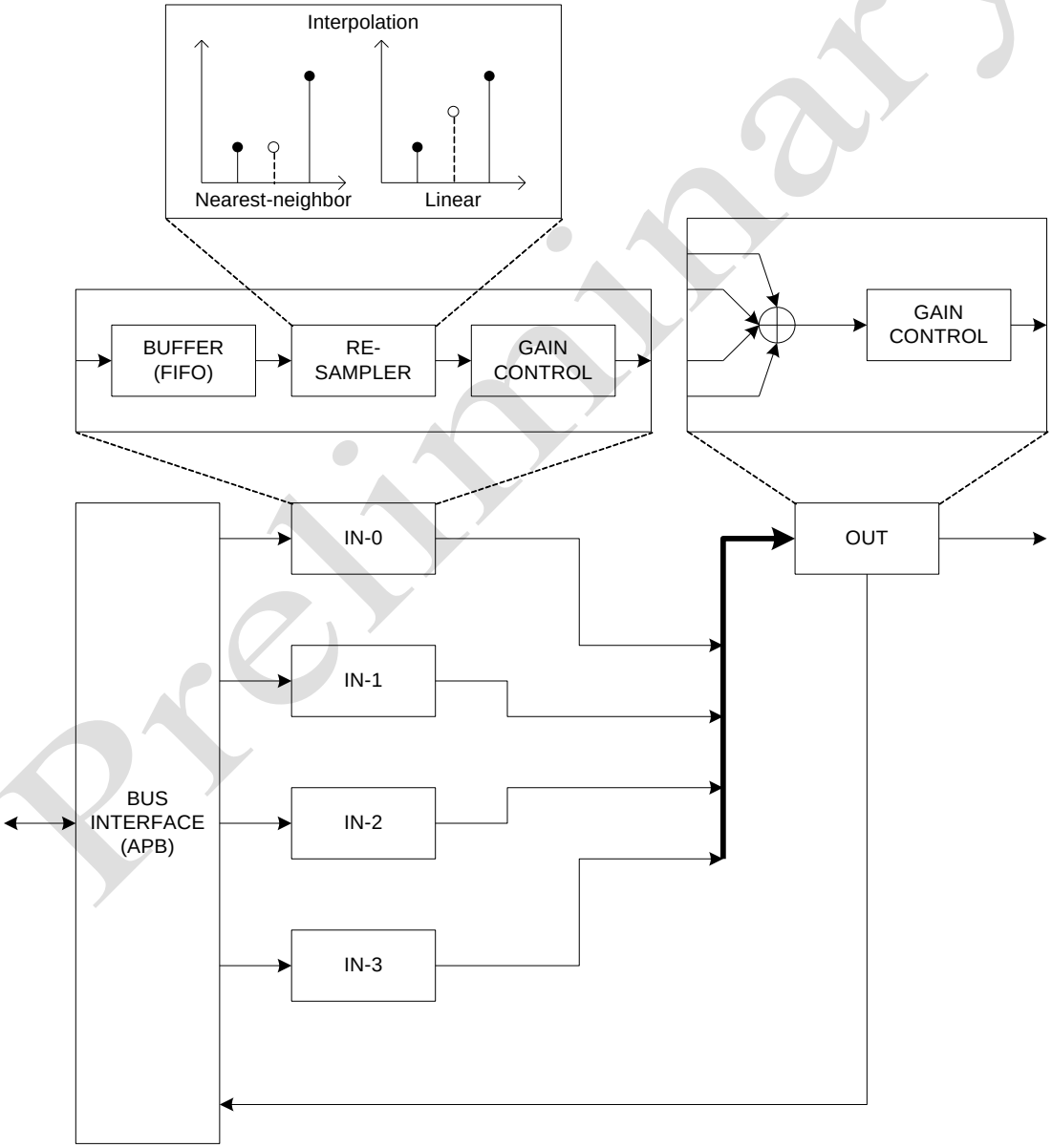


Figure 22-1 Mixer Block Diagram

22.3 Low Pass Filter for Digital Modulator

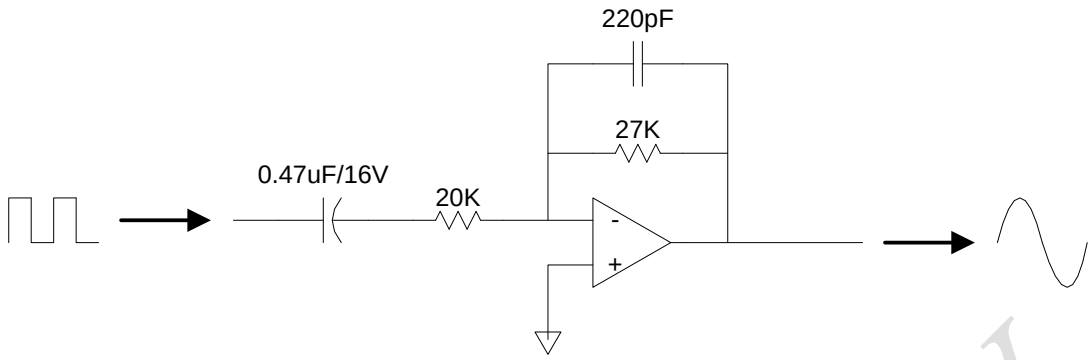


Figure 22-2 Low pass filter for digital modulator

22.4 Sound Mixer clock

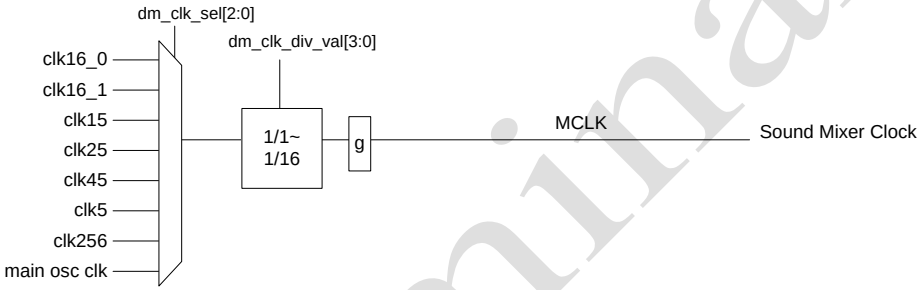


Figure 22-3 Sound Mixer Pre-Scaler

*** As shown in the Figure 22-3, there are eight possible sources for MCLK. The selected clock can be further divided by any ratio from 1 to 1/16 before going to the Sound Mixer module. (Refer to 4.2 Clock control)

22.5 Mixer Block Diagram

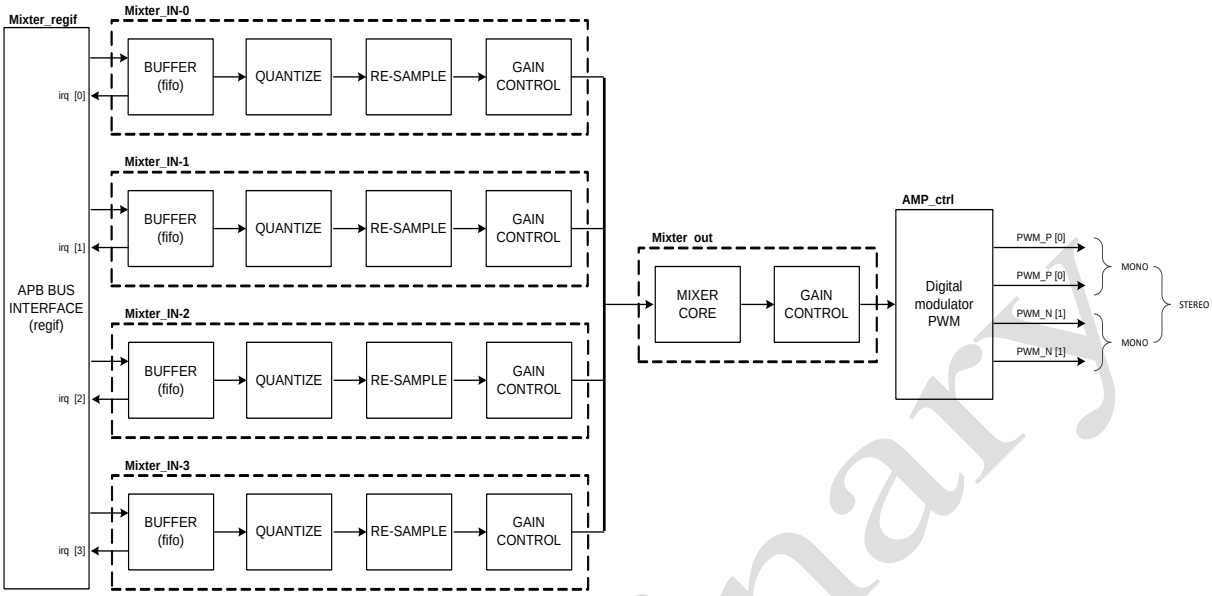


Figure 22-4 Sound Mixer output diagram

*** Sound mixer consist of 4ch input(IN0~3) and 1ch output(out_2). The value which configured by register entry to mixer IN 0~3 and output to mixer OUT like Figure 22-4. At this moment, Each IN0~3 interrupt signals make from or circuit inside the mixer_regif block.

22.6 Register Description

22.6.1 Mixer Control Register (MIXER_ CON)

Address: 0xA002_1C00, 0xA002_1C10, 0xA002_1C20, 0xA002_1C30 (IN-0 ~ IN-3)

Bit	*R/W*	*Description*	*Default Value*
31 : 29	R	Reserved	-
28	R/W	Method of interpolation 0: Nearest-neighbor 1: Linear	0x0
27 : 25	R	Reserved	-
24 : 16	R/W	Step for re-sampling N = ((InFs * 256) / OutFs) – 1, (N=0~511)	0x0FF
15 : 10	R	Reserved	-
9 : 8	R/W	Out selection 10 : Out	0x0
7 : 4	R/W	Mode 0000: Unsigned stereo 8-bit PCM 0001: Unsigned mono 8-bit PCM 0010: Signed stereo 8-bit PCM 0011: Signed mono 8-bit PCM 0100: Unsigned stereo 16-bit PCM 0101: Unsigned mono 16-bit PCM 0110: Signed stereo 16-bit PCM 0111: Signed mono 16-bit PCM 1xxx: Reserved	0x0
3	R/W	DMA request 0: Disable 1: Enable	0x0
2	R/W	Interrupt 0: Disable 1: Enable	0x0
1	R/W	L/R swap 0: Disable 1: Enable	0x0
0	R/W	Active 0: Disable 1: Enable	0x0

Address: 0xA002_1CA0 (OUT)

Bit	R/W	Description	Default Value
31 : 1	R	Reserved	-
0	R/W	Active 0: Disable 1: Enable	0x0

22.6.2 Mixer Volume Register (MIXER_VOL)

Address: 0xA002_1C04, 0xA002_1C14, 0xA002_1C24, 0xA002_1C34, 0xA002_1CA4 (IN-0 ~ IN-3, OUT)

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 8	R/W	Right gain (±0.5dB) 0xFF(0dB) ~ 0x80(-63.5dB), 0x7F~0x0(-∞dB)	0xFF
7 : 0	R/W	Left gain (±0.5dB) 0xFF(0dB) ~ 0x80(-63.5dB), 0x7F~0x0(-∞dB)	0xFF

22.6.3 Mixer Buffer Status Register (MIXER_BST)

Address: 0xA002_1C08, 0xA002_1C18, 0xA002_1C28, 0xA002_1C38 (IN-0 ~ IN-3)

Bit	R/W	Description	Default Value
31 : 6	R	Reserved	-
5 : 0	R	Buffer count value 0(Empty) ~ 32(Full)	0x0

22.6.4 Mixer Data Register (MIXER_DAT)

Address: 0xA002_1C0C, 0xA002_1C1C, 0xA002_1C2C, 0xA002_1C3C (IN-0 ~ IN-3)

Bit	R/W	Description	Default Value
31 : 0	R/W	PCM data	-

22.6.5 Mixer Out Register (MIXER_OUT)

Address: 0xA002_1CAC (OUT)

Bit	R/W	Description	Default Value
31 : 10	R/W	Reserved	-
9 : 8	R/W	Step for over-sampling 00: x1 01: x2 10: x4 11: x8	0x0
7 : 4	R/W	Sine wave generation (For test) 0000: Disable otherwise: Enable	0x0
3 : 2	R/W	PWM modulation 00: Class-AD single side modulation 01: Class-AD double side modulation 10: Class-BD single side modulation 11: Class-BD double side modulation	0x0
1 : 0	R/W	Noise transfer function 00: Disable 01: 4th-order FIR filter 10: 5th-order FIR filter 11: 5th-order optimal FIR filter	0x0

22.6.6 Mixer Interrupt Status Register (MIX_IST)

Address: 0xA002_1CC0

Bit	R/W	Description	Default Value
31 : 7	R	Reserved	-
6 : 4	R	Reserved	-
3	R	IN-3 interrupt	0x0
2	R	IN-2 interrupt	0x0
1	R	IN-1 interrupt	0x0
0	R	IN-0 interrupt	0x0

23 ADC CONTROLLER

adStar-L includes 100KSPS 12-bit SAR ADC. Recommended operation frequency is 1.2MHz. Conversion cycle is 15 cycles of ADC input clock.

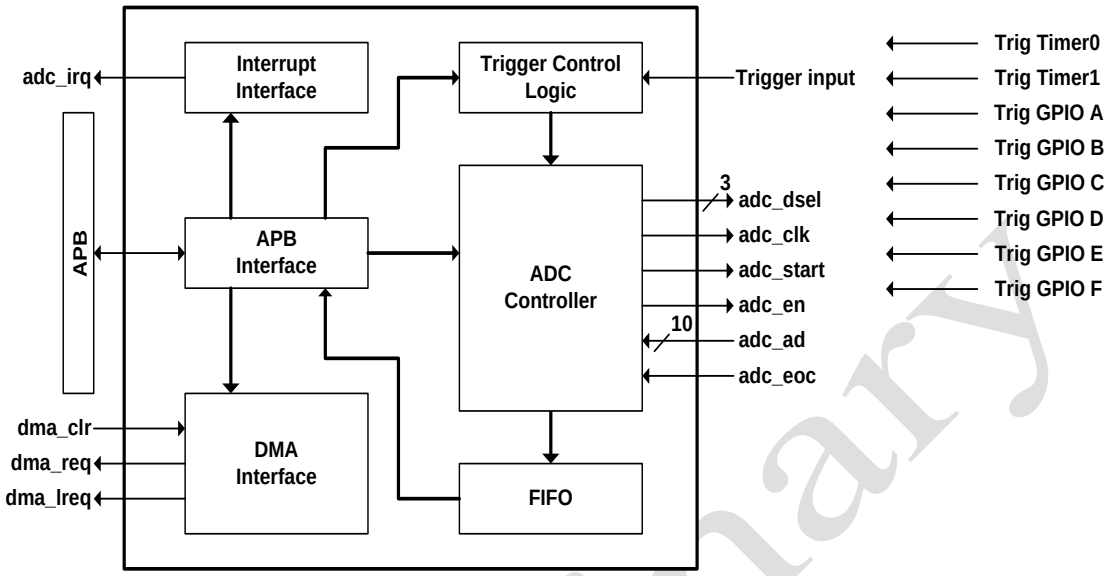


Figure 23-1 ADC Block Diagram

23.1 Features

- Various SOC source select
- Continuous Mode support
- 4-depth FIFO
- DMA Mode (in FIFO Mode)
- 4 channel input

23.2 Register Description

23.2.1 ADC Control Register (ADCCTRL)

Address : 0xA002_3800

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15	R/W	External Trigger Enable 1: External Trigger enable 0: External Trigger disable	0
14 : 12	R/W	External Trigger Source Select Choose trigger source for SOC 000: Timer 0 001: Timer 1 010: GPIOA[7] 011: GPIOB[0] 100: GPIOC[7] 101: GPIOD[7] 110: GPIOE[7] 111: GPIOF[7]	000
11	R/W	Periodic Mode Selection 0: Normal Operation Mode (1 pulse SOC Generation) 1: Periodic Mode (Continuous SOC Generation)	0
10	R/W	DMA Last Transfer If it is set in FIFO and DMA mode, it initiates DMA last request, and cleared after the initiation.	0
9	R/W	DMA Mode Enable If it is set in FIFO mode, it requests DMA transfer until FIFO is full. It is cleared when DMA last request happens.	0
8	R/W	FIFO Mode 1: Using FIFO 0: NOT using FIFO	0
7 : 5	R/W	ADC Channel Selection 000: ADCIN0 001: ADCIN1 010: ADCIN2 011: ADCIN3	00
4 : 2	R/W	ADC Source clock selection 000: APB Clock / 2 001: APB Clock / 4 010: APB Clock / 8 011: APB Clock / 16 100: APB Clock / 32 101: APB Clock / 64 110: APB Clock / 128 111: APB Clock / 256 * Sampling period is as long as twelve times the period of ADC source clock.	00
1	R/W	ADC Start Conversion(STC) SOC happens when it is set. Cleared after one period of ADC clock.	0
0	R/W	ADC Enable 0: ADC Disable 1: ADC Enable	0

23.2.2 ADC Data Register (ADCDATA)

Address: 0xA002_3804

Bit	R/W	Description	Default Value
31 : 12	R	Reserved	-
11 : 0	R	12-bit ADC data	0x000

23.2.3 ADC FIFO Register (ADCFIFO)

Address: 0xA002_3808

Bit	R/W	Description	Default Value
31 : 12	R	Reserved	-
11 : 0	R	In case of ADC FIFO Mode 12-bit ADC FIFO Data	0

23.2.4 ADC Status Register (ADCSTAT)

Address : 0xA002_380C

Bit	R/W	Description	Default Value
31 : 9	R	Reserved	-
8	R	EOC status 0: EOC have not occurred. 1: an EOC has occurred. If EOC occured this bit set 1. When you read this bit it will be cleared.	0
7	R	EOC Occur Check [START/EOC pair] This signal available when user coose ADC START and ADC EOC pair latch. After ADC START, if ADC EOC not occured this bit set 1. If EOC occured or EOC Reset set this bit set 0.	0
6	R	FIFO Overflow "1" represents FIFO is overflowed. If new data arrive in overflowed status, old data are deleted and new data are stored inside FIFO.	0
5	R	FIFO Full 1: FIFO is Full 0: FIFO is not Full	0
4	R	FIFO Empty 1: FIFO is Empty 0: FIFO is not empty	1
3 : 1	R	FIFO Level (0~4)	0
0	R	ADC Data Ready 1: ADC Data is valid 0: ADC Data is not ready	0

23.2.5 ADC Control Register2 (ADCCTRL2)

Address: 0xA002_3810

Bit	R/W	Description	Default Value
31 : 5	R	Reserved	-
4	R/W	EOC Reset 0: Disable 1: Enable This signal available when user coose ADC START and ADC EOC pair latch. After ADC START, if ADC EOC not occured this bit used for Controller IDLE state.	0
3:1	R	Reserved	-
0	R/W	Latch Select 0: EOC latch After ADC START, data latch is occured at every EOC occured. 1: ADC START and ADC EOC pair latch After ADC START, first EOC makes data latch is occured once. After first EOC, data latch is not occured at every EOC.	0

24 TFT LCD CONTROLLER

24.1 Introduction

LCD Controller is composed of Register, Timing Generation, FIFO Control, and Sync Control. and FIFO Control blocks are for reading frame memory data, and Sync Control block is for VGA mode. Timing Generation block manages overall control of timing control.

The LCD Controller handles the synchronous LCD interface. It provides timing and data for constant graphics refresh to a TFT LCD display. It supports a wide variety of full-color display types and sizes by use of programmable timing controls.
Graphics data is processed and stored in frame buffers.
A frame buffer is a contiguous memory block in the system. A built-in DMA engine supplies the graphics data to the external LCD device. The DMA engine provides a constant flow of data from the frame buffer(s) to the external LCD panel. In addition, CPU access is provided to read and write registers via the APB Bus.

The frame data for the display output is fetched from memory over the AHB interface.

The Timing Generation block is responsible for generating the correct external timing.

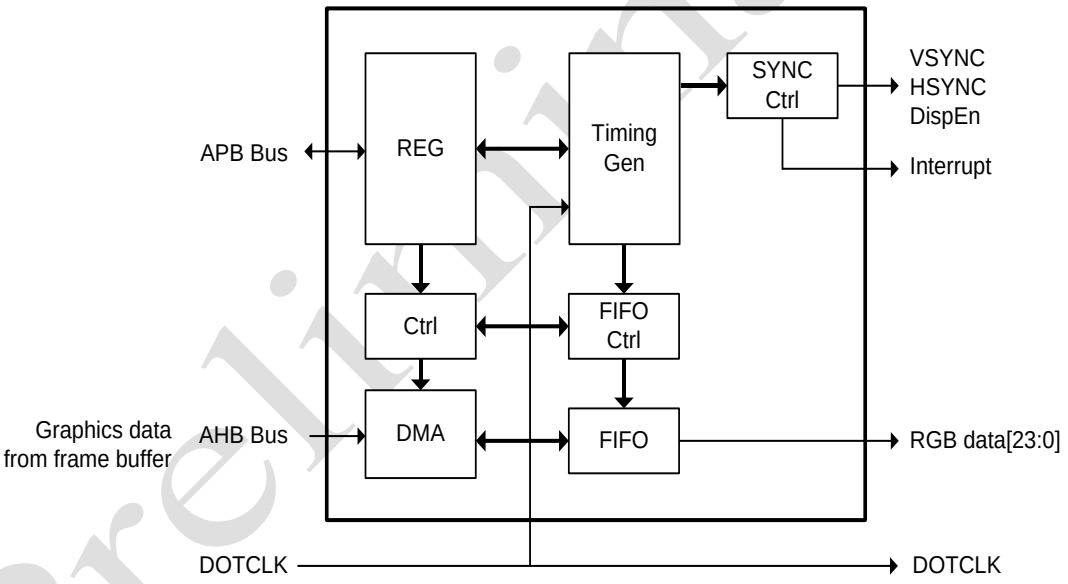


Figure 24-1 LCD Controller Block Diagram

24.2 Features

General features of the LCD Controller include:
- Supports up to 24-bit data output; 8 bits-per-pixel (RGB).
- Supports up to SVGA(800x600) resolution.
- Supports TFT color displays.
- Internal Color Bar Generator
- Programmable timing for different display panels.
- AHB bus master interface to access frame buffer.
- A page-flip double buffering mechanism, synchronizing read and write access to system memory, to prevent tearing effects.

24.3 Functional Description

24.3.1 LCD clock source and divider

The following Figure 24-2 shows the LCD clock and the clock sources controller by lcd_clk_sel and lcd_clk_div_val control bits.
(for details, see Section4.2, *Clock control*).

The DOTCLK is also used by the LCD display and continuously toggles as long as the reference clock is enabled.

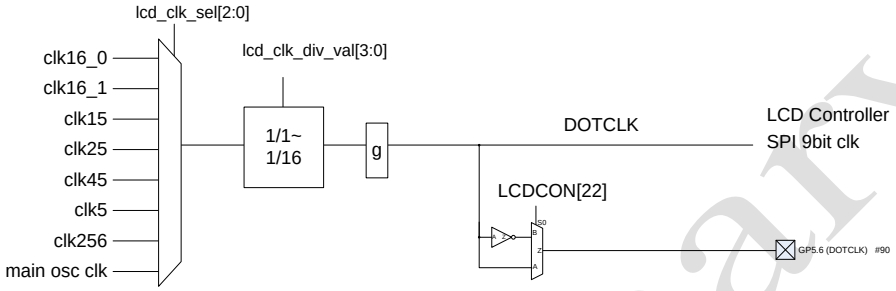


Figure 24-2 LCD Clock

24.3.2 Double buffering

It is preferable to have at least two frame buffers(front buffer, back buffer). A flip occurs, the display delays until the vertical synchronization is occurred. The delay is necessary to ensure that the back buffer is not written on before it is finished being displayed. This synchronization means that tearing effects are avoided when using double buffering.

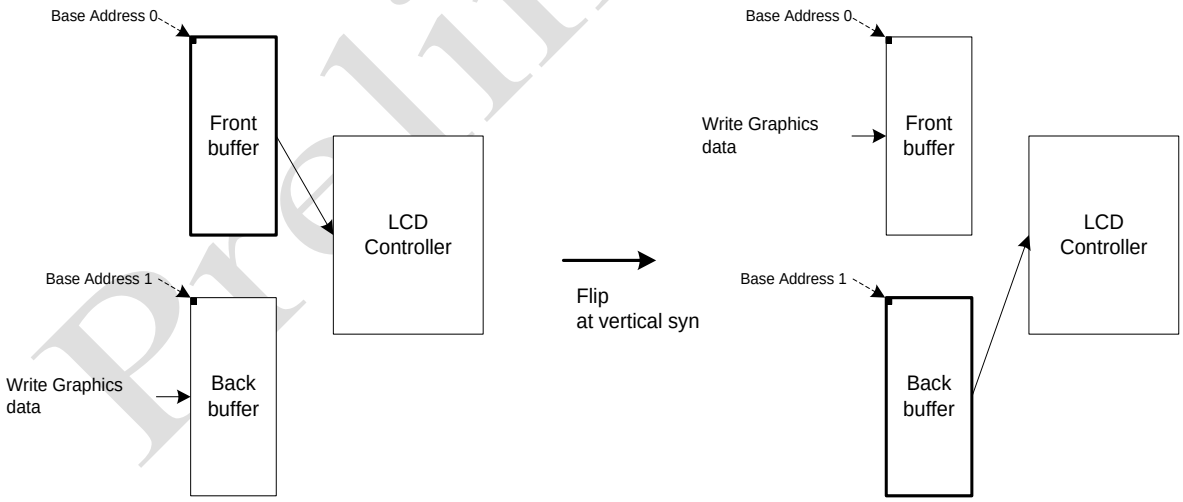


Figure 24-3 Flipping Structure with double buffering

Double-buffering is enabled if the bit 19 of LCD control register(LCDCON) is set. In this case, the setting of the software flip request in the Flip Control register allows creating double-buffed video displays at each LCD vertical synchronization.

Optionally, up to quad buffering is configurable through a set of base address registers that contains the start address of each frame buffer (LCDBADR0, LCDBADR1, LCDBADR2, LCDBADR3 registers). The configuration of the number of frame buffer is determined by the bits 7:6 of the Flip control register.

24.3.3 LCD Interrupt

The LCD controller generates an interrupt at start of the vertical synchronization. The interrupt can be used to reprogram the base address when generating double-buffered video

24.3.4 HSYNC, VSYNC

The HSYNC toggles after all pixels in a horizontal line have been transmitted to the LCD and the timings of the HSYNC is programmable through LCDHT, LCDHS, and LCDHA registers.

The HSYNC can be programmed to be synchronized with the rising or falling edge of DOTCLK. This is achieved by inverting DOTCLK. Its polarity is also programmable.

The VSYNC toggles after all lines in a frame have been transmitted to the LCD and the timings of the VSYNC is programmable through LCDVT, LCDVS, and LCDVA registers.

The VSYNC can be programmed to be synchronized with the rising or falling edge of DOTCLK. This is achieved by inverting DOTCLK. Its polarity is also programmable.

See Section 24.3.6, *VGA Timings*, for detailed information about the timing configurations.

Below diagram shows sync signal timings of 640 by 480 definition depending on Horizontal Total, Sync Start(End), Active Start(End), Vertical Total, Sync Start(End), Active Start(End) register settings. HSYNC and VSYNC signals are low active in default, and [5:4] bits of LCD control register can control their active polarity. Horizontal and vertical active signals are high active.

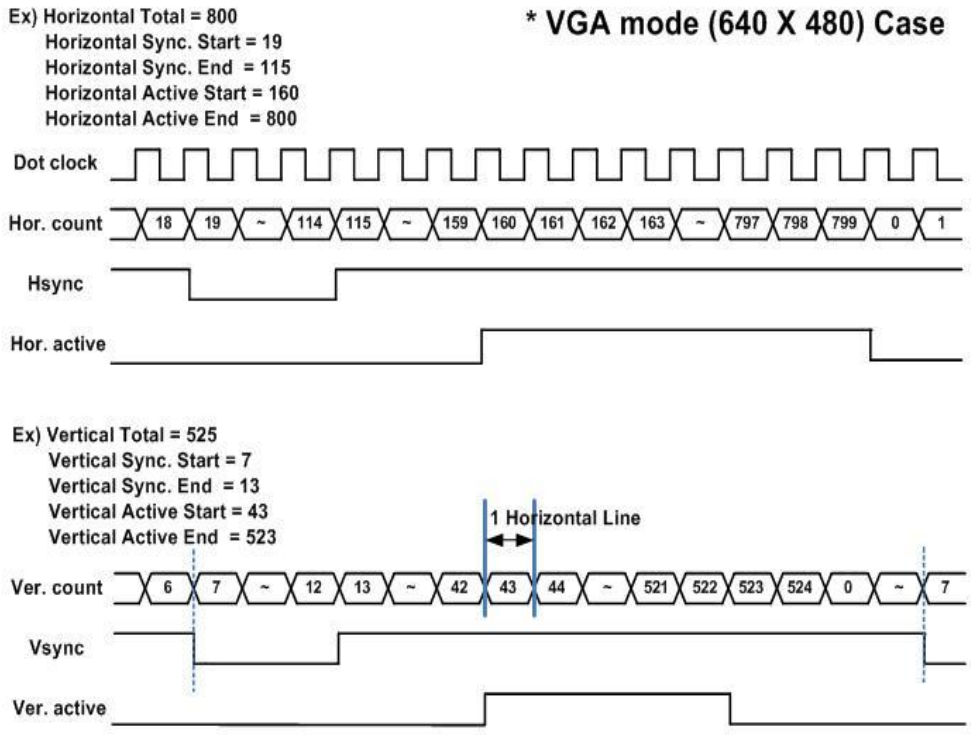


Figure 24-4 LCDC Horizontal, Vertical Sync / Active Signal Timing

24.3.5 DISPEN (Hor.active)

This signal is used to signal the external LCD device that the data is valid on the data bus(R[7:0], G[7:0], B[7:0]). The DISPEN can be programmed to be synchronized with the rising or falling edge of DOTCLK. This is achieved by inverting DOTCLK.

24.3.6 VGA Timings

The following timing parameters can be programmed:

- Horizontal front and back porch
- Horizontal synchronization pulse width
- Number of pixels per line
- Vertical front and back porch
- Vertical synchronization pulse width
- Number of lines per frame

Table 24-1 Typical VGA Timings

Format	*Dot Clock (MHz)*	*Horizontal (in Pixels)*				*Vertical (In Lines)*			
		Active Video THd	*Front Porch THf*	*Sync Pulse THp*	*Back Porch THb*	*Active Video TVd*	*Front Porch TVf*	*Sync Pulse TVp*	*Back Porch TVb*
QVGA 240x320	5.33	240	-	-	-	320	-	-	-
WQVGA 480x272	9.000	480	-	-	-	272	-	-	-
VGA 640X480, 60Hz	25.175	640	16	96	48	480	11	2	31
WVGA 800x480	33.3	800	-	-	-	480	-	-	-
SVGA 800x600, 60Hz	40.000	800	40	128	88	600	1	4	23

Horizontal Timing registers

LCDHT, LCDHS and LCDHA registers control the Horizontal Synchronization pulse width(THp), the Horizontal Front Porch(THf) period, the Horizontal Back Porch(THb) period, and the Pixels-Per-Line(THd).

The timing configuration uses the following equations:

LCDHT[10:0] = THf + THp + THb + THd
LCDHS[26:16] = THf
LCDHS[10:0] = THf + THp
LCDHA[26:16] = THf + THp + THb
LCDHA[10:0] = THf + THp + THb + THd

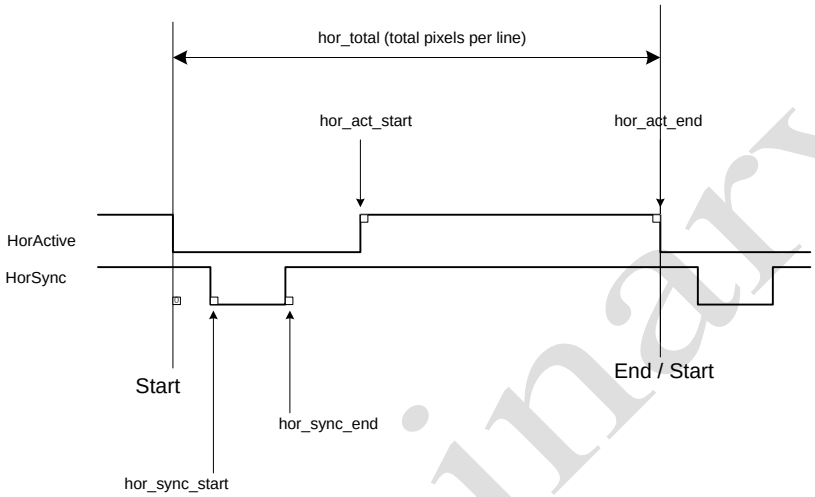


Figure 24-5 Horizontal Timing

Vertical Timing registers

LCDVT, LCDVS and LCDVA registers control the Vertical Synchronization pulse width(TVp), the Vertical Front Porch(TVf) period, the Vertical Back Porch(TVb) period, and the Lines-Per-Frame(TVd).

The timing configuration uses the following equations:

LCDVT[10:0] = TVf + TVp + TVb + TVd
LCDVS[26:16] = TVf
LCDVS[10:0] = TVf + TVp
LCDVA[26:16] = TVf + TVp + TVb
LCDVA[10:0] = TVf + TVp + TVb + TVd

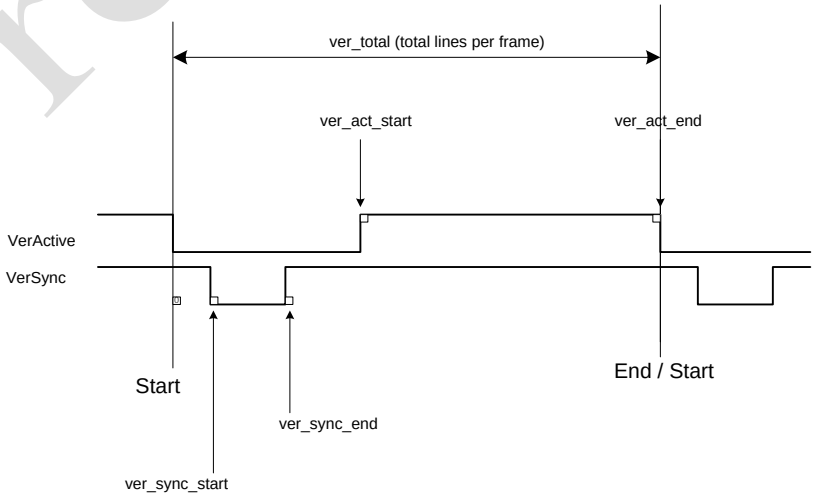


Figure 24-6 Vertical Timing

Here are some example settings for some common display resolutions:

Table 24-2 Register Values for VGA timing

Register	LCDBA	LCDHT	LCDHS	LCDHA	LCDVT	LCDVS	LCDVA	LCDCON
640x480 (800x525)	00000000	00000320	00130073	00A00320	0000020D	0007000D	002B020B	00080000
800x600 (1056x628)	00000000	00000420	002300C3	01000420	00000274	0004000A	001A0272	00080000

* Register Values are Hexa-Decimal.
* Memory Read Request is based on half position of FIFO.
* Screen Display Mode is based on Normal operation.
* H(V)SYNC. Output Polarity is based on Low Active.
* H(V)SYNC. Output Select is based on SYNC. Output generated from Internal block

24.3.7 Color Bar Test Pattern Generation Block

Color bar test pattern generation is activated and request generation, address generation, and FIFO control blocks are deactivated when [1:0] bits of LCD control register is “01”. Video data mux & serialization block outputs selected color bar pattern video data. Color bar pattern is generated in black, white, yellow, blue-green, green, purple, red, and blue color order from left, and has even distribution regardless of screen definition. If active section is not exact multiple of 8, right side of the screen can have black outputs.

24.4 Register Description

LCD Controller Register Summary

Table 24-3 LCD Controller Registers Table

Absolute Address	Register Name	Description
0x8002_2404h	LCD Horizontal Total Register (LCDHT)	Horizontal Total Scan Value including horizontal active and black section
0x8002_2408h	LCD Horizontal Sync. Start / End Register (LCDHS)	Start(End) value in Horizontal Sync section
0x8002_240Ch	LCD Horizontal Active Start / End Register (LCDHA)	Start(End) value in Horizontal active section
0x8002_2410h	LCD Vertical Total Register (LCDVT)	Vertical Total scan value including Vertical Active and blank section
0x8002_2414h	LCD Vertical Sync. Start/End Register (LCDVS)	Start(End) value of Vertical Sync section
0x8002_2418h	LCD Vertical Active Start/End Register (LCDVA)	Start(End) value of Vertical active section
0x8002_241Ch	LCD Display Current X / Y Position Register (LCDXY)	Horizontal/Vertical Counter value
0x8002_2420h	LCD Status Register (LCDSTAT)	Sync status of LCD controller
0x8002_2424h	LCD Control Register (LCDCON)	Controls display, sync, memory, and FIFO mode of LCD
0x8002_2430h	LCDC Base Address 0	Designate the start point of screen
0x8002_2434h	LCDC Base Address 1	Designate the start point of screen
0x8002_2438h	LCDC Frame sync. Counter	Count the number of frame syncs.
0x8002_243Ch	LCD Horizontal Width	Decide the LCD’s horizontal width
0x8002_2440h	LCD Flip Command	Process flip operation
0x8002_2444h	LCDC Base Address 2	Configure frame buffer start point
0x8002_2448h	LCDC Base Address 3	Configure frame buffer start point

24.4.1 LCD Horizontal Total Register(LCDHT)

Horizontal total scan value including horizontal active and blank section.

Address : 0x8002_2404h

Bit	R/W	Description	Default Value
31 : 11	R	Reserved	-
10 : 0	R/W	Horizontal Total The value loaded into this field is the total pixel counts per line.	000h

24.4.2 LCD Horizontal Sync. Start / End Register(LCDHS)

Start(End) value of horizontal sync section.

Address : 0x8002_2408h

Bit	R/W	Description	Default Value
31 : 27	R	Reserved	-
26 : 16	R/W	Horizontal Sync Start The value loaded into this field is the value of horizontal sync period start by the horizontal counter	000h
15 : 11	R	Reserved	-
10 : 0	R/W	Horizontal Sync End The value loaded into this field is the value of horizontal sync period end by the horizontal counter	000h

24.4.3 LCD Horizontal Active Start / End Register(LCDHA)

Start(End) value of horizontal active section.

Address : 0x8002_240Ch

Bit	R/W	Description	Default Value
31 : 27	R	Reserved	-
26 : 16	R/W	Horizontal Active Start The value loaded into this field is the value of horizontal active period start by the horizontal counter	000h
15 : 11	R	Reserved	-
10 : 0	R/W	Horizontal Active End The value loaded into this field is the value of horizontal active period start by the horizontal counter	000h

24.4.4 LCD Vertical Total Register(LCDVT)

Vertical total scan value including vertical active and blank section.

Address : 0x8002_2410h

Bit	R/W	Description	Default Value
31 : 11	R	Reserved	-
10 : 0	R/W	Vertical Total The value loaded into this field is the value of the total vertical line counts.	000h

24.4.5 LCD Vertical Sync. Start / End Register(LCDVS)

Start(End) value of vertical Sync section.

Address : 0x8002_2414h

Bit	R/W	Description	Default Value
31 : 27	R	Reserved	-
26 : 16	R/W	Vertical Sync Start The value loaded into this field is the value of vertical sync period start by the vertical counter	000h
15 : 11	R	Reserved	-
10 : 0	R/W	Vertical Sync end The value loaded into this field is the value of vertical sync period end by the vertical counter	000h

24.4.6 LCD Vertical Active Start / End Register(LCDVA)

Start(End) value of Vertical Active section.

Address : 0x8002_2418h

Bit	R/W	Description	Default Value
31 : 27	R	Reserved	-
26 : 16	R/W	Vertical Active Start The value loaded into this field is the value of vertical active period start by the vertical counter	000h
15 : 11	R	Reserved	-
10 : 0	R/W	Vertical Active end The value loaded into this field is the value of vertical active period end by the vertical counter	000h

24.4.7 LCD Display Current X / Y Position Register(LCDXY)

Display current X position register is read-only, and represent the horizontal counter value. Display current Y position register is also read-only, and represent the vertical counter value.

Address : 0x8002_241Ch

Bit	R/W	Description	Default Value
31 : 27	R	Reserved	-
26 : 16	R	The value loaded into this field is the value of the vertical counter.	000h
15 : 11	R	Reserved	-
10 : 0	R	The value loaded into this field is the value of the horizontal counter.	000h

24.4.8 LCD Status Register(LCDSTAT)

LCD status register is read-only. It shows the sync status of LCD controller. Both horizontal sync and vertical sync signal have low active status when control register [21:20] bits are “00”. However, both horizontal and vertical active signal have high active status regardless of control register [21:20] value.

Address : 0x8002_2420h

Bit	R/W	Description	Default Value
31 : 7	R	Reserved.	-
6	R	Current Display Bank 0 : BANK0 , 1 : BANK1	0b
5 : 4	R	Reserved.	1b
3	R	Vertical Active (active high)	0b
2	R	Vertical Sync	1b
1	R	Horizontal Active (active high) .	0b
0	R	Horizontal Sync	1b

24.4.9 LCD Control Register(LCDCON)

LCD control register is used to control the operation mode of LCDC

* Frame Memory Bank <n> Ping-Pone Enable
: Activate/deactivate the frame memory bank switches due to LCD flop register setting
- When deactivated, LCD Frame Memory Bank is fixed
- When activated, LCD frame memory bank is switched by LCD flip register.

Address : 0x8002_2424h

Bit	R/W	Description	Default Value
31 : 25	R	Reserved	-
24	R/W	Software Reset. 0 = Normal operation 1=Reset,.	1b
23	R	Reserved	-
22	R/W	Invert DOTCLK output 0 = Normal 1 = Inverted	-
21	R/W	HSYNC. Output Polarity. 0 = Low Active 1 = High Active	0b
20	R/W	VSYNC. Output Polarity. 0 = Low Active 1 = High Active	0b
19	R/W	Frame buffer double buffering. 0 = Disabled 1 = Enabled	0b
18 : 17	R/W	FIFO Request Control(Total depth : 256) 00 : one half request(128) 01 : one fourth request(64) 10 : one eighth request(32) 11 : Don't use	00b
16 : 15	R	Reserved	0b
14	R/W	When RGB 32bit mode, Input data sequence : 0 = dRGB 1 = RGBd	0b
13 : 12	R/W	Frame data format 00 = undefined. 01 = 16bpp, 5:6:5 mode, RGB 16bit 10 = 24bpp, 8:8:8 mode, RGB 32bit 11 = undefined.	0b
11 : 10	R	Reserved	-
9 : 8	R	Bus Burst Length Select. 10 : 16burst 01 : 32 burst 00 : Max burst(256 burst)	-
7 : 5	R	Reserved	-
4	R/W	Use hwidth register	0b
3 : 2	R/W	Reserved	-
1 : 0	R/W	Screen Display Mode Control. 00=Normal operation. 01=Regular Pattern Generation 1x=Screen off	00b

24.4.10 LCD Base Address 0 Register (LCDBADR0)

Address : 0x8002_2430h

Bit	R/W	Description	Default Value
31 : 2	R/W	Base Address 0 This is the start address of the frame data in memory and is word aligned. Only SDRAM area is available	0000h
1 : 0	R	Reserved	-

24.4.11 LCD Base Address 1 Register (LCDBADR1)

Address : 0x8002_2434h

Bit	R/W	Description	Default Value
31 : 2	R/W	Base Address 1 This is the start address of the frame data in memory and is word aligned. Only SDRAM area is available	0000h
1 : 0	R	Reserved	-

24.4.12 LCD Frame Sync. Count Register (LCDFRAMECNT)

Address : 0x8002_2438h

Bit	R/W	Description	Default Value
31 : 0	R/W	Frame Sync. Count	0h

24.4.13 LCD Horizontal Width Register (LCDHWIDTH)

Address : 0x8002_243Ch

Bit	R/W	Description	Default Value
31 : 12	R	Reserved	-
11 : 0	R/W	Horizontal Width	400h

24.4.14 LCD Flip Control Register (LCDFCTL)

Address : 0x8002_2440h

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 6	R/W	Select the number of Frame buffer 01 : use 2 Frame buffers 10 : use 3 Frame buffers 11 : use 4 Frame buffers	01b
5	R	Reserved	-
4	R/W	Software flip enable	0
3:2	R	Current Frame buffer number	0
1	R	Reserved	-
0	R/W	Software flip request 1 : set 0 : cleared by H/W automatically	0

24.4.15 LCD Base Address 2 Register (LCDBADR2)

Address : 0x8002_2444h

Bit	R/W	Description	Default Value
31 : 2	R/W	Base Address 2 This is the start address of the frame data in memory and is word aligned. Only SDRAM area is available	0000h
1 : 0	R	Reserved	-

24.4.16 LCD Base Address 3 Register (LCDBADR3)

Address : 0x8002_2448h

Bit	R/W	Description	Default Value
31 : 2	R/W	Base Address 3 This is the start address of the frame data in memory and is word aligned. Only SDRAM area is available	0000h
1 : 0	R	Reserved	-

25 JPEG DECODER

25.1 Features

- 640x480 4:2:0 format 1frame(lena image) 35ms 안에 decoding 가능
- ISO 10918-2 base line JPEG decoder
- Only support typical Huffman table defined in annex K of standard.
- Supports YCbCr 4:2:2 format
- Supports YCbCr 4:2:0 format
- Maximum resolution:2048x2048

25.2 Block Description

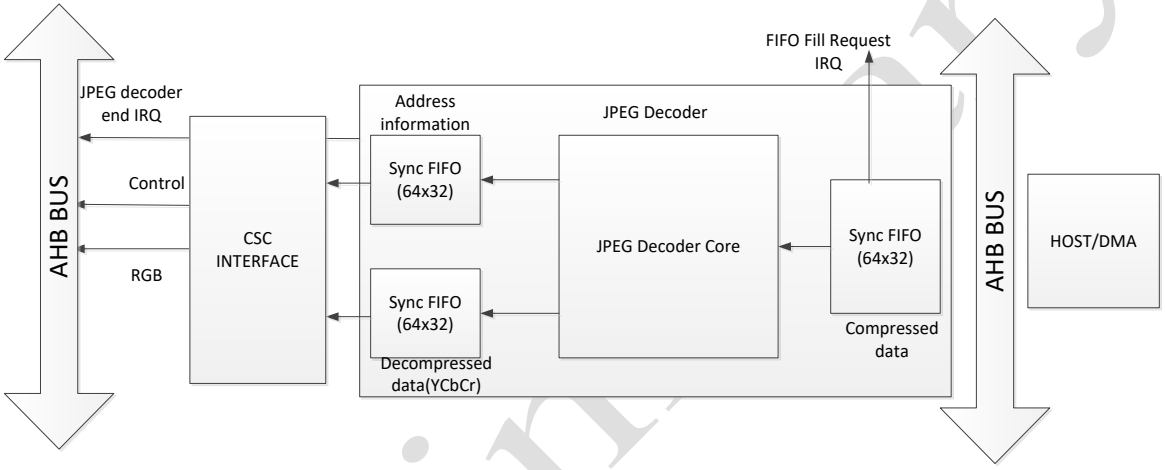


Figure 25-1 JPEG Decoder Block Diagram

There are three 64x32 FIFOs in JPEG Decoder for storing JPEG Image data , decompressed DATA (YCbCr) and address informant of MCU(Minimum Code Unit). The FIFO's level is decided by setting value of JDFCON Register[6:0]

During the operation of JPEG decoder, FIFO Fill Request IRQ (Level Trigger) is triggered in decoder by JPEG Image data Request. IRQ is held when data fills the FIFO up to the FIFO level set in JDCTRL register and cleared automatically when the number of DATA in FIFO is more than the level of FIFO. IRQ reoccurs when number of data in FIFO is below the FIFO level.

During the operation of JPEG decoder, FIFO Fill Request IRQ (Level Trigger) is triggered in decoder by JPEG Image data Request. IRQ is held when data fills the FIFO up to the FIFO level set in JDCTRL register and cleared automatically when the number of DATA in FIFO is more than the level of FIFO. IRQ reoccurs when number of data in FIFO is below the FIFO level.

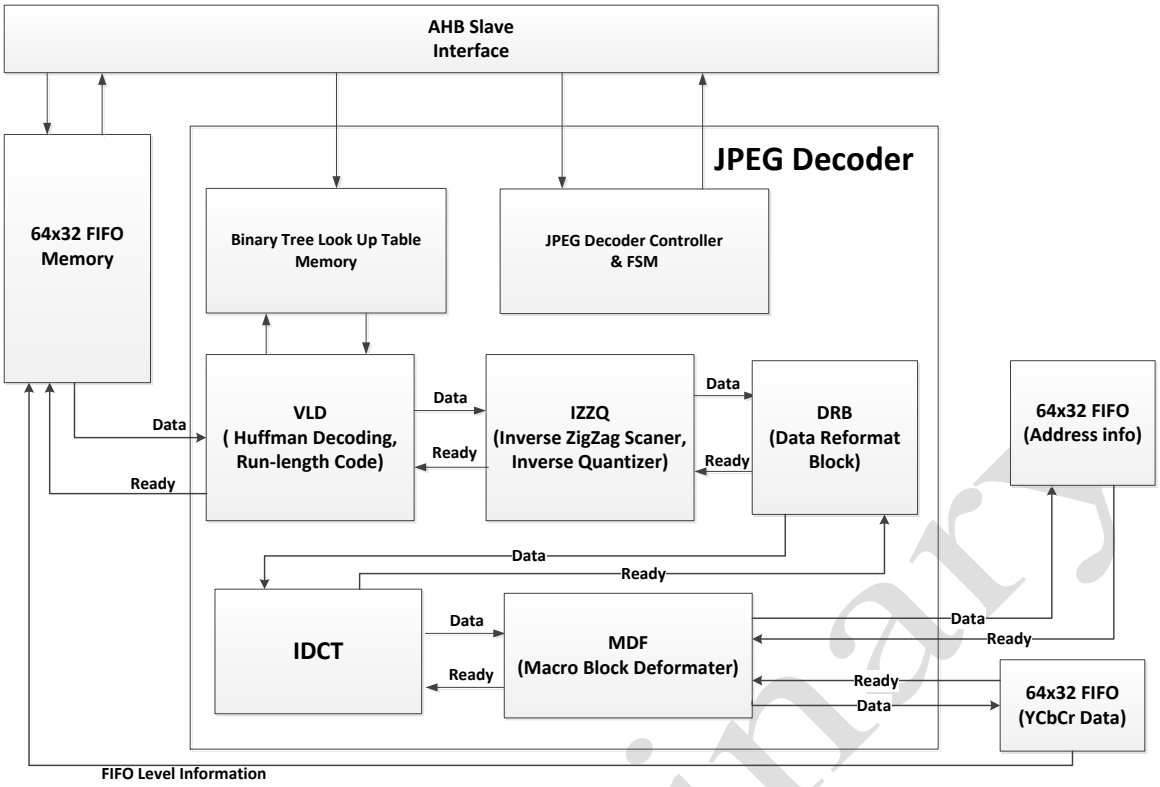
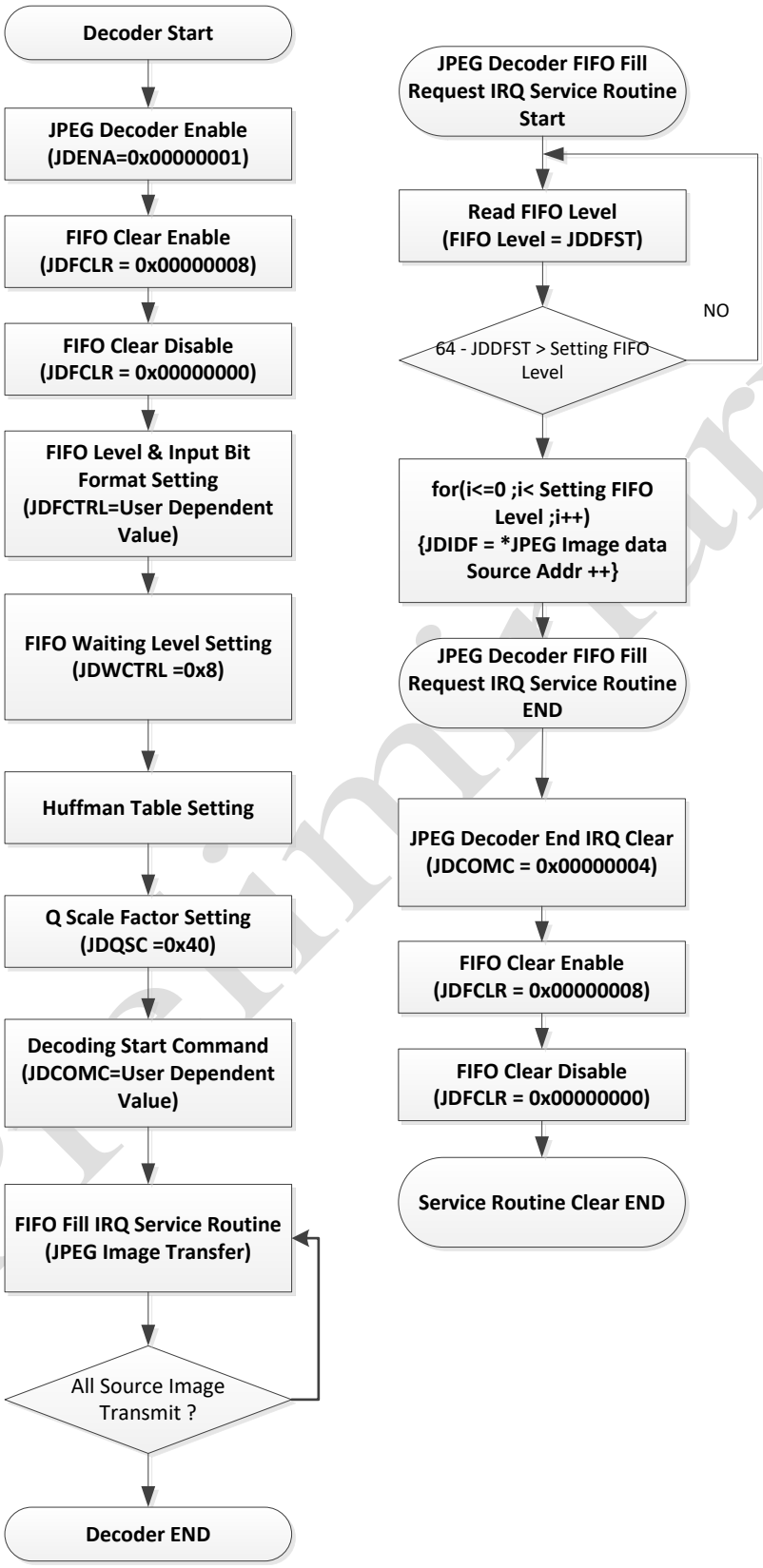


Figure 25-2 Decoder Core Block Diagram

Each JPEG Decoder block transmit data output to the next stage operation block based on ready signal generated by the next stage operation block. JPEG enters waiting state when a JPEG image input stream is waiting due to external system condition or output data is filling the FIFO up to the level set in JDWCON register. JPEG Decoder is restarted from the waiting point when Input Image stream is resumed or numbers of output data in FIFO is below the programmed FIFO level.

25.3 Functional Description



25.4 Register Description

25.4.1 JPEG Decoder Quantization Scale Control Register (JDQSC)

Address: 0xA004_023C

Bit	R/W	Description	Default
31 : 12	R	Reserved.	
11 : 0	W	JPEG Quantization Scale Control Scale quantization table value in the JPEG image header. With 64 as base value, larger number increases Q table value and smaller number decreases Q table value If other value other than 64 is used, image distortion may occur under the condition of different value setting.	000h

25.4.2 JPEG Decoder Command Control Register (JDCC)

Address: 0xA004_0240

Bit	R/W	Description	Default
31 : 3	R	Reserved.	
2	W	JPEG Decoder End IRQ Clear 1:End IRQ Clear 0:IDLE JPEG Decoder End IRQ is used as JICIRQ source. This bit is set when both JPEG Decoder End IRQ and JICIRQ are cleared. After changing to '1', this bit will toggle back to '0' at the next clock. After this bit is set to '1', it is automatically cleared to '0' at the next clock. *JPEG Decoder End IRQ must be cleared for JPEG decoder to decode the next image	0b
1	W	DECODING IMAGE FORMAT 1:YCBCR 420 0:YCBCR 422	0b
0	W	Decoding Start 1:Decoding Start 0:IDLE If JDENA Register[0] is set to '1', JPEG decoder shall operate when this bit changes to '1'. The first JPEG Decoder FIFO Fill Request IRQ is initiated by setting this bit to '1'. After decoder starts the decoding operation, this bit will be cleared automatically.	0b

25.4.3 JPEG Decoder Y DC NODE Table (JDYDCNT)

Address: 0xA004_0800 ~ 0xA004_0830

Bit	R/W	Description	Default
31 : 18	R	Reserved.	
17 : 0	W	Y DC Node Table for Huffman Decoding The node table of Y DC binary tree used for Huffman decoding	000h

25.4.4 JPEG Decoder Y DC Leaf Table (JDYDCLT)

Address : 0xA004_0C00 ~ A004_0C30

Bit	R/W	Description	Default
31 : 8	R	Reserved	-
7 : 0	W	Y DC LEAF Table for Huffman Decoding The leaf table of Y DC binary tree used for Huffman decoding	-

25.4.5 JPEG Decoder Y AC Node Table (JDYACNT)

Address : 0xA004_2800 ~ A004_2A88

Bit	R/W	Description	Default
31 : 18	R	Reserved	-
17 : 0	W	Y AC Node Table for Huffman Decoding The node table of Y AC binary tree used for Huffman decoding	-

25.4.6 JPEG Decoder Y AC Leaf Table (JDYACLT)

Address : 0xA004_3000 ~ A004_3288

Bit	R/W	Description	Default
31 : 8	R	Reserved	-
7 : 0	W	Y AC LEAF Table for Huffman Decoding The leaf table of Y AC binary tree used for Huffman decoding	-

25.4.7 JPEG Decoder UV DC Node Table (JDUVDCNT)

Address : 0xA004_4800 ~ A004_4830

Bit	R/W	Description	Default
31 : 18	R	Reserved	-
17 : 0	W	UV DC Node Table for Huffman Decoding The node table of UV DC binary tree used for Huffman decoding	-

25.4.8 JPEG Decoder UV DC Leaf Table (JDUVDCLT)

Address : 0xA004_5000 ~ A004_5030

Bit	R/W	Description	Default
31 : 8	R	Reserved	-
7 : 0	W	UV DC LEAF Table for Huffman Decoding The leaf table of UV DC binary tree used for Huffman decoding	-

25.4.9 JPEG Decoder UV AC Node Table (JDUVACNT)

Address : 0xA004_6800 ~ A004_6A88

Bit	R/W	Description	Default
31 : 18	R	Reserved	-
17 : 0	W	UV AC Node Table for Huffman Decoding The node table of UV AC binary tree used for Huffman decoding	-

25.4.10 JPEG Decoder UV AC Leaf Table (JDUVACLT)

Address : 0xA004_7000 ~ A004_7288

Bit	R/W	Description	Default
31 : 8	R	Reserved	-
7 : 0	W	UV AC LEAF Table for Huffman Decoding The leaf table of UV AC binary tree used for Huffman decoding	-

25.4.11 JPEG Decoder Status Register (JDSTAT)

Address : 0xA004_8000

Bit	R/W	Description	Default
31 : 4	R	Reserved	-
3	R	JPEG Decoder Finished	0b
2	R	JPEG Decoder MCU Decoding	0b
1	R	JPEG Decoder Header Parsing	0b
0	R	JPEG Decoder Ready	0b

25.4.12 JPEG Decoder IRQ Status Register (JDIRQSTAT)

Address : 0xA004_8004

Bit	R/W	Description	Default
31 : 3	R	Reserved.	-
2	R	JPEG Decoder Timeout Interrupt is generated when a time-out value is reached due to an abnormal function or compressed input data failure for some time. Even if terminated by time-out, software reset and the interrupt clearing processed to resume to initial state.	0b
1	R	JPEG Decoder FIFO Fill Request IRQ Interrupt is triggered when the compressed data in JPEG Decoder Internal FIFO is not filled up to the level configured in JDCTRL Register [6:0].	0b
0	R	JPEG Decoder End IRQ Display the end point of JEPG Decoder. after JPEG Decoder decodes the required number of MCU in decoder, this IRQ shall occur when JPEG EOF Flag is arrives in Decoder. *this interrupt is inputted to JPEG image capturer and used for the source of JICIRQ.	0b

25.4.13 JPEG Decoder Data FIFO Status Register (JDDFSTAT)

Address : 0xA004_8008

Bit	R/W	Description	Default
31 : 7	R	Reserved.	-
6 : 0	R	Current FIFO Level Status Show current input data FIFO level. When input data is written into the FIFO, input data must be written within the value of Current FIFO Level Status of under 3Fh. If exceeded, new subsequent data will overwrite the existing data in FIFO.	00h

25.4.14 JPEG Decoder Enable Register (JDENA)

Address : 0xA004_8010

Bit	R/W	Description	Default
31 : 1	R	Reserved.	-
0	R/W	JPEG Decoder Enable This bit enables JPEG decoder. After this bit is set to 1, JPEG Decoder shall start data decoding when bit 0 of JDCOMCON register is set to '1'.	0b

25.4.15 JPEG Decoder FIFO Clear Register (JDFCLR)

Address : 0xA004_8014

Bit	R/W	Description	Default
31: 4	R	Reserved.	-
3	R/W	FIFO Clear 1:ALL FIFO Clear 0:IDLE	0b
2 : 0	R	Reserved	-

25.4.16 JPEG Decoder FIFO Control Register (JDFCON)

Address : 0xA004_8018

Bit	R/W	Description	Default
31 : 10	R	Reserved	-
9	R/W	Input data Format Selection 1:Big Endian Format 0:Little Endian Format	0b
8 : 7	R	Reserved	-
6 : 0	R/W	Data FIFO Threshold Level This field identifies the threshold level of data FIFO. FIFO Fill Request Interrupt occurs when number of data into FIFO is below the value set in this field. lower value must be used for setting values other than FIFO size(64)	00h

25.4.17 JPEG Decoder Waite Control Register (JDWCON)

Address : 0xA004_801C

Bit	R/W	Description	Default
31 : 7	R	Reserved	-
6 : 0	R	WAITE FIFO Threshold Level This field determines the decoding data output FIFO level. Decoder goes into waiting mode when the number of data stored in FIFO is 8 times the WAITE FIFO Threshold Level value and operates again when the remaining data in FIFO is below the value of WAITE FIFO Threshold Level *8 The value range is between a minimum 1 to a maximum 8, the smaller the value, the more frequent the decoder has to wait.	08h

25.4.18 JPEG Decoder Software Reset Register (JDSRST)

Address : 0xA004_8024

Bit	R/W	Description	Default
31 : 1	R	Reserved.	-
0	R/W	Software Reset 1:IDLE 0:Reset This bit forces a decoder initialization when JPEG decoder is not operating under normal condition by taking in wrong data. The decoder shall enter reset state when this bit is set to '0', and operation starts again when this bit is set to '1'.	1b

25.4.19 JPEG Decoder Version Information Register (JDVERINFO)

Address : 0xA004_8028

Bit	R/W	Description	Default
31 : 0	R/W	JPEG Decoder Version	-

25.4.20 JPEG Decoder CSC Base Address Register (JDCSCBASEADDR)

Address : 0xA004_802C

Bit	R/W	Description	Default
31 : 0	R/W	JPEG Decoder RGB data Base address for transferring	C2000000 h

25.4.21 JPEG Decoder Stride Size Register (JDCSTRID)

Address : 0xA004_8030

Bit	R/W	Description	Default
31 : 0	R/W	JPEG Decoder Stride size Configure maximum vertical pixel size set in the crtc.	400h

25.4.22 JPEG Decoder RGB565 mode and Timeout count enable (JDCRGBTIMEOUT)

Address : 0xA004_8034

Bit	R/W	Description	Default
31 : 2	R	Reserved	-
1	R/W	JPEG Decoder timeout counter ctrl 0 : disable Timeout counter 1 : enable Timeout counter	0h
0	R/W	JPEG Decoder RGB888/565 mode 0 : RGB888 mode 1 : RGB565 mode	0h

25.4.23 JPEG Decoder Timeout counter Register (JDCTIMEOUTCNT)

Address : 0xA004_8038

Bit	R/W	Description	Default
31 : 0	R/W	JPEG Decoder timeout counter register When JPEG abnormally stop due to corrupted data input, time-out is detected with time-out value.	8000000h

25.4.24 JPEG Decoder Timeout counter clear (JDCTIMEOUTCLR)

Address : 0xA004_803C

Bit	R/W	Description	Default
31 : 1	R	Reserved	-
0	R/W	JPEG Decoder timeout counter clear register When timer-out is occurred, it must be cleared by this bit to continue to run. 1 : timeout clear set 0 : timeout clear off	0h

25.4.25 JPEG Decoder Input Data FIFO Register (JDIDF)

Address : 0xA004_9000

Bit	R/W	Description	Default
31 : 0	W	INPUT DATA FIFO Compressed data(JPEG Input stream) FIFO	-

26 USB DEVICE

USB Device of *adStar-L* supports 2.0 Full-speed (12Mbps) and consists of 5 endpoints.

USB Protocol is supported in hardware, and provides automatically data retry, data toggle, and power management (suspend and resume). The USB device includes PHY.

26.1 Features

- USB 2.0 Full Speed(12Mbps)
- 5 Endpoints
- USB protocol support in hardware
- Provides suspend and resume signaling

Table 26-1 Endpoint List

Endpoint	*Max Size (bytes)*	*Direction*	*Transaction Type*
0	16	IN/OUT	Control
1	64	OUT	Bulk
2	64	IN	Bulk
3	16	OUT	Interrupt
4	16	IN	Interrupt

26.2 Register Summary

Table 26-2 USB Core Register List

Register	*Address*	*R/W*	*Description*	*Default Value*
USBFA	0xA0001800	R/W	Function address register	0x00
USBPM	0xA0001804	R/W	Power management register	0x00
USBEPI	0xA0001808	R/W	Endpoint interrupt register	0x00
USBINT	0xA0001810	R/W	USB interrupt register	0x00
USBEPIEN	0xA0001814	R/W	Endpoint interrupt enable register	0x1F
USBINTEN	0xA0001818	R/W	USB interrupt enable register	0x04
USBLBFN	0xA000181C	R	Frame number1 register	0x00
USBHBFN	0xA0001820	R	Frame number2 register	0x00
USBIND	0xA0001824	R/W	Index register	0x00
USBMP	0xA0001828	R/W	MAXP register	0x00
USBEP0C	0xA000182C	R/W	EP0 control register	0x00
USBIC1	0xA000182C	R/W	EP2, 4 IN Control register1	0x00
USBIC2	0xA0001830	R/W	EP2, 4 IN Control register2	0x00
USBOC1	0xA0001838	R/W	EP1, 3 OUT Control register 1	0x00
USBOC2	0xA000183C	R/W	EP1, 3 OUT Control register 2	0x00
USBLBOWC	0xA0001840	R	Low Byte OEP Write count register	0x00
USBHBOWC	0xA0001844	R	High Byte OEP write count register	0x00
USBEP0D	0xA0001848	R/W	EP0 FIFO data register	0x00
USBEP1D	0xA000184C	R/W	EP1 FIFO data register	0x0000_0000
USBEP2D	0xA0001850	R/W	EP2 FIFO data register	0x0000_0000
USBEP3D	0xA0001854	R/W	EP3 FIFO data register	0x00
USBEP4D	0xA0001858	R/W	EP4 FIFO data register	0x00

26.2.1 USB Function Address Register

USBFAR register holds USB Device address that is assigned by host. MCU stores the data to the register by executing SET_ADDRESS Descript. This value is used for next token.

26.2.2 USB Power Management Register

Power management register is used by Suspend, Resume and Reset signals. Statuses of Suspend and Reset are stored into USB_INTERRUPT register.

26.2.3 USB Interrupt Registers

This register informs statuses of USB Host request and Endpoint..

26.2.4 USB Interrupt Enable Registers

Interrupt enables of each endpoint. Most of interrupts are enabled initially, but suspend interrupt is disabled.

26.2.5 Frame Number Registers

This register holds frame number at the end of frame packet.

26.2.6 Index Register

The index register is used for selecting control register of each endpoint.

26.2.7 MAXP Register

User can configure FIFO size that is times of 8byte. However, user cannot set larger the FIFO size than maximum FIFO size that is provided by each endpoint.

26.2.8 EP0 Control Register

This register represents control and status of Endpoint0.

26.2.9 IN Control Registers

This register represents control and status of IN Endpoint

26.2.10 Out Control Registers

This register represents control and status of OUT Endpoint

26.2.11 Out Write Count Registers

The 2 Out Write Count registers hold write count. The registers hold the number of packets that are used by MCU, if OPOPR bit is set at the OUT endpoint.

26.2.12 Endpoint FIFO Access Registers

The register accesses to an Endpoint FIFO..

26.3 Register Description

26.3.1 USB Function Address Register (USBFA)

Address : 0xA000_1800h

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 8			Reserved	
7	R/W	R/ Clear	ADDUP : ADDR_UPDATE bit. The MCU sets this bit whenever it updates the FUNCTION_ADDR field in this register. The FUNCTION_ADDR field is used after the Status phase of a Control transfer, which is signaled by the clearing of the DATA_END bit in the Endpoint 0 CSR.	0
6 : 0	R/W	R	FUNADD : FUNCTION_ADDR bits. MCU writes address into this bit.	0

26.3.2 USB Power Management Register (USBPM)

Address : 0xA000_1804h

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 4			Reserved	
3	R	Set	UBRST : USB_RESET bit. If USB receives Reset signal from host, USB sets this bit. If the Reset signal remains in bus, this bit keeps holding 1.	0
2	W/R	R	UBRSUM : USB_RESUME bit. In order to initialize Resume signal, MCU configures this bit during 10ms (Max 15ms). In the Suspend mode, USB generates Resume signal during this bit is set.	0
1	R	R/W	UBSPDMOD : SUSPEND_MODE bit. USB configures this bit when enters into Suspend mode. This bit is cleared by following conditions. -MCU clears MCU_RESUME to finish Resume signal. -MCU reads interrupt register 3 when USB_RESUME interrupt is occurred.	0
0	R/W	R	UBENSPD : ENABLE_SUSPEND bit = 1 Enable Suspend mode = 0 Disable Suspend mode (Default) If this bit is set to 0, USB Device does not enter suspend mode.	0

26.3.3 USB Endpoint Interrupt Register (USBEPI)

Address : 0xA000_1808h

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 5			Reserved	
4	R/ Clear	Set	EP4INT : EP4 Interrupt bit. (Interrupt in mode) This bit is for Endpoint4 interrupt. (Refer to USBIC1R, USBIC2R bit) When ICIPR(In Control 1 In Packet Ready bit) bit is cleared When FIFO is flushed. When ICSTSTAL (In Control 1 Sent Stall bit) bit is set.	0
3	R/ Clear	Set	EP3INT : EP3 Interrupt bit. (Interrupt out mode) This bit is for Endpoint3 interrupt. (Refer to USBOC1R, USBOC2R bit) When OCOPR (Out Control 1 Out Packet Ready bit) bit is set. When OCSTSTAL (Out Control 1 Sent Stall bit) bit is set.	0
2	R/ Clear	Set	EP2INT : EP2 Interrupt bit. (Bulk in mode) This bit is for Endpoint2 interrupt. (Refer to USBIC1R, USBIC2R bit) When ICIPR (In Control 1 In Packet Ready bit) bit is clear. When FIFO is flushed. When ICSTSTAL (In Control 1 Sent Stall bit) bit is set.	0
1	R/ Clear	Set	EP1INT : EP1 Interrupt bit. (Bulk out mode) This bit is for Endpoint1 interrupt. (Refer to USBOC1R, USBOC2R bit) When OCOPR (Out Control 1 Out Packet Ready bit) bit is set. When OCSTSTAL (Out Control 1 Sent Stall bit) bit is set.	0
0	R/ Clear	Set	EP0INT : EP0 Interrupt bit. (Control mode) This bit is for Endpoint0 interrupt. (Refer to USBEP0CR bit) EP0OPR bit is set. EP0IPR bit is cleared EP0STSTAL bit is set EP0STED bit is set EP0DED bit is cleared(Indicates End of control transfer)	0

26.3.4 USB Interrupt Register (USBINT)

Address : 0xA000_1810h

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 3			Reserved	
2	R/ Clear	Set	RSTINT: USB Reset Interrupt bit. USB set this bit when receives Reset signal.	0
1	R/ Clear	Set	RSUMINT: Resume Interrupt bit. In the suspend mode, USB set this bit when receives Resume signal. If the resume is caused by USB Reset, MCU interrupt is occurred by Resume interrupt. If clock continues to operate and duration of SE0 status is 3ms, then USB Reset interrupt is occurred.	0
0	R/ Clear	Set	SPDINT : Suspend Interrupt bit USB sets this bit when receive suspend signal. If there are no operations in bus during 3ms, this bit is set. Therefore, if the MCU does not stop Clock after the first suspend interrupt, the interrupt is occurred every 3ms. The default value of this interrupt is disable.	0

26.3.5 Endpoint Interrupt Enable Register (USBEPIEN)

Address : 0xA000_1814h

Bit	R/W	Description	Default Value
31 : 5	R	Reserved	
4	R/W	EP4INTEN : Endpoint 4 Interrupt enable bit	1
3	R/W	EP3INTEN : Endpoint 3 Interrupt enable bit	1
2	R/W	EP2INTEN : Endpoint 2 Interrupt enable bit	1
1	R/W	EP1INTEN : Endpoint 1 Interrupt enable bit	1
0	R/W	EP0INTEN : Endpoint 0 Interrupt enable bit	1

26.3.6 USB Interrupt Enable Register (USBINTEN)

Address : 0xA000_1818h

Bit	R/W	Description	Default Value
31 : 3	R	Reserved	
2	R/W	RSTINTEN : USB RESET Interrupt enable bit	1
1	R	Reserved	
0	R/W	SPDINTEN : SUSPEND Interrupt enable bit	0

26.3.7 USB Low Byte Frame Number Register (USBLBFN)

Address : 0xA000_181Ch

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R/W	Frame Number 1 register	0x00

26.3.8 USB High Byte Frame Number Register (USBHBFN)

Address : 0xA000_1820h

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R/W	Frame Number 2 register	0x00

26.3.9 USB Index Register (USBIND)

Address : 0xA000_1824h

Bit	R/W	Description	Default Value
31 : 3	R	Reserved	
2 : 0	R/W	Index register 000 : Endpoint 0 001 : Endpoint 1 010 : Endpoint 2 011 : Endpoint 3 100 : Endpoint 4 101 : Reserved 110 : Reserved 111 : Reserved	000

26.3.10 USB MAXP Register (USBMP)

Address : 0xA000_1828h

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R/W	Max FIFO Size 0000_0001 MAXP=8 0000_0010 MAXP=16 0000_0100 MAXP=32 0000_1000 MAXP=64	0x00

26.3.11 USB EP0 Control Register (USBEP0C)

Address : 0xA000_182Ch

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 8	R		Reserved	
7	Clear		EP0SUEC : EP0 Set Up End Clear bit. MCU write 1 to this bit in order to clear EP0STED bit.	0
6	Clear		EP0OPRC : EP0 Out Packet Ready Clear bit. MCU write 1 to this bit in order to clear EP0OPR bit.	0
5	Set	Clear	EP0SDSTAL: EP0 Send Stall bit. If the MCU recognizes the token is wrong, the MCU clears EP0OPR bit and sets this bit. USB generates STALL handshake to current control transfer. MCU write 0 in order to finish STALL.	0
4	R	Set	EP0STED: EP0 Setup End bit. Read Only bit. If control transfer is finished before set the EP0DED bit, USB set this bit. When USB sets this bit, MCU receives interrupt. In this case, USB flushed FIFO, and invalidates FIFO access from MCU. If the FIFO access is validated, this bit is cleared.	0
3	Set/R	Clear	EP0DED: EP0 Data End bit. MCU sets this bit at following conditions. - EP0OPR bit is cleared after takes the last data packet. - EP0OPR bit is cleared and EP0IPR is set in Zero length data phase. - MCU sets EP0IPR bit and this bit (EP0DED) after MCU loads packet data from FIFO.	0
2	Clear/R	Set	EP0STSTAL: Sent Stall bit. If control transaction is finished by protocol error, USB set this bit. If this bit is set, interrupt is occurred.	0
1	Set/R	Clear	EP0IPR: EP0 In Packet Ready bit. MCU set this bit after writes data into Endpoint0 FIFO. If the data packet is transferred to host successfully, USB clears this bit. If USB clears this bit, interrupt is occurred. Therefore, MCU can keep loading the next data. MCU set EP0IPR and EP0DED in Zero length data phase at the same time.	0
0	R	Set	EP0OPR: EP0 Out Packet Ready bit. Read only. if valid token is written in FIFO, USB set this bit. USB sets this bit, interrupt is occurred. By writing value 1 to EP0OPRC, MCU clears this bit.	0

26.3.12 USB IN Control 1 Register (USBIC1)

Address : 0xA000_182Ch

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 7	R		Reserved	
6	Set	R/Clear	ICCDT: In Control 1 Clear Data Toggle bit. Write Only. If MCU writes 1 to this bit, data toggle bit is cleared.	0
5	R/ Clear	Set	ICSTSTAL: In Control 1 Sent Stall bit. Because MCU sets ICSDSTAL bit, STALL handshake is occurred in the In token. At the time, USB sets this bit. If USB generates STALL handshake, ICIPR bit is cleared. By writing 0, this bit is cleared.	0
4	R/W	R	ICSDSTAL: In Control 1 Send Stall bit. In order to generate STALL handshake to USB, MCU writes 1 to this bit. To finish the STALL, MCU clears this bit.	0
3	R/Set	Clear	ICFFLU: In Control 1 FIFO Flush bit. In order to flush IN FIFO, MCU set this bit. If FIFO is flushed, this bit is cleared by USB. In this circumstance, interrupt is occurred. If a token is processing, USB waits for finish the data transfer. If two packets are loaded into FIFO, the first packet (that will be sent to host) is flushed and the corresponding ICIPR bit is cleared.	0
2			Reserved	0
1	R	Set	ICFNE: In Control 1 FIFO Not Empty bit. This bit represents that FIFO contains at most 1 data packet. 0: No packet inside FIFO. 1: The FIFO holds packets.	0
0	R/Set	Clear	ICIPR: In Control 1 In Packet Ready bit. After write data to FIFO, MCU set this bit. If data packet transfer is success, USB clears this bit. If USB clears this bit, interrupt is occurred, and MCU can load the next packet. During this bit is set, MCU cannot write FIFO. If MCU set ICSDSTAL, this bit cannot be set.	0

26.3.13 USB IN Control 2 Register (USBIC2)

Address : 0xA000_1830h

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 8	R		Reserved	
7	R/W	R	ICASET: In Control 2 Auto Set bit. If this bit is set, MCU set ICIPR bit automatically when MCU writes data as MAXP. In the case of write smaller size data than XAXP, MCU should set ICIPR bit.	0
6			Reserved	0
5	R/W	R	ICMODIN: In Control 2 Mode In bit. With this bit, the direction of Endpoint can be programmable. 1 = In Endpoint 0 = Out Endpoint	1
4 : 0			Reserved	

26.3.14 USB Out Control Register 1 (USBOC1)

Address : 0xA000_1838h

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 8	R		Reserved	
7	R/W	R	OCCDT: Out Control 1 Clear Data Toggle bit. If MCU write 1 to this bit, data toggle sequence bit is reset to DATA0.	0
6	Clear/R	Set	OCSTSTAL: Out Control 1 Sent Stall bit. When OUT token is finished by the STALL handshake, USB set this bit. If OUT Token sends larger size of data than MAXP, USB generates STALL handshake to host. If MCU writes 0, this bit is cleared.	0
5	W/R	R	OCSDSTAL: Out Control 1 Send Stall bit. MCU writes 1 to this bit in order to generate STALL handshake to USB. In order to finish the STALL status, MCU write 0 into this bit.	0
4	R/W	Clear	OCFFLU: Out Control 1 FIFO Flush bit. MCU writes 1 to this bit in order to flush FIFO and write 0 to stop. Only during OCOPR bit is set, this bit can be set. Data packet that is taken by MCU will be flushed.	0
3	R	R/W	OCERR : Out Control 1 Data Error bit This bit represents that there are errors (bit stuffing or CRC) in received data. This bit is cleared automatically when OCOPR bit is cleared.	0
2	R	R	Reserved	
1	R	R/W	OCFFUL: Out Control 1 FIFO Full bit. This bit represents that FIFO is Full. 0: FIFO is not full. 1: FIFO is full.	0
0	R/ Clear	Set	OCOPR: Out Control 1 Out Packet Ready bit. When data packet is loaded into FIFO, USB set this bit. After MCU reads entire packet, this bit should be cleared by MCU. MCU write 0 to this bit in order to clear.	0

26.3.15 USB OUT Control Register 2 (USBOC2)

Address : 0xA000_183Ch

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 8	R		Reserved	
7	R/W	R	OCACLR: Out Control 2 Auto Clear bit. If this bit is set, whenever MCU reads data from OUT FIFO, OCOPR bit is cleared automatically by USB core.	0
6 : 0			Reserved	0

26.3.16 USB Low Byte Out Write Count Register (USBLOWC)

Address : 0xA000_1840h

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R/W	(LBOWC) Low Byte OEP write count register	0x00

26.3.17 USB High Byte Out Write Count Register (USBHBOWC)

Address : 0xA000_1844h

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R/W	(HBOWC) High Byte OEP write count register	0x00

26.3.18 EP0 FIFO Data Register (USBEP0)

Address : 0xA000_1848h

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R/W	EP0 FIFO Data Register	0x00

26.3.19 EP1 FIFO Data Register (USBEP1)

Address : 0xA000_184Ch

Bit	R/W	Description	Default Value
31 : 0	R/W	EP1 FIFO Data Register	0x00

26.3.20 EP2 FIFO Data Register (USBEP2)

Address : 0xA000_1850h

Bit	R/W	Description	Default Value
31 : 0	R/W	EP2 FIFO Data Register	0x00

26.3.21 EP3 FIFO Data Register (USBEP3)

Address : 0xA000_1854h

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R/W	EP3 FIFO Data Register	0x00

26.3.22 EP4 FIFO Data Register (USBEP4)

Address : 0xA000_1858h

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R/W	EP4 FIFO Data Register	0x00

27 USB HOST CONTROLLER

USB 1.1 Host Controller of *adStar-L* supports OpenHCI(ver1.0a).

27.1 Features

- OpenHCI1.0 compatible
- USB 1.1 compatible

27.2 Operational Registers

Table 27-1 USB Host Register List

Address	*Registers*
A0000000	HcRevision
A0000004	HcControl
A0000008	HcCommandStatus
A000000C	HcInterruptStatus
A0000010	HcInterruptEnable
A0000014	HcInterruptDisable
A0000018	HcHCCA
A000001C	HcPeriodCurrentED
A0000020	HcControlHeadED
A0000024	HcControlCurrentED
A0000028	HcBulkHeadED
A000002C	HcBulkCurrentED
A0000030	HcDoneHead
A0000034	HcFmInterval
A0000038	HcFmRemaining
A000003C	HcFmNumber
A0000040	HcPeriodicStart
A0000044	HcLSThreshold
A0000048	HcRhDescriptorA
A000004C	HcRhDescriptorB
A0000050	HcRhStatus
A0000054	Reserved.
A0000058	HcRhPortStatus[1]

28 ELECTRICAL CHARACTERISTIC

28.1 DC Electrical Characteristic

The ESD of device meets HBM-2KV and MM-200V.
The following table summarizes the electrical design specifications of DC specifications:

Table 28-1 I/O DC Electrical Characteristic

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level output voltage	VOH	IOH = -2, -4, -8, -16, -24mA	2.4			V
Low level output voltage	VOL	IOL = 2, 4, 8, 16, 24mA			0.4	V
High level input voltage	VIH	LVTTL/CMOS interface	2.0		IOVDD+0.5	V
Low level Input voltage	VIL	LVTTL/CMOS interface			0.8	V
Switch threshold	Vth	CMOS interface	1.2	1.3	1.4	V
		Schmitt-falling-trigger	0.8	0.9	1.0	V
		Schmitt-rising-trigger	1.45	1.55	1.65	V
Hysteresis		Schmitt-trigger interface	0.55	0.65	0.7	V
Input pull-up resistance	RPU	VIN = 0	34	41	64	kΩ
Input pull-down resistance	RPD	VIN = VDDH	33	44	79	kΩ
Input current	II	Vdd = MAX, 0V £ Vin £ 3.6V	-10		10	µA
Input current with pull down		Vin = Vdd	40		160	µA
Input current with pull up		Vin = 0	-160		40	µA

28.2 Operating Conditions

The following table gives the recommended operating conditions for the integrated circuit (IC) chips using this library:

Table 28-2 I/O Recommended Operating Conditions

Operating Conditoins	Min	Typ	Max
Core DC Supply (CoreVDD)	1.62V	1.8V	1.98V
I/O DC Supply Voltage (IOVDD)	3.0V	3.3V	3.6V

28.3 LDO Electrical Specification

Table 28-3 LDO Electrical Specifications

VDD33=3.3V, COUT=1uF, TA=25˚C unless otherwise noted

Parameters	Symbol	Test Condition	Min	Typ	Max	Units
Quiescent Current	Iq	Iout = 0 PD = 0		35		uA
Shutdown Current	Isd	PD = VDD33			1	uA
Input Voltage	VDD33		1.8+Vdrp	-	3.6	V
Output Voltage	VDD18	Iout = 0	1.75		1.85	V
Band Gap Output	VBG			1.2		V
External Capacitor				4.7		uF
Line Regulation		Vcc=3.0~3.6V Iout=10mA		0.2		%
		Vcc=3.0~3.6V Iout=150mA		0.4		
Dropout Voltage	Vdrp	Iout=150mA		240		mV
Ripple Rejection	PSRR	Iout=10mA Without bypass Cap (1kHz)		38		db
		Iout=150mA Without bypass Cap (1kHz)		38		
		Iout=150mA With bypass Cap (1kHz)		-		
Output Current	Iout			150		mA
PD Logic input High	ViH		0.85			V
PD Logic input Low	ViL				0.45	V
VDD18 Temperature Coefficient	TC	-45~125˚C		40		ppm

28.4 POR Electrical Specification

Table 28-4 POR Specification (Unless otherwise specified, Topr=25˚C, VDD=1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VDD	Supply voltage		1.6	1.8	2	V
Is	Supply current	VDD=1.8V		3	5	uA
Vtd	Minimum power up trigger level		1			V
Vtdr	Maximum power drop trigger level				0.9	V
Tr	Rising time of VDD		10u		10m	s
Tf	Falling time of VDD to VTH-100Mv (0.9V)		5			us
Td	Reset delay time after VTH trigger	Tr=80us		20		us
VOH	POR output high voltage	No load		VDD		V
		Isource=30uA, VDD≥1V		0.8*VDD		V
		Isource=100uA, VDD≥1.8V		0.8*VDD		V
VOL	POR output low voltage	No load		GND		V

28.5 PLL Electrical Specification

Table 28-5 PLL DC Characteristics (Unless otherwise specified, Topr=25˚C, VDD=1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
AVDD	Supply Voltage		1.6	1.8	2	V
DVDD	Digital Supply Voltage		1.6	1.8	2	V
Is	Supply Current	normal		3		mA
VIH	Input High Voltage		DVDD-0.3			V
VIL	Input Low Voltage				DGND+0.3	V

Table 28-6 PLL Input Frequency (Unless otherwise specified, Topr=25˚C, VDD=1.8V)

Symbol	Parameter	Min	Typ	Max	Unit
Fin	Input Frequency	0.06		2.25	Mhz

28.6 ADC Electrical Specification

Table 28-7 ADC Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
AVDD	Analog Supply Voltage	3	3.3	3.6	V
DVDD	Digital Supply Voltage	1.62	1.8	1.98	V
IR	Input Voltage	0.3		VDDA-0.3	V

Table 28-8 ADC DC Characteristics (Unless otherwise specified, Topr=25˚C, VDD=1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIH	Input High Voltage		1.5			V
VIL	Input Low Voltage				0.8	V

28.7 RTC Operation Voltage

Symbol	Parameter	Min	Typ	Max	Unit
VBAT	Analog Supply Voltage	1.8		3.6	V

28.8 Power Consumption

Table 28-9 Power Consumption from different conditions

Condition	Freq.	Typ.
CPU running from flash LCD displaying and Sound playing from NAND Flash file system	101Mhz	512.7mW
	108Mhz	525.3mW
CPU running from flash	96Mhz	341mW

29 PACKAGE DIMENSION

Unit: mm

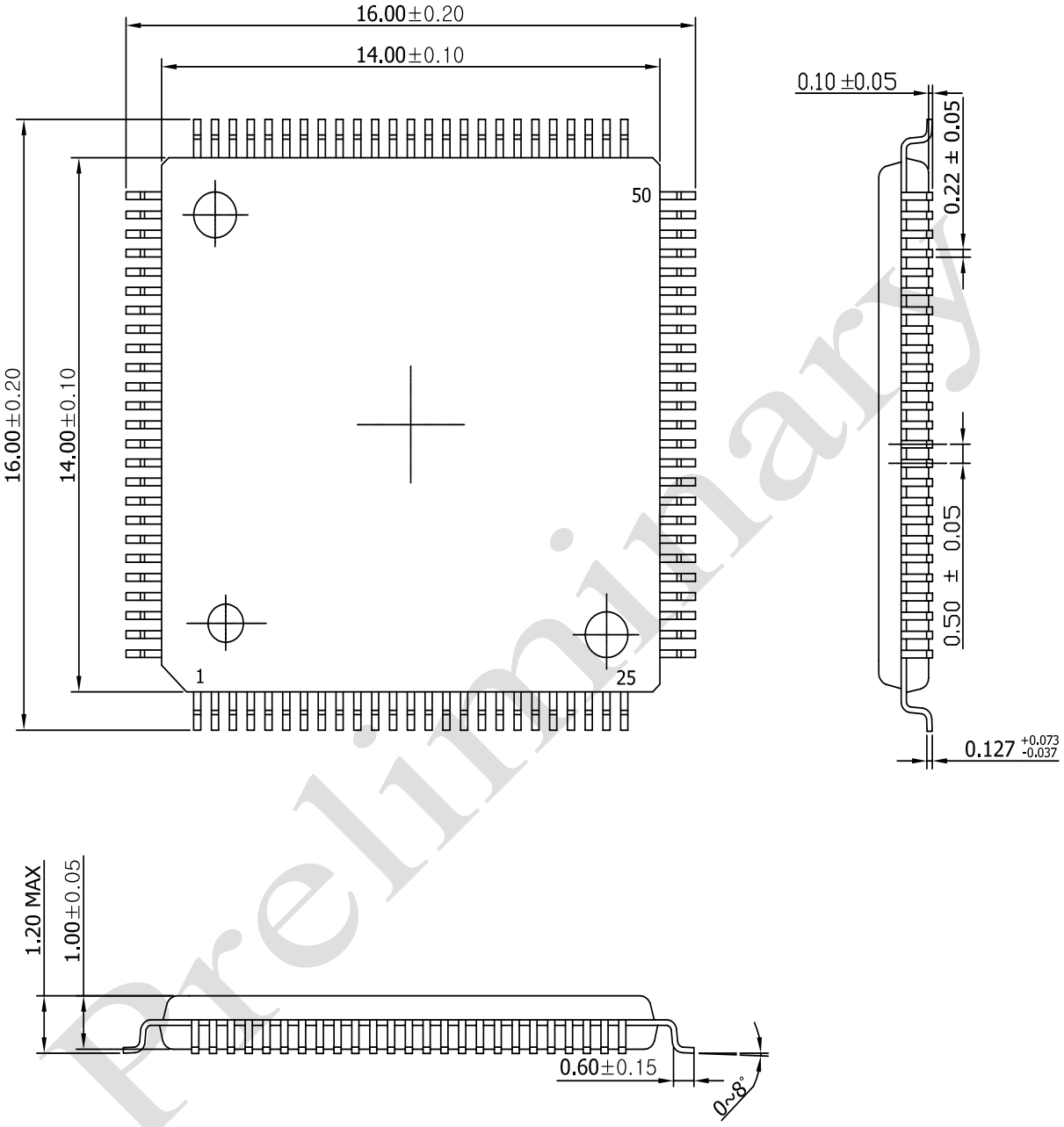


Figure 29-1 Package Dimension