advanced digital chips inc

Preliminary

adStar-D

adStar-D8M
adStar-D16M
adStar-D16MF512

Ver 0.7.1

September 19, 2023

Advanced Digital Chips, Inc.

History

Ver 0.0	
Jul. 21, 2011	1st version released
Ver 0.1	
Aug. 2, 2011	2nd version released
Ver 0.2	
Aug. 5, 2011	3rd version released
Ver 0.2.1	
Aug. 16, 2011	Figure 28-1 Package Dimension changed. Figure 2-3 added. Figure 2-2 modified
Ver 0.2.2	
Aug. 17, 2011	Pin layout Pin name fixed. Pin definition Pullup/Pulldown description modified
Ver 0.2.3	
Aug. 22, 2011	Features: Analog IPs modified. MCPWM/QEI added. Operating Temp. fixed. Block diagram SPM -> SRAM
Ver 0.2.4	
Aug. 29, 2011	Timer Wave Output Generation bit added.
Ver 0.2.5	
Sep. 15, 2011	Pin diagram fixed. (pin 120) Pin description fixed. (pin 33, 111, 128)
Ver 0.2.6	
Sep. 22, 2011	adStar general description updated.
Ver 0.2.7	
Oct. 2, 2011	Pinmux Description updated (ex. PA[0] -> P0.0)
Ver 0.2.8	
Oct. 4, 2011	Watch dog Register Address fixed. Timer description fixed (8ch->4ch) CRTC Register fixed
Ver 0.2.9	
Oct. 21, 2011	ADC Register's address fixed. Flash Mapping Address fixed. SPI Register address fixed. DMA Register address fixed. UART Irda Register added
Ver 0.3.0	
Oct. 25, 2011	Pinmux -> Port Alternative Functions (PAF)

Ver 0.3.2	
Nov. 2, 2011	ADC Sampling clock description
Ver 0.3.3	
Nov. 8, 2011	Wrong description fixed (Alternate function pins, USB PHY control register)
Ver 0.3.5	
Nov. 14, 2011	Wrong description fixed (Features, Dedicated PWM pin description, etc.)
Ver 0.3.6	
Nov. 15, 2011	Output Compare function removed
Ver 0.3.7	
Nov. 16, 2011	Miss typing corrected (Dedicated PWM)
Ver 0.3.8	
Nov. 18, 2011	Serial DBG description removed.
Ver 0.3.9	
Nov. 21, 2011	PLL Parameter Fin. added. I2S Clock control description added
Ver 0.4.0	
Nov. 29, 2011	CRT Controller Resolution fixed. External SRAM Register description fixed ADC Conversion cycle description added
Ver 0.4.1	
Nov. 30, 2011	Dedicated PWM function removed
Ver 0.4.2	
Dec. 9, 2011	GPIO Block diagram updated. GPIO Schmitt input enable register added Some CRTC registers added. Short name of some INTC registers changed
Ver 0.4.3	
Dec. 21, 2011	PWM function added
Ver 0.4.4	
Dec. 27, 2011	adStar Block diagram modified CRT -> LCD
Ver 0.4.5	
Jan. 3, 2012	TWI Master Receive mode flow chart fixed. Cache write-back removed
Ver 0.4.6	
Feb. 7, 2012	Internal SRAM description updated. LDO deleted.
Ver 0.4.7	
Feb. 13, 2012	Area information of analog IPs removed. Office information updated.

Ver 0.4.8	
Feb. 24, 2012	USB Host: TBD. LDO added. Block diagram updated.
Ver 0.4.9	
Feb. 27, 2012	USB Host: TBD -> *TBD, description added
Ver 0.5.0	
Mar. 2, 2012	Electrical Characteristic information of Analog IPs not needed removed
Ver 0.5.1	
Mar. 15, 2012	PMU Write Enable Register fixed. (Core Clock Off by Halt) PMU Clock Control Register fixed. (WIRQ mode/enable deleted) Flash Register added. (FLSTS2, FLCKDLY)
Ver 0.5.2	
Apr. 18, 2012	Power consumption added.
Ver 0.5.3	
Apr. 20, 2012	Untranslated description updated.
Ver 0.5.4	
May. 3, 2012	22.5.5 Mixer Out Register description fixed
Ver 0.5.5	
Sep. 21, 2012	PWM Override Control Register Description fixed.
Ver 0.5.6	
Nov. 16, 2012	Power On Start Time added.
Ver 0.5.7	
Dec. 17, 2012	Delete Special Event Register of PWM.
Ver 0.6.1 Dec 26,2013	Added the flip function in the LCD module Update Figure 12-2, 12-24 USB PHY D+/D- Pull-down enable bit added|
Ver 0.6.3 Nov. 11,2015	ADC characteritics added GP6.x SHMIT configuration is corrected
Ver 0.6.6 Jan. 18,2017	gpio register explanation modify
Ver 0.6.7 May 18,2017	Remove ADC trigger set Update LCD controller
Ver 0.6.8 May 26,2017	Remove bit 16 on MEMCON in SDRAM controller
Ver 0.6.8 Dec. 20,2017	Adress of UART IRDA Register corrected.
Ver 0.6.9 May. 14,2020	D8MF512 removed

Ver 0.7.0	
Nov. 11, 2022	IOH -2, -4, -16, -24mA removed IOL 2, 4, 16, 24mA removed PWM(Pulse Width Modulation) removed
Ver 0.7.1	
Sep. 09, 2023	LDO_VBG Pin added VDD18_OUT Pin added Operating Temperature changed (+80℃ -> +85℃)

adStar
Data Book

Office

22F, KeumkangPenterium IT Tower A dong, 810, Gwangyang-dong,
Dong-gu, Anyang-si, Gyeonggi-do, 431-060, Korea

Tel : +82-31-463-7500
Fax : +82-31-463-7588
URL : http://www.adc.co.kr

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1 DESCRIPTIONS AND FEATURES

1.1 General Description

adStar is a 32-bit micro-controller that has maximum 108HMz operation frequency. Especially, an embedded memory system of the *adStar* supports a flash memory as well as a SDRAM. Due to that reason, programmer can apply variable applications to the *adStar.*

PART NAME	FLASH	SDRAM
adStar-D8M	-	8MB
adStar-D16M	-	16MB
adStar-D16MF512	512KB	16MB

The *adStar* operates with off-chip or on-chip connected Quad Flash. The flash memory can be used as both a program memory and a data memory. The *adStar* can access the flash memory by configuring Quad-data bit for high speed. In addition, JTAG programming lets developers download a program with high speed.

A CPU of the *adStar* has separated bus architecture to access data and program memory (Harvard Architecture), and is implemented as 5-stage pipeline EISC architecture which provides fast instruction execution.

A LCD controller that is organized as additional hardware supports RGB888 and RGB565. In addition the LCD controller of the *adStar* provides maximum 800 x 600 resolution, Graphic Library, and JPEC Decoding Library. The *adStar* is the best solution for smart application with the resolution and supported libraries.

Additionally, MP3 Decoding Library and Sound Mixer can be used for voice, sound effects, and background sound. 4-channel 10-bit ADC (1MSPS) can convert analog data of sensor or external input into digital.

In particular, to enhance protection, the *adStar* provides Copy Protection by writing 24-bit key at the first time.

Also, the *adStar* can expand SRAM, Flash memory, and SD card manually. Especially, in the case of the NAND flash memory, by adapting SLC Type as well as 24-bit ECC, developers can reduce entire system design cost.

The *adStar* provides USB 2.0 Full-Speed Device/Host(*TBD), 5-channel UART, 2-channel SPI, 2-channel I2S, and TWI for communication. In the case of 8-channel DMA provides more fast communication than others. (*Notice. TBD means “To be determined”)

The *adStar* can be applied into Smart application of smart appliances, GUI (Graphical User Interface) of factory automation system with LCD, Access control system, Smart Greed, Sign pad, printer, POS, Barcode system, POP monitor, and etc.

Developers can download GCC based EISC compiler, software toolchain (assembler, linker, debugger), EISC Studio (IDE: Integrated Development Environment for EISC), Reference Circuit Schematics, software libraries, and example codes from ADChips

homepage (http://www.adchips.co.kr) without any restriction. In addition, developers can purchase development board (test board), and E-con (download/debugging tool) with reasonable price. As mass product tool, we provide two writing methods. One is 7-socket GANG-writer that can write to the chips before packing. The other is stand-alone type EISC HANDY that can write to the chip by using target board's power.

1.2 Features

▫ **High-performance, Low-power 32-bit EISC Microprocessor**

▫ **32-bit EISC Architecture**
- AE32000C-Lucida
- Harvard Architecture
- 5-Stage Pipelining
- 1 Cycle 32bit MAC
- Up to 108MIPS Throughput at 108MHz
- 8KB 2-way Instruction Cache
- 8KB 2-way Data Cache
- JTAG Debugger
  - Core Debugger
  - Bus Debugger

▫ **Embedded Memory**
- 2KBytes Internal SRAM for Instruction
- 30KBytes Internal SRAM for Data
- 8/16Mbytes SDRAM
- Optional 512KBytes Flash (More than 100,000 erase/program cycles)

▫ **External Memory Interface**
- 8 or 16-bit data, up to 18-bit addressing SRAM Interface
- 8-bit NAND Flash Interface supports SLC and MLC (4/24-bit ECC) type

▫ **Boot Mode**
- ROM Booting
- NAND Flash Booting
- Flash Booting

▫ **JTAG Interface**
- Boundary-scan capabilities
- Extensive On-chip Debug Support
- Programming of Fuses through the JTAG Interface

▫ **LCD Controller**
- RGB 888 or 565 output
- Supports up to 800 x 600 resolution display in RGB mode

▫ **USB 2.0 Full-Speed Device/Host(*TBD) Compatible**
- Supports Full-speed Data Rate 12Mbps

(*Notice. TBD means "To be determined")

▫ **Copy Protection**
- 24-bit key-protected only-one programmable bits

▫ **SD-Card Interface**
- Supports single/quad

▫ **Sound Mixer**
2ch. I2S, 2ch Digital Modulator

▫ **Other Peripherals**
32-bit Watchdog Timer
8-ch DMA
Interrupt Controller with 2 External IRQ
4 Channel 16-bit Timer/Counter with 15-bit Pre-scaler, Capture, PWM
5 Channel UART with 16Bytes FIFO, Functionally compatible with the 16550, with 1Channel IrDA
2 Channel Master/Slave SPI with 8Bytes FIFO
Two Wire Interface
Auto ECC NAND Flash Controller: 4-bit/24-bit ECC Support, Auto Booting with ECC Support
75-Port(adStar-16M) or 69-Port(adStar-16MF512) In/Out with open drain mode

▫ **Analog IPs**
10-bit 1MSPS SAR ADC with 4 analog input channels
POR (Power On Reset)
LDO
PLL x 2

▫ **Operating frequency**
Up to 108MHz

▫ **Power**
3.0V to 3.6V

▫ **Operating Temperature**
-40℃ / +85℃

▫ **Package**
128ETQFP (14 x 14)

2 BLOCK DIAGRAM & PIN DESCRIPTIONS

2.1 Block Diagram

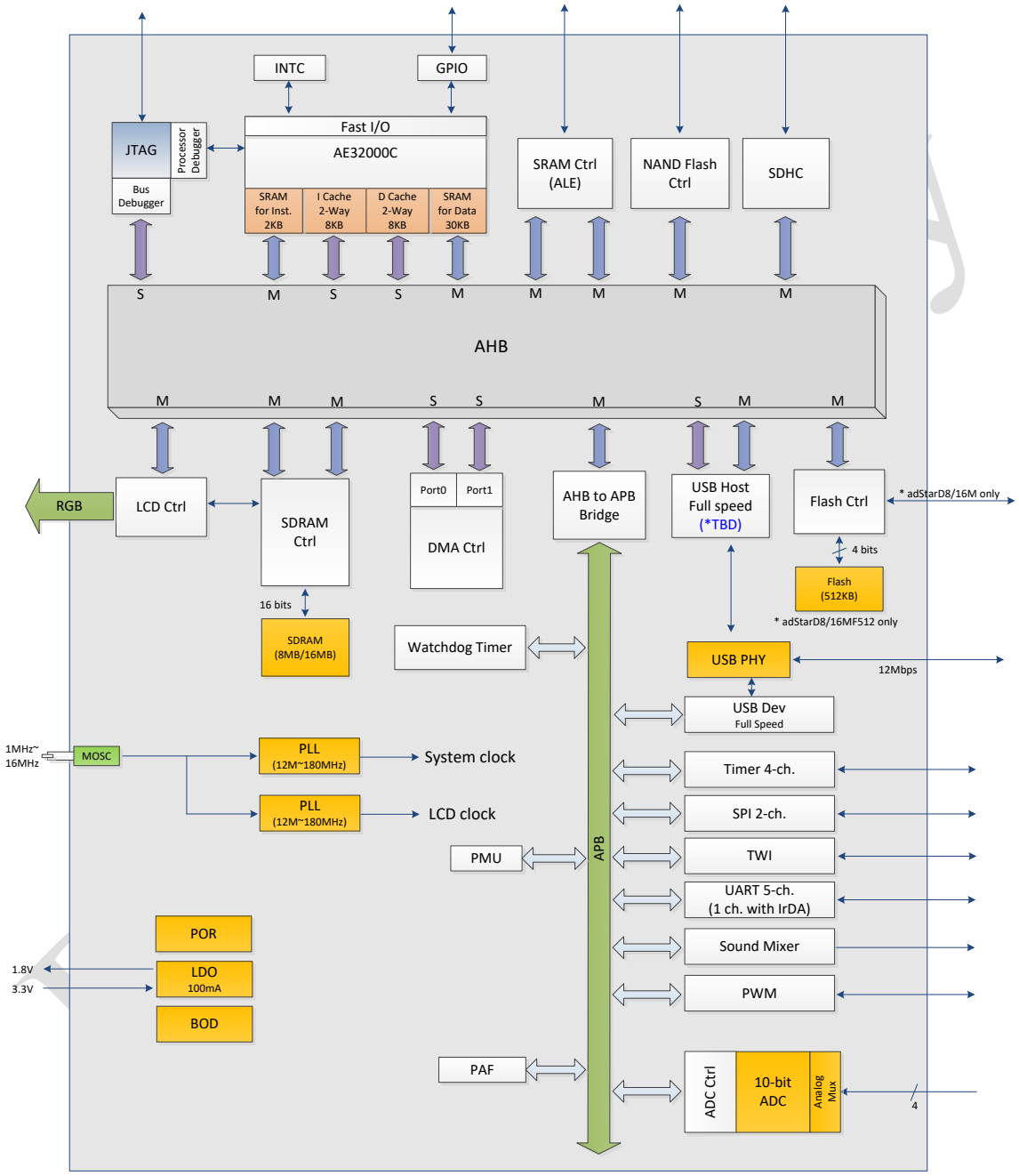


Figure 2-1 adStar Block Diagram

* Notice. TBD means “To be determined”

2.2 Pin Layout

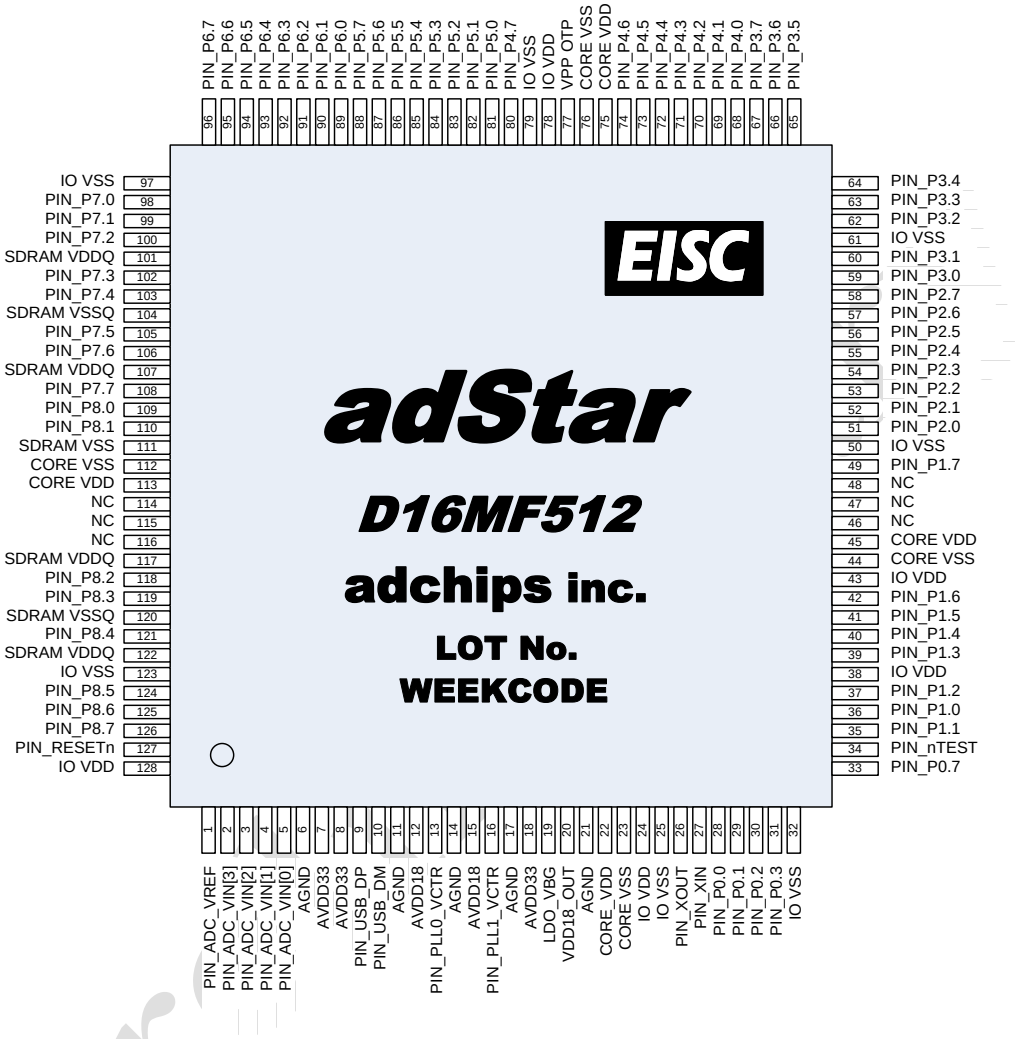


Figure 2-2 adStar 16MF512 Pin Layout

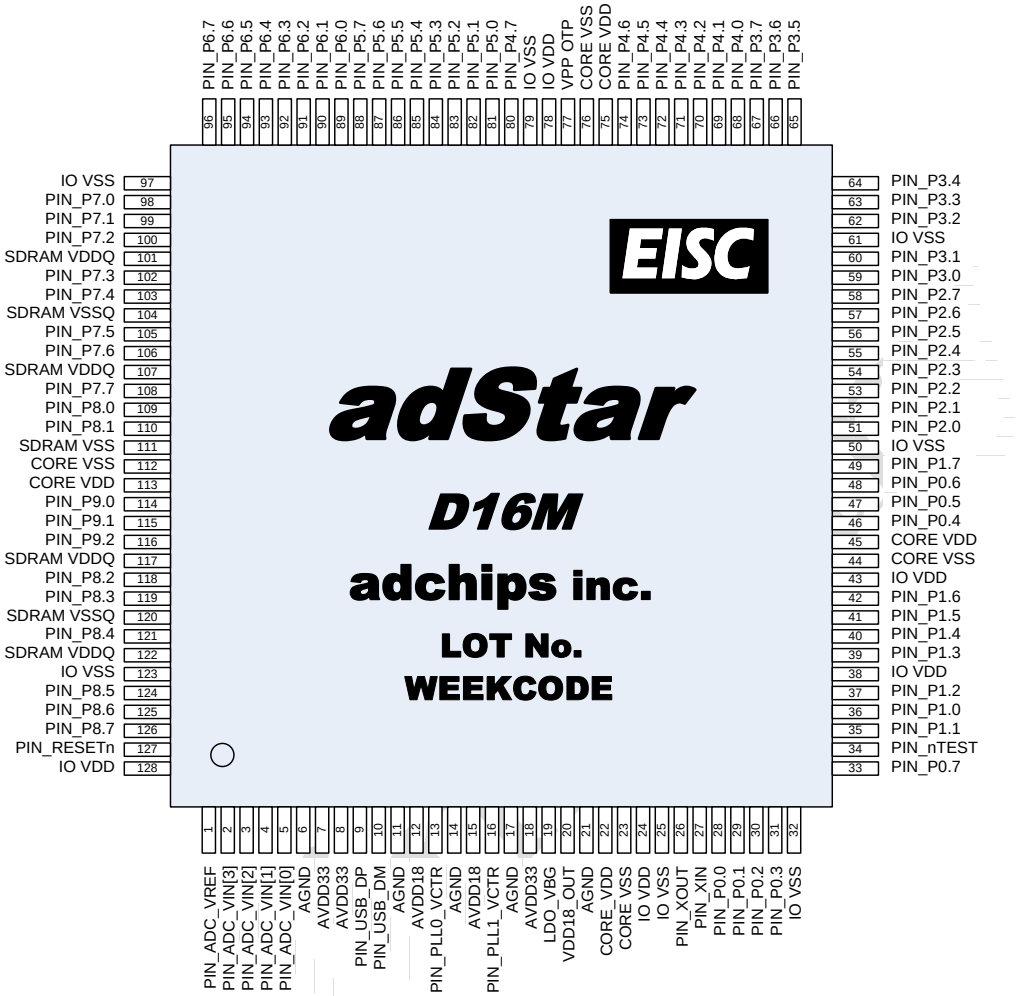


Figure 2-3 adStar D8/16M Pin Layout

2.3 Pin Definition

Table 2-1 adStar Pin Definitions 128-Pin

No.	Port Name	Description.	Type	Output Drive Current	Pull-Up / Pull-Down
1	PIN_ADC_VREF	ADC VREF - Reference Voltage Input Pin	In		
2	PIN_ADC_VIN[3]	ADC VIN 3 - Analog Voltage Input Channel 3	In		
3	PIN_ADC_VIN[2]	ADC VIN 2 - Analog Voltage Input Channel 2	In		
4	PIN_ADC_VIN[1]	ADC VIN 1 - Analog Voltage Input Channel 1	In		
5	PIN_ADC_VIN[0]	ADC VIN 0 - Analog Voltage Input Channel 0	In		
6	AGND	ADC GND - Ground	In		
7	AVDD33	ADC VDD - Positive Power Supply 3.3V	In		
8	AVDD33	USB PHY VDD - Power 3.3V	In		
9	PIN_USB_DP	USB DP - Data+ pin	I/O		
10	PIN_USB_DM	USB DM - Data- pin	I/O		
11	AGND	USB GND - Ground	In		
12	AVDD18	PLL0 VDD - Analog Power Supply 1.8V	In		
13	PIN_PLL0_VCTR	PLL0 VCTR - VCO Control Voltage, corresponding LPF should be connected here	In		
14	AGND	PLL0 GND - Ground	In		
15	AVDD18	PLL1 VDD - Analog Power Supply 1.8V	In		
16	PIN_PLL1_VCTR	PLL1 VCTR - VCO Control Voltage, corresponding LPF should be connected here	In		
17	AGND	PLL1 GND – Ground	In		
18	AVDD33	VDD - Power Supply 3.3V	In		
19	LDO_VBG	Band-Gap Reference for LDO	In		
20	VDD18_OUT	LDO 1.8V Output	Out		
21	AGND	GND - Ground	In		
22	CORE VDD	Core VDD - Power Supply 1.8V	In		
23	CORE VSS	Core GND - Ground	In		
24	IO VDD	IO VDD - Power Supply 3.3V	In		
25	IO VSS	IO GND - Ground	In		
26	PIN_XOUT	OSC XOUT - Oscillator XOUT	Out		
27	PIN_XIN	OSC XIN - Oscillator XIN	In		
28	PIN_P0.0	GPIO - General Purpose I/O P0.0 SPI0_CSn - SPI Channel 0 Chip Select TWI_SCL - TWI Serial Clock Output	I/O	8mA	Controllable (Up, Down or Disable)
29	PIN_P0.1	GPIO - General Purpose I/O P0.1 SPI0_MISO - SPI Channel 0 Master In Slave Out TWI_SDA - TWI Serial Data Input Output	I/O	8mA	Controllable (Up, Down or Disable)
30	PIN_P0.2	GPIO - General Purpose I/O 0.2 DM0_PWMR_P - Sound Channel2 Digital Modulator PWM Right Channel Positive Output SPI0_MOSI - SPI Channel 0 Master Out Slave In SRAM_CS1x - SRAM Bank 1 Chip Select	I/O	8mA	Controllable (Up, Down or Disable)
31	PIN_P0.3	GPIO - General Purpose I/O P0.3 DM0_PWMR_N - Sound CH2 Digital Modulator PWM Right Channel Negative Output SPI0_SCK - SPI Channel 0 SCK Clock SRAM_CS2x - SRAM Bank 2 Chip Select	I/O	8mA	Controllable (Up, Down or Disable)
32	IO VSS	IO GND - Ground	In		
33	PIN_P0.7	GPIO - General Purpose I/O P0.7 DM1_PWMR_N - Sound CH3 Digital Modulator PWM Right Channel Negative Output TAP_SEL - TAP Controller Select (BSC or DBG) UART_RX4 - UART Channel 4 RX (IrDA)	I/O	8mA	Controllable (Up, Down or Disable)
34	PIN_nTEST	nTEST - Test Mode Enable Pin	In		Up
35	PIN_P1.1	GPIO - General Purpose I/O 1.1 UART_RX0 - UART Channel 0 RX I2S0_SDI - Sound Channel 0 I2S Data Input TWI_SDA - TWI Serial Data Input Output	I/O	8mA	Controllable (Up, Down or Disable)
36	PIN_P1.0	GPIO - General Purpose I/O 1.0 UART_TX0 - UART Channel 0 TX I2S_MCLK - Sound I2S Master Clock TWI_SCL - TWI Serial Clock Output	I/O	8mA	Controllable (Up, Down or Disable)
37	PIN_P1.2	GPIO - General Purpose I/O 1.2 NF_CSx - NAND Flash Chip Select SRAM_CS1x - SRAM Bank 1 Chip Select	I/O	8mA	Controllable (Up, Down or Disable)
38	IO VDD	IO / SDRAM VDD - Power Supply 3.3V	In		

39	PIN_P1.3	GPIO - General Purpose I/O 1.3 NF_ALE - NAND Flash Address Latch Enable SDHC_CMD - SDHC Command SRAM_CS3x - SRAM Bank 3	I/O	8mA	Controllable (Up, Down or Disable)
40	PIN_P1.4	GPIO - General Purpose I/O 1.4 NF_CLE - NAND Flash Command Latch Enable SDHC_CLK - SDHC Clock SRAM_BE1x - SRAM Byte Enable [1]	I/O	8mA	Controllable (Up, Down or Disable)
41	PIN_P1.5	GPIO - General Purpose I/O 1.5 NF_WEx - NAND Flash Write Enable I2S0_SCLK - Sound Channel 0 I2S Bit Clock SRAM_A17 - SRAM Address [17]	I/O	8mA	Controllable (Up, Down or Disable)
42	PIN_P1.6	GPIO - General Purpose I/O 1.6 NF_REx - NAND Flash Read Enable I2S0_LRCLK - Sound Channel 0 I2S Sample Clock SRAM_A18 - SRAM Address [18]	I/O	8mA	Controllable (Up, Down or Disable)
43	IO VDD	IO VDD - Power Supply 3.3V	In		
44	CORE VSS	Core GND - Ground	In		
45	CORE VDD	Core VDD - Power Supply 1.8V	In		
46	NC (D16MF512)	Not Connected.			
	PIN_P0.4 (D16M or D8M)	GPIO - General Purpose I/O 0.4 DM1_PWML_P - Sound Channel 3 Digital Modulator PWM Left Channel Positive Output Flash_CSx - Flash Chip Select CAP_IN1 - Capture Channel 1 Input	I/O	8mA	Controllable (Up, Down or Disable)
47	NC (D16MF512)	Not Connected.			
	PIN_P0.5 (D16M or D8M)	GPIO - General Purpose I/O 0.5 DM1_PWML_N - Sound Channel 3 Digital Modulator PWM Left Channel Negative Output Flash_DQ1 - Flash Data[1] TM_OUT1 - PWM Channel 1 output	I/O	8mA	Controllable (Up, Down or Disable)
48	NC (D16MF512)	Not Connected.			
	PIN_P0.6 (D16M or D8M)	GPIO - General Purpose I/O 0.6 DM1_PWMR_P - Sound Channel 3 Digital Modulator PWM Right Channel Positive Output Flash_DQ2 - Flash Data[2] UART_TX4 - UART Channel 4 TX (IrDA)	I/O	8mA	Controllable (Up, Down or Disable)
49	PIN_P1.7	GPIO - General Purpose I/O 1.7 NF_BUSYx - NAND Flash Busyx I2S0_SDO - Sound Channel 0 I2S Data Output SRAM_WAITx - SRAM Wait Signal Input	I/O	8mA	Controllable (Up, Down or Disable)
50	IO VSS	IO GND	In		
51	PIN_P2.0	GPIO - General Purpose I/O 2.0 NF_D0 - NAND Flash Data[0] UART_TX3 - UART Channel 3 TX SRAM_A8/D8 - SRAM Address[8]/Data[8]	I/O	8mA	Controllable (Up, Down or Disable)
52	PIN_P2.1	GPIO - General Purpose I/O 2.1 NF_D1 - NAND Flash Data[1] UART_RX3 - UART Channel 3 RX SRAM_A9/D9 - SRAM Address[9]/Data[9]	I/O	8mA	Controllable (Up, Down or Disable)
53	PIN_P2.2	GPIO - General Purpose I/O 2.2 NF_D2 - NAND Flash Data[2] UART_TX4 - UART Channel 4 TX (IrDA) SRAM_A10/D10 - SRAM Address[10]/Data[10]	I/O	8mA	Controllable (Up, Down or Disable)
54	PIN_P2.3	GPIO - General Purpose I/O 2.3 NF_D3 - NAND Flash Data[3] UART_RX4 - UART Channel 4 RX (IrDA) SRAM_A11/D11 - SRAM Address[11]/Data[11]	I/O	8mA	Controllable (Up, Down or Disable)
55	PIN_P2.4	GPIO - General Purpose I/O 2.4 NF_D4 - NAND Flash Data[4] SDHC_D0 - SDHC Data[0] SRAM_A12/D12 - SRAM Address[12]/Data[12]	I/O	8mA	Controllable (Up, Down or Disable)
56	PIN_P2.5	GPIO - General Purpose I/O 2.5 NF_D5 - NAND Flash Data[5] SDHC_D1 - SDHC Data[1] SRAM_A13/D13 - SRAM Address[13]/Data[13]	I/O	8mA	Controllable (Up, Down or Disable)
57	PIN_P2.6	GPIO - General Purpose I/O 2.6 NF_D6 - NAND Flash Data[6] SDHC_D2 - SDHC Data[2]	I/O	8mA	Controllable (Up, Down or Disable)

		SRAM_A14/D14 - SRAM Address[14]/Data[14]			
58	PIN_P2.7	GPIO - General Purpose I/O 2.7 NF_D7 - NAND Flash Data[7] SDHC_D3 - SDHC Data[3] SRAM_A15/D15 - SRAM Address[15]/Data[15]	I/O	8mA	Controllable (Up, Down or Disable)
59	PIN_P3.0	GPIO - General Purpose I/O 3.0 SRAM_A0/A8/D0 - SRAM Address[0]/Address[8]/Data[0] CAP_IN0 - Capture Channel 0 Input	I/O	8mA	Controllable (Up, Down or Disable)
60	PIN_P3.1	GPIO - General Purpose I/O 3.1 SRAM_A1/A9/D1 - SRAM Address[1]/Address[9]/Data[1] TM_OUT0 - PWM Channel 0 Output	I/O	8mA	Controllable (Up, Down or Disable)
61	IO VSS	IO / SDRAM GND - Ground	In		
62	PIN_P3.2	GPIO - General Purpose I/O 3.2 SRAM_A2/A10/D2 - SRAM Address[2]/Address[10]/Data[2] UART_TX3 - UART Channel 3 TX	I/O	8mA	Controllable (Up, Down or Disable)
63	PIN_P3.3	GPIO - General Purpose I/O 3.3 SRAM_A3/A11/D3 - SRAM Address[3]/Address[11]/Data[3] UART_RX3 - UART Channel 3 RX	I/O	8mA	Controllable (Up, Down or Disable)
64	PIN_P3.4	GPIO - General Purpose I/O 3.4 SRAM_A4/A12/D4 - SRAM Address[4]/Address[12]/Data[4] CAP_IN2 - Capture Channel 2 Input	I/O	8mA	Controllable (Up, Down or Disable)
65	PIN_P3.5	GPIO - General Purpose I/O 3.5 SRAM_A5/A13/D5 - SRAM Address[5]/Address[13]/Data[5] TM_OUT2 - PWM Channel 2 Output	I/O	8mA	Controllable (Up, Down or Disable)
66	PIN_P3.6	GPIO - General Purpose I/O 3.6 SRAM_A6/A14/D6 - SRAM Address[6]/Address[14]/Data[6] OHCI_OVC - USB Host Over Current	I/O	8mA	Controllable (Up, Down or Disable)
67	PIN_P3.7	GPIO - General Purpose I/O 3.7 SRAM_A7/A15/D7 - SRAM Address[7]/Address[15]/Data[7] OHCI_PPW - USB Host Port Power	I/O	8mA	Controllable (Up, Down or Disable)
68	PIN_P4.0	GPIO - General Purpose I/O 4.0 SRAM_A16 - SRAM Address[16] EIRQ0 - External Interrupt Request 0	I/O	8mA	Controllable (Up, Down or Disable)
69	PIN_P4.1	GPIO - General Purpose I/O 4.1 SRAM_ALE0 - SRAM Address Latch Enable 0 EIRQ1 - External Interrupt Request 1	I/O	8mA	Controllable (Up, Down or Disable)
70	PIN_P4.2	GPIO - General Purpose I/O 4.2 SRAM_ALE1 - SRAM Address Latch Enable 0 UART_TX1 - UART Channel 1 TX	I/O	8mA	Controllable (Up, Down or Disable)
71	PIN_P4.3	GPIO - General Purpose I/O 4.3 SRAM_REx - SRAM Read Enable UART_RX1 - UART Channel 1 RX	I/O	8mA	Controllable (Up, Down or Disable)
72	PIN_P4.4	GPIO - General Purpose I/O 4.4 SRAM_WEx - SRAM Write Enable TWI_SCL - TWI Serial Clock UART_TX2 - UART Channel 2 TX	I/O	8mA	Controllable (Up, Down or Disable)
73	PIN_P4.5	GPIO - General Purpose I/O 4.5 SRAM_CS0x - SRAM Bank 0 Chip Select TWI_SDA - TWI Serial Data UART_RX2 - UART Channel 2 RX	I/O	8mA	Controllable (Up, Down or Disable)
74	PIN_P4.6	GPIO - General Purpose I/O 4.6 I2S_MCLK - Sound I2S Master Clock SPI_SCK1 - SPI Channel 1 SCK CAP_IN3 - Capture Channel 3 Input	I/O	8mA	Controllable (Up, Down or Disable)
75	CORE VDD	Core VDD - Power Supply 1.8V	In		
76	CORE VSS	Core GND - Ground	In		
77	VPP OTP	OTP VPP - Supply Voltage for Program 6.7V	In		
78	IO VDD	IO VDD - Power Supply 3.3V	In		
79	IO VSS	IO GND - Ground	In		
80	PIN_P4.7	GPIO - General Purpose I/O 4.7 I2S0_SDI - Sound Channel 0 I2S Data Input SPI_CS1x - SPI Channel 1 Chip Select TM_OUT3 - PWM Channel 3 Output	I/O	8mA	Controllable (Up, Down or Disable)
81	PIN_P5.0	GPIO - General Purpose I/O 5.0 I2S0_SCLK - Sound Channel 0 I2S Bit Clock SPI_MISO1 - SPI Channel 1 Master In Slave Out SRAM_A0 - SRAM Address[0]	I/O	8mA	Controllable (Up, Down or Disable)

82	PIN_P5.1	GPIO - General Purpose I/O 5.1 I2S0_LRCLK - Sound Channel 0 Sample Clock SPI_MOSI1 - SPI Channel 1 Master Out Slave In SRAM_A1 - SRAM Address[1]	I/O	8mA	Controllable (Up, Down or Disable)
83	PIN_P5.2	GPIO - General Purpose I/O 5.2 I2S0_SDO - Sound Channel 0 I2S Data Output UART_TX0 - UART Channel 0 TX SRAM_A2 - SRAM Address[2]	I/O	8mA	Controllable (Up, Down or Disable)
84	PIN_P5.3	GPIO - General Purpose I/O 5.3 LCDC_CLK_IN - LCDC Clock Input UART_RX0 - UART Channel 0 RX SRAM_A3 - SRAM Address[3]	I/O	8mA	Controllable (Up, Down or Disable)
85	PIN_P5.4	GPIO - General Purpose I/O 5.4 VSYNC - LCDC Vertical Sync. EIRQ0 - External Interrupt Request 0 SRAM_A4 - SRAM Address[3]	I/O	8mA	Controllable (Up, Down or Disable)
86	PIN_P5.5	GPIO - General Purpose I/O 5.5 HSYNC - LCDC Horizontal Sync. EIRQ1 - External Interrupt Request 1 SRAM_A5 - SRAM Address[5]	I/O	8mA	Controllable (Up, Down or Disable)
87	PIN_P5.6	GPIO - General Purpose I/O 5.6 DISP_EN - LCDC Display Enable UART_TX1 - UART Channel 1 TX SRAM_A6 - SRAM Address[6]	I/O	8mA	Controllable (Up, Down or Disable)
88	PIN_P5.7	GPIO - General Purpose I/O 5.7 LCDC_CLK_OUT - LCDC Clock Output UART_RX1 - UART Channel 1 RX SRAM_A7 - SRAM Address[7]	I/O	8mA	Controllable (Up, Down or Disable)
89	PIN_P6.0	GPIO - General Purpose I/O 6.0 R0 - LCDC Red 0 Output nTRST - JTAG nTRST	I/O	8mA	Controllable (Up, Down or Disable)
90	PIN_P6.1	GPIO - General Purpose I/O 6.1 R1 - LCDC Red 1 Output TCK - JTAG TCK	I/O	8mA	Controllable (Up, Down or Disable)
91	PIN_P6.2	GPIO - General Purpose I/O 6.2 R2 - LCDC Red 2 Output TDI - JTAG TDI	I/O	8mA	Controllable (Up, Down or Disable)
92	PIN_P6.3	GPIO - General Purpose I/O 6.3 R3 - LCDC Red 3 Output SDHC_CMD - SDHC Command I2S1_SCLK - Sound Channel 1 I2S Bit Clock	I/O	8mA	Controllable (Up, Down or Disable)
93	PIN_P6.4	GPIO - General Purpose I/O 6.4 R4 - LCDC Red 4 Output SDHC_D0 - SDHC Data[0] I2S1_LRCLK - Sound Channel 1 I2S Sample Clock	I/O	8mA	Controllable (Up, Down or Disable)
94	PIN_P6.5	GPIO - General Purpose I/O 6.5 R5 - LCDC Red 5 Output SDHC_D1 - SDHC Data[1] I2S1_SDO - Sound Channel 1 I2S Data Output	I/O	8mA	Controllable (Up, Down or Disable)
95	PIN_P6.6	GPIO - General Purpose I/O 6.6 R6 - LCDC Red 6 Output SDHC_D2 - SDHC Data[2] UART_TX2 - UART Channel 2 TX	I/O	8mA	Controllable (Up, Down or Disable)
96	PIN_P6.7	GPIO - General Purpose I/O 6.7 R7 - LCDC Red 7 Output SDHC_D3 - SDHC Data[3] UART_RX2 - UART Channel 2 RX	I/O	8mA	Controllable (Up, Down or Disable)
97	IO VSS	IO / SDRAM VSS - Ground	I/O		
98	PIN_P7.0	GPIO - General Purpose I/O 7.0 G0 - LCDC Green 0 Output TMS - JTAG TMS SRAM_CS1x - SRAM Bank 1 Chip Select	I/O	8mA	Controllable (Up, Down or Disable)
99	PIN_P7.1	GPIO - General Purpose I/O 7.1 G1 - LCDC Green 1 Output TDO - JTAG TDO SRAM_CS2x - SRAM Bank 2 Chip Select	I/O	8mA	Controllable (Up, Down or Disable)
100	PIN_P7.2	GPIO - General Purpose I/O 7.2 G2 - LCDC Green 2 Output SDHC_CLK - SDHC Clock SRAM_A10 - SRAM Address[10]	I/O	8mA	Controllable (Up, Down or Disable)
101	SDRAM VDDQ	SDRAM VDD - Power Supply 3.3V	In		
102	PIN_P7.3	GPIO - General Purpose I/O 7.3 G3 - LCDC Green 3 Output	I/O	8mA	Controllable (Up, Down

		CFG[0] - Power Configuration[0] SRAM_A11 - SRAM Address[11]			or Disable)
103	PIN_P7.4	GPIO - General Purpose I/O 7.4 G4 - LCDC Green 4 Output CFG[1] - Power Configuration[1] SRAM_A12 - SRAM Address[12]	I/O	8mA	Controllable (Up, Down or Disable)
104	SDRAM VSSQ	SDRAM VSS - Ground	In		
105	PIN_P7.5	GPIO - General Purpose I/O 7.5 G5 - LCDC Green 5 Output CFG[2] - Power Configuration[2] SRAM_A13 - SRAM Address[13]	I/O	8mA	Controllable (Up, Down or Disable)
106	PIN_P7.6	GPIO - General Purpose I/O 7.6 G6 - LCDC Green 6 Output CFG[3] - Power Configuration[3] SRAM_A14 - SRAM Address[14]	I/O	8mA	Controllable (Up, Down or Disable)
107	SDRAM VDDQ	SDRAM VDD - Power Supply 3.3.V	In		
108	PIN_P7.7	GPIO - General Purpose I/O 7.7 G7 - LCDC Green 7 Output CFG[4] - Power Configuration[4] (Not used, Pull-up Only) SRAM_A15 - SRAM Address[15]	I/O	8mA	Controllable (Up, Down or Disable)
109	PIN_P8.0	GPIO - General Purpose I/O 8.0 B0 - LCDC Blue 0 Output DM0_PWML_P - Sound Channel 2 Digital Modulator PWM Left Channel Positive Output SRAM_A8 - SRAM Address[8]	I/O	8mA	Controllable (Up, Down or Disable)
110	PIN_P8.1	GPIO - General Purpose I/O 8.1 B1 - LCDC Blue 1 Output DM0_PWML_N - Sound Channel 2 Digital Modulator PWM Left Channel Negative Output SRAM_A9 - SRAM Address[9]	I/O	8mA	Controllable (Up, Down or Disable)
111	SDRAM VSS	SDRAM VSS - Ground	In		
112	CORE VSS	Core GND - Ground	In		
113	CORE VDD	Core VDD - Power Supply 1.8V	In		
114	NC (D16MF512)	Not Connected.			
	PIN_P9.0 (D16M or D8M)	GPIO - General Purpose I/O 9.0 I2S1_SCLK - Sound Channel 1 I2S Bit Clock Flash_DQ0 - Flash Data[0] CAP_IN0 - Capture Channel 0 Input	I/O	8mA	Controllable (Up, Down or Disable)
115	NC (D16MF512)	Not Connected.			
	PIN_P9.1 (D16M or D8M)	GPIO - General Purpose I/O 9.1 I2S1_LRCLK - Sound Channel 1 I2S Sample Clock Flash_CLK - Flash Clock TM_OUT0 - PWM Channel 0 Output	I/O	8mA	Controllable (Up, Down or Disable)
116	NC (D16MF512)	Not Connected.			
	PIN_P9.2 (D16M or D8M)	GPIO - General Purpose I/O 9.2 I2S1_SDO - Sound Channel 1 I2S Data Output Flash_DQ3 - Flash Data[3] SRAM_CS3x - SRAM Bank 3 Chips Select	I/O	8mA	Controllable (Up, Down or Disable)
117	SDRAM VDDQ	SDRAM VDD - Power Supply 3.3V	In		
118	PIN_P8.2	GPIO - General Purpose I/O 8.2 B2 - LCDC Blue 2 Output DM0_PWMR_P - Sound Channel 2 Digital Modulator PWM Right Channel Positive Output CAP_IN1 - Capture Channel 1 Input	I/O	8mA	Controllable (Up, Down or Disable)
119	PIN_P8.3	GPIO - General Purpose I/O 8.3 B3 - LCDC Blue 3 Output DM0_PWMR_N - Sound Channel 2 Digital Modulator PWM Right Channel Negative Output TM_OUT1 - PWM Channel 1 Output	I/O	8mA	Controllable (Up, Down or Disable)
120	SDRAM VSSQ	SDRAM VSS - Ground	In		
121	PIN_P8.4	GPIO - General Purpose I/O 8.4 B4 - LCDC Blue 4 Output DM1_PWML_P - Sound Channel 3 Digital Modulator PWM Left Channel Positive Output CAP_IN2 - Capture Channel 2 Input	I/O	8mA	Controllable (Up, Down or Disable)
122	SDRAM VDDQ	SDRAM VDD - Power Supply 3.3V	In		
123	IO VSS	IO / SDRAM VSS - Ground	In		
124	PIN_P8.5	GPIO - General Purpose I/O 8.5 B5 - LCDC Blue 5 Output	I/O	8mA	Controllable (Up, Down

		DM1_PWML_N - Sound Channel 3 Digital Modulator PWM Left Channel Negative Output TM_OUT2 - PWM Channel 2 Output			or Disable)
125	PIN_P8.6	GPIO - General Purpose I/O 8.6 B6 - LCDC Blue 6 Output DM1_PWMR_P - Sound Channel 3 Digital Modulator PWM Right Channel Positive Output CAP_IN3 - Capture Channel 3 Input	I/O	8mA	Controllable (Up, Down or Disable)
126	PIN_P8.7	GPIO - General Purpose I/O 8.7 B7 - LCDC Blue 7 Output DM1_PWMR_N - Sound Channel 3 Digital Modulator PWM Right Channel Negative Output TM_OUT3 - PWM Channel 3 Output	I/O	8mA	Controllable (Up, Down or Disable)
127	PIN_nRESET	Reset - adStar Reset pin	In		Up
128	IO VDD	IO / SDRAM VDD - Power Supply 3.3V	In		

2.4 Pin Description

AVDD33, IO VDD, SDRAM VDD, SDRAM VDDQ : 3.3V Supply voltage
AVDD18, Core VDD : 1.8V Supply voltage
AGND, IO VSS, Core VSS, SDRAM VSSQ : Ground

VDD18_OUT : LDO 1.8V Output
LDO_VBG : Band-Gap Reference for LDO

VPP OTP : 6.5V Supply voltage for OTP Program

PIN_nTEST : Chip Test pin (Low active)
For testing the Chip. If the value of this pin is 0, then PIN_P6.0~2 and PIN_P7.0~1 are set to JTAG Interface PIN and PIN_P0.7 is set to TAP_SEL pin with regardless of PAF configuration.

TAP_SEL : TAP Controller Select
This pin selects JTAG Debugger TAP Controller or Boundary Scan TAP Controller of which inside the chip. If the value of the pin is set to 1, then JTAG Debugger TAP Controller is selected, otherwise, Boundary Scan TAP Controller is selected, i.e. the value is set to 0.

CFG[4:0] : Booting Mode Select (Please refer to 3.4 Boot Mode)
With this pin, developer selects Flash Booting, NOR Flash/ROM Booting, and NAND Flash Booting, etc.

PIN_ADC_VREF : reference voltage input pin that compares with VIN.
PIN_ADC_VIN[3:0] : Analog voltage level input channel which will be converted to digital value.

USB Pins: USB Shares USB Device and Host. (Refer to 4.3.7 USB PHY Control Register)
PIN_USB_DP : USB Data+ I/O
PIN_USB_DM : USB Data- I/O

GPIO : General Purpose I/O (Refer to 7 GPIO)

EIRQ0, EIRQ1 : External Interrupt Request Input Pins (Refer to 8 Interrupt Controller) supporting external interrupt.

Flash (Refer to 10 Flash Memory Controller)
Flash_CSx : Flash Chip Select
Flash_CLK : Flash Clock
Flash_D[3:0] : Flash Data I/O. This pin is for writing Command and Address into Flash memory. Also, Write/Read data.

External SRAM : Supports 4-bank External SRAM. (Refer to 12 External SRAM Controller)
Bank0 is used for booting and the data width should be 8-bit only.
SRAM_CS0x : Chip Select pin that selects ROM or NOR Flash that can be used for booting.
SRAM_CS1x, SRAM_CS2x, SRAM_CS3x : SRAM Chips Select
SRAM_A[7:0]/A[15:8]/D[7:0] : With following configurations, the SRAM Controller

configuration is 8-bit bus width and ALE Enable, if SRAM_ALE[1] is set to 1, then address[15:8] will be output, and if SRAM_ALE[0] is set to 1, address[7:0] will be output. And data [7:0] is output in other region. (Refer to Figure 12-1) With the same configurations except bus width that is 16-bit size long, the address [15:8] output will be removed. (Refer to Figure 12-3)
SRAM_A[15:8]/D[15:8] : With following configurations, the SRAM Controller configuration is 16-bit bus width and ALE Enable, if SRAM_ALE[1] is set to 1, then address[15:8] will be output, and data[15:8] is output in other region. (Refer to Figure 12-3)
SRAM_A[18:16] : SRAM Address[18:16] output.
SRAM_ALE[1:0] : If SRAM Address Latch is set to Enable and ALE is also set to Enable, then SRAM Data pin generates address output. If ALE[1] is set to 1, the output is Address[15:8] and if ALE[0] is set to 1, the output is Address[7:0].
SRAM_BE1x : SRAM Byte Enable[1]. Enable signal to access upper 8-bit data when the data length is 16-bit width.
SRAM_WEx : SRAM Write Enable.
SRAM_REx : SRAM Read Enable.
SRAM_WAITx : SRAM Wait signal. It is set to disable as Default. In case of SRAM supports the signal, developer can use.

NAND Flash (Refer to 13 NAND Flash Controller)
NF_CSx: NAND Flash Chips Select. Activates the NAND Flash.
NF_ALE: NAND Flash Address Latch Enable. Sends an address to the NAND Flash.
NF_CLE: NAND Flash Command Latch Enable. Sends a command to the NAND Flash.
NF_WEx: NAND Flash Write Enable. Stores data into NAND Flash.
NF_REx: NAND Flash Read Enable. Reads data from NAND Flash.
NF_BUSYx: NAND Flash Busy signal input pin. If the state of NAND Flash is Busy, the value of the pin is 0.
NF_D[7:0]: NAND Flash 8-bit Data I/O.

SDHC (Refer to 14 SD Host Controller)
SDHC_CLK : SDHC Clock
SDHC_CMD : SDHC Command
SDHC_D[3:0] : SDHC Data I/O

LCDC : RGB 888 output. Provides 1024x768 resolution (Refer to 16 LCD Controller)
LCDC_CLK_IN : Clock Input for LCD
VSYNC : Signal for vertically synchronization.
HSYNC : for horizontally synchronization.
DISP_EN : for horizontally synchronization.
LCDC_CLK_OUT : LCDC Clock Output
R[7:0] : Red Output 8-bit
G[7:0] : Green Output 8-bit
B[7:0] : Blue Output 8-bit

PWM/Capture : 4 channels. (Refer to 17 Timer)
TM_OUT0, TM_OUT1, TM_OUT2, TM_OUT3 : PWM Output.
CAP_IN0, CAP_IN1, CAP_IN2, CAP_IN3
: Capture Input. Input pin to measure period and pulse width of external signal.

SPI : 2 channels. (Refer to 18 SPI)
SPI0_CSn, SPI1_CSn : SPI Chip select signal
SPI0_SCK, SPI1_SCK : SPI Clock pin

SPI0_MISO, SPI1_MISO : When SPI is configured to Master, It used for Data input, otherwise, Data output.
SPI0_MOSI, SPI1_MOSI : When SPI is configured to Master, It used for Data output, otherwise, Data input.

TWI (Refer to 19 TWI)
TWI_SCL : TWI Serial Clock
TWI_SDA : TWI Serial Data

UART : 5 channels. (Refer to 20 UART)
Channel 0~3 are for UART only. Channel 4 supports IrDA.
UART_RX0, UART_RX1, UART_RX2, UART_RX3 : UART RX
UART_TX0, UART_TX1, UART_TX2, UART_TX3 : UART TX
UART_RX4 : UART RX with IrDA supported
UART_TX4 : UART TX with IrDA supported

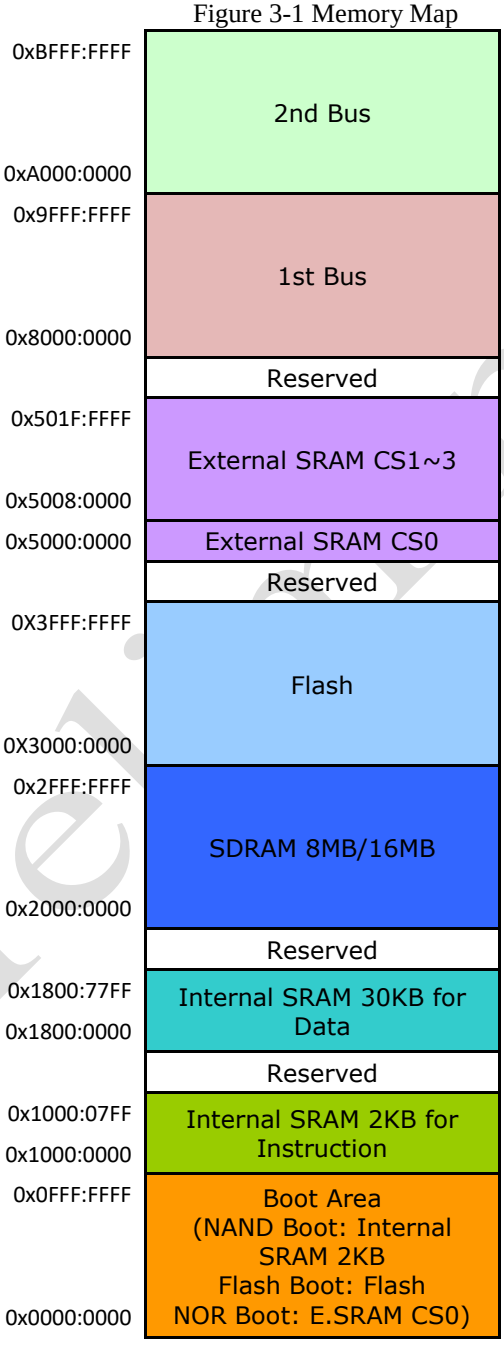
Sound Mixer : I2S 2 channels, Digital Modulator 2 channels. (Refer to 22 Sound Mixer)
I2S_MCLK : I2S Master Clock
I2S0_SDI : I2S Data input pin. It is used when external data is used as an input. Channel 0 only.
I2S0_SCLK, I2S1_SCLK : I2S Bit Clock
I2S0_LRCLK, I2S1_LRCLK : I2S Sample Clock. Separate between Left data and Right data.
I2S0_SDO, I2S1_SDO : I2S Data output pin
DM0_PWML_P, DM0_PWML_N, DM0_PWMR_P, DM0_PWMR_N,
DM1_PWML_P, DM1_PWML_N, DM1_PWMR_P, DM1_PWMR_N
: Sound Mixer Digital Modulator PWM output
Assigned to channel 2,3 of Sound Mixer. Each channel has Left and Right outputs and the outputs are divided into Positive and Negative outputs. As a result, one channel has total 4 output signals.

3 MEMORY ARCHITECTURE AND BOOTING MODE

3.1 Memory Map

The memory map is designed as following figure 3-1.

Figure 3-1 Memory Map



3.2 Embedded Memories

2KB Internal SRAM for Instruction
30KB Internal SRAM for Data

3.2.1 Internal SRAM for Instruction

adStar contains 2KB SRAM memory for instruction. The SRAM memory can be used for store instruction or data, and mainly it is used as instruction memory. In the case of read an instruction, the SRRAM memory access latency is 1-cycle and data read latency is 3-cycle.

3.2.2 Internal SRAM for Data

adStar contains 30KB SRAM memory for data. The data SRAM memory is used for store data, and it's access latency is 1-cycle.

3.2.3 Internal SRAM Registers

Internal SRAM Global Control Register
Address : 0x700 - Global Control Register

Bit	*R/W*	*Description*	*Default*
31 : 28	R	Exception Status 4'b0001 : DATA Access Violation 4'b0010 : Instruction Access Violation	0h
27 : 24	R	Reserved	0h
23 : 20	R	iBank Size: Physical memory size of each bank of internal SRAM for instruction 4'h0 : 1 KB 4'h1 : 2 KB 4'h2 : 4 KB 4'h3 : 8 KB 4'h4 : 16 KB 4'h5 : 32 KB 4'h6 : 64 KB 4'h7 : 128 KB	
19 : 16	R/W	iSRAM Configuration 4'h0 : user is recognized as one chunk of memory 4'h1 : Reserved 4'h2 : user is recognized as four memory chunks	0h

15 : 12	R	iSRAM Enable 4'b0001 : SRAM Enable 4'b0000 : SRAM Disable	0h
11 : 8	R	dBank Size: Physical memory size of each bank of internal SRAM for data 4'h0 : 1 KB 4'h1 : 2 KB 4'h2 : 4 KB 4'h3 : 8 KB 4'h4 : 16 KB 4'h5 : 32 KB 4'h6 : 64 KB 4'h7 : 128 KB	
7 : 4	R/W	dSRAM Configuration 4'h0 : user is recognized as one chunk of memory 4'h1 : Reserved 4'h2 : user is recognized as four memory chunks	0h
3 : 0	R	dSRAM Enable 4'b0001 : SRAM Enable 4'b0000 : SRAM Disable	0h

Internal SRAM Local Control Register

Address : 0x701, 0x711, 0x721, 0x731 – Local iSRAM Control Register

Address : 0x704, 0x714, 0x724, 0x734 – Local dSRAM Control Register

Bit	*R/W*	*Description*	*Default*
31 : 12	R	Reserved	0h
11 : 8	R	External Access: BUS Access Permission 4'h0 : External Access Not Support 4'h1 : External Access Support	
7 : 4	R/W	Privilege Mode: User Permission 4'h0 : Supervisor only Access 4'h1 : Supervisor/User Access	0h
3 : 0	R	Enable 4'b0001 : Local SRAM Enable 4'b0000 : Local SRAM Disable	0h

Internal SRAM Local Start Address Register

Address : 0x702, 0x712, 0x722, 0x732 – Local iSRAM Start Register

Address : 0x705, 0x715, 0x725, 0x735 – Local dSRAM Start Register

Bit	R/W	Description	Default
31 : 0	R/W	SRAM Start Address	0h

Internal SRAM Local End Address Register
ADDRESS : 0x703, 0x713, 0x723, 0x733 – Local iSRAM End Register
ADDRESS : 0x706, 0x716, 0x726, 0x736 – Local dSRAM End Register

Bit	R/W	Description	Default
31 : 0	R/W	SRAM End Address	0h

3.2.4 Internal SRAM Register Setting

Example.

```
//#########################################################
//## Internal SRAM Global Register Setting
//#########################################################
asm(“ ldi 0x700,          %r0”);
asm(“ mvtc 0x0,           %r3”);
asm(“ ldi 0x00021021,     %r0”); //#ON //#Num of Memory Bank: 4
asm(“ mvtc 0x0,           %r4”);
```

3.3 Memory Mapped I/O

The register space is from 8000_0000h, and the size of each functional block is 1Kbyte. Memory mapped I/O is represented as following Table 3-1.

Table 3-1 Memory Mapped I/O Register

Offset Address	Block	BUS	Remark
0x8000_0000	Flash Controller	1st AHB	
0x8000_0400	SDRAM Controller		
0x8000_0800	External SRAM Controller		
0x8000_0C00	Reserved		
0x8000_1000	Reserved		
0x8000_1400	DMA Controller		
0x8002_0000	Watchdog Timer	1st APB	
0x8002_0400	Timer		4 Channels
0x8002_0800	UART (5th ch. IrDA)		5 Channels
0x8002_0C00 ~0x8002_17FF	Reserved		
0x8002_1800	TWI		
0x8002_1C00 ~0x8002_23FF	Reserved		
0x8002_2400	LCDC		
0x8002_2800 ~0x8002_33FF	Reserved		
0x8002_3400	Port Alternate Functions		
0x8002_3800	OTP Controller		
0x8002_3C00	PMU		
0x8003_0000 ~0x8003_FFFF	Reserved		
Offset Address	**Block**	**BUS**	**Remark**
0xA000_0000	USB Host **(*TBD)**	2st	

0xA000_0400 ~0xA000_0BFF	Reserved	AHB	
0xA000_0C00	NAND Flash Controller		
0xA000_1000	SDHC		
0xA000_1400	Reserved		
0xA000_1800	USB Device		
0xA002_1000	SPI 0	2st APB	
0xA002_1400	SPI 1		
0xA002_1800	Reserved		
0xA002_1C00	Sound Mixer		
0xA002_2000 ~0xA002_37FF	Reserved		
0xA002_3800	ADC Controller		10-bit ADC
0xA002_3C00	Reserved		
0xA003_0000 ~0xA003_FFFF	Reserved		

*Notice. TBD means “To be determined”

3.4 Boot Mode

3.4.1 Debugger Boot Mode

If CFG[0]=0, then *adstar* boots as Debugger mode. With this mode, CPU's execution is stopped, and user can control the CPU's program execution via JTAG Debugger.

3.4.2 Normal Boot Mode

If CFG[0]=1, then *adstar* boots as Normal mode. With this mode, CPU executes a program normally.

3.4.3 Flash Boot Mode

If CFG[3:1]=001b, then *adstar* boots with Flash. With this mode, CPU executes instructions which are already stored into Flash memory (instruction memory).

3.4.4 NOR Flash Boot Mode

If CFG[3:1]=000b, then *adstar* boots with 8-bit NOR Flash. With this mode, CPU executes instructions which are already stored into NOR Flash memory.

3.4.5 NAND Flash Auto Boot Mode

If CFG[3:1] is neither 000b nor 001b, then *adstar* boots with NAND Flash. With this mode, initially, the boot codes are copied into 2KB internal SRAM memory, and then CPU executes the copied instructions.

CFG[3:1]	***NAND Boot Mode***	***NAND Flash Type***
100	Small type 3-Cycle	NAND Flash Small type Address 3 cycles
101	Small type 4-Cycle	NAND Flash Small type Address 4 cycles
110	Large type 4-Cycle	NAND Flash Large type Address 4 cycles
111	Large type 5-Cycle	NAND Flash Large type Address 5 cycles
010	MLC 4-Bit ECC	NAND Flash MLC type 4-bit ECC
011	MLC 24-Bit ECC	NAND Flash MLC type 24-bit ECC

4 SYSTEM RESET AND CLOCK

4.1 Reset

Reset controller consists of External Reset, JTAG Reset, and Watchdog Reset. A following figure 4-1 shows the entire Reset signals.

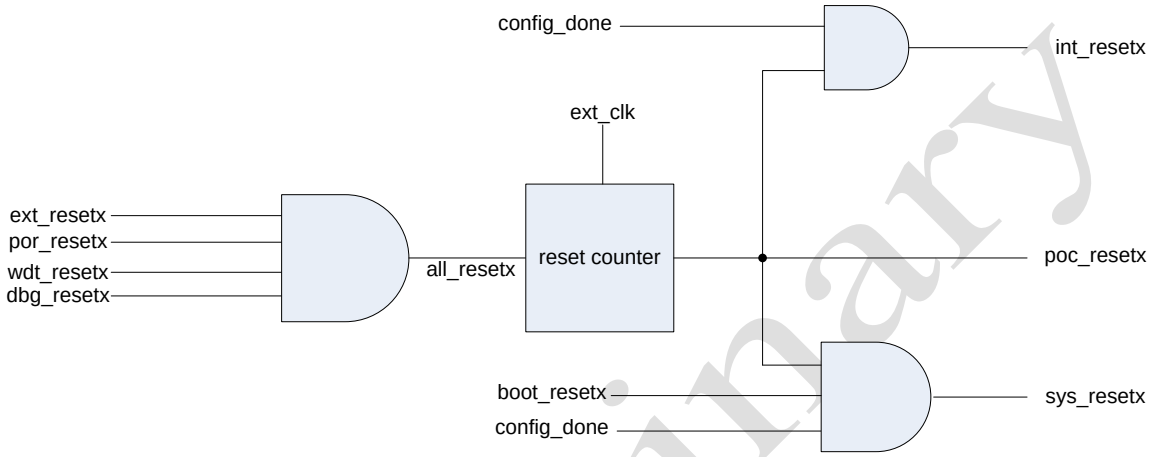


Figure 4-1 Reset

4.1.1 System Reset

The System Reset is occurred at the following categories.

1. External Reset
2. JTAG Reset
3. Watchdog Reset
4. POR Reset

4.1.2 Power On Start Time

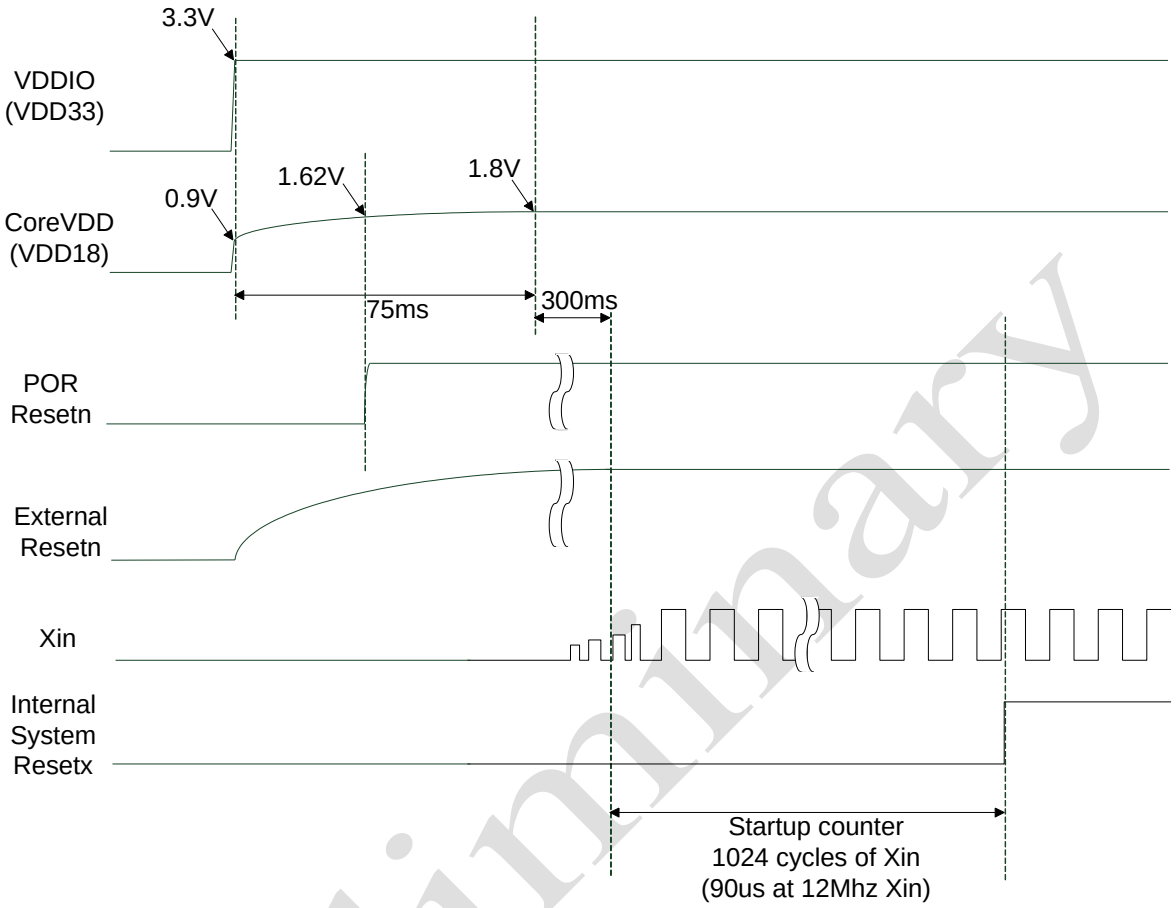


Figure 4-2 Power On Start Time Diagram

4.2 Clocks

The External Clock, that is XIN input signal, uses 1~16 MHz.

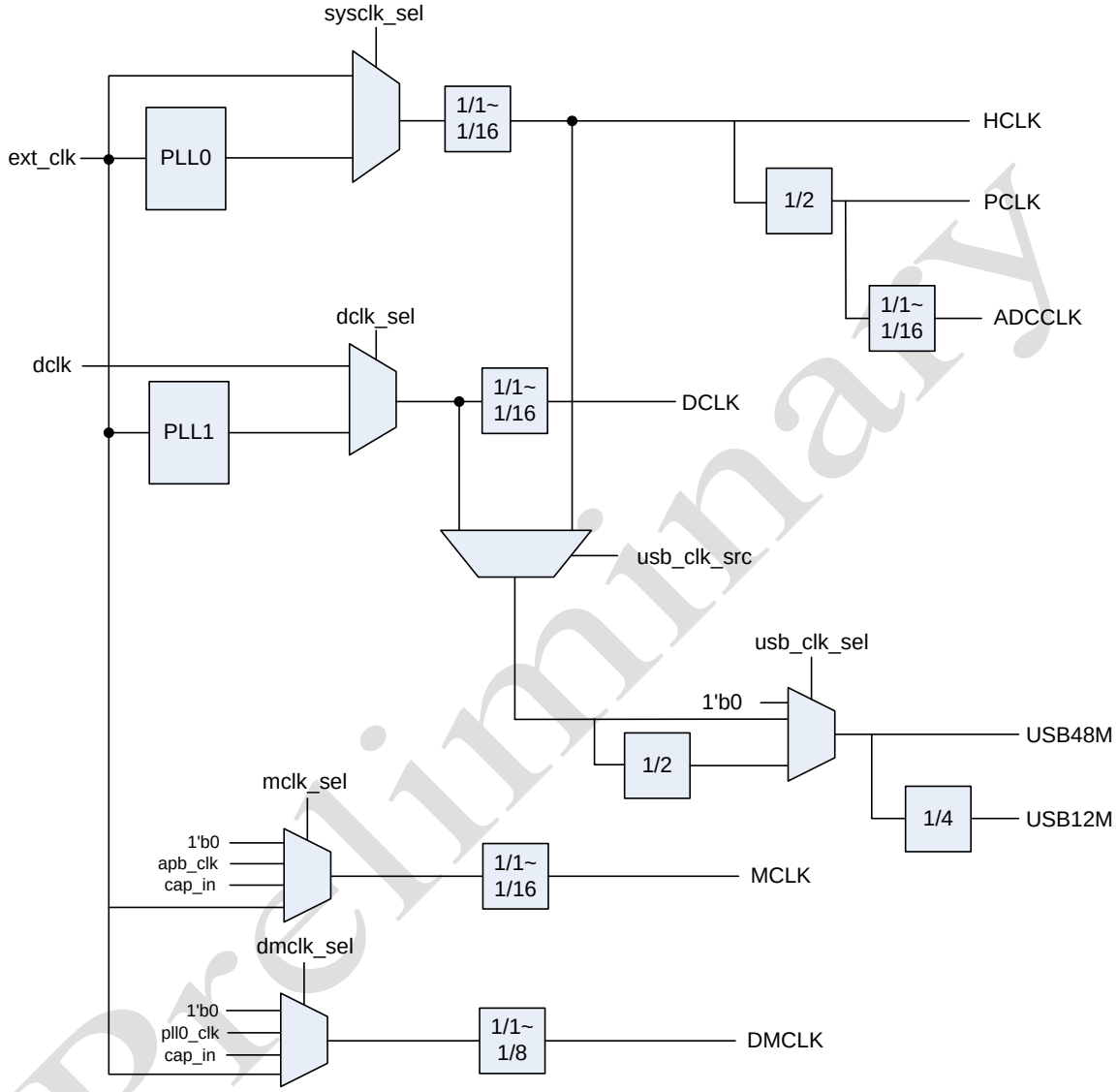


Figure 4-2 Clocks

adstar receives 7 clock sources as inputs.

1. HCLK
2. PCLK
3. DCLK (LCDC)
4. USBCLK
5. TCK (JTAG)
6. MCLK (I2S)
7. DMCLK (Digital Modulator)

HCLK and PCLK clocks supply to AHB and APB, respectively. The two clocks have same phase and 2:1 frequency ratio. The maximum frequency of HCLK is 108MHz and that of PCLK is 54MHz.

DLCK clock supplies to LCDC.

USBCLK clock supplies to USB Host/Device.

TCK clock supplies to JTAG module. The clock is asynchronized with HCLK and PCLK. However, the frequency of the TCK should be under 1/4 of HCLK to operate JTAG module.

MCLK clock supplies to I2S and DMCLK clock supplies to Digital Modulator. It is used for sound output.

4.3 Power Management Unit Registers

4.3.1 PMU Write Enable Register (PMUWREN)

Address : 0x8002_3C00

Bit	*R/W*	*Description*	*Default Value*
31:14	R	Reserved	-
13	R/W	USB PHY Control Register Write Enable	0
12	R/W	PCLK Control Register Write Enable	0
11	R/W	HCLK Control Register Write Enable	0
10	R/W	Sound Clock Control Register Write Enable	0
9	R/W	PLL Control Register Write Enable	0
8	R/W	Clock Control Register Write Enable	0
7:3	R	Reserved	-
2	R/W	Core Clock Off by Halt 3 Enable	0
1:0	R	Reserved	-

* Bit[2] should be set to 1 to disable core clock by Halt 3 command.
* Interrupt request is able to wake up core entered to sleep mode by halt command.

4.3.2 Clock Control Register (CLKCON)

Address : 0x8002_3C20

Bit	R/W	Description	Default Value
31:16	R	Reserved	-
19:16	R/W	AHB Clock Select 0000: System Clock 0001: System Clock / 2 0010: System Clock / 3 0011: System Clock / 4 … 1110: System Clock / 15 1111: System Clock / 16	0
15:12	R/W	LCDC Clock Select 0000: DotSrcClk 0001: DotSrcClk / 2 0010: DotSrcClk / 3 0011: DotSrcClk / 4 … 1110: DotSrcClk / 15 1111: DotSrcClk / 16	0
11:10	R	Reserved	-
9	R/W	LCDC Source Clock Select (DotSrcClk) 0: External LCDC Clock 1: PLL1 Clock	0
8	R/W	LCDC Clock Enable bit 0: LCDC Clock Disable 1: LCDC Clock Enable	1
7:4	R/W	Reserved	-
3	R/W	USB Clock Enable bit 0: USB Clock Disable 1: USB Clock Enable	0
2	R/W	USB Clock Select 0: USB Source Clock / 2 1: USB Source Clock	0
1	R/W	USB Source Clock Select 0: AHB Clock 1: LCDC Clock	0
0	R/W	System Clock Select bit 0: External Clock 1: PLL0 Clock	0

4.3.3 PLL Control Register (PLLCON)

Address : 0x8002_3C24

Bit	R/W	Description	Default Value
31:15	R	Reserved	-
14:12	R/W	PLL1 OS	0
11	R	Reserved	-
10:8	R/W	PLL1 IS	0
7	R	Reserved	-
6:4	R/W	PLL0 OS	0
3	R	Reserved	-
2:0	R/W	PLL0 IS	0

IS[2:0]	Input Divider Ratio(N)
000	1
001	2
010	4
011	6
100	8
101	10
110	12
111	16

OS[2:0]	Feedback Divider Ratio(M)	Output Divider Ratio(O)
000	180	1
001	120	1
010	81	1
011	48	1
100	180	2
101	81	3
110	48	2
111	48	4

* FOUT = (XIN*M)/(N*O) [Where XIN/N is between 1M and 3M, XIN*M/N is between 48M and 180M]

4.3.4 Sound Control Register (SNDCLKCON)

Address : 0x8002_3C28

Bit	R/W	Description	Default Value
31:14	R	Reserved	-
13:12	R/W	Digital Modulator Source Clock (DMCLKSRC) 00: Clock disable 01: External Clock 10: PLL Clock 11: Capture Input[0]	01
11:10	R	Reserved	-
9:8	R/W	Digital Modulator Clock Divide Select 00: DMCLKSRC 01: DMCLKSRC / 2 10: DMCLKSRC / 4 11: DMCLKSRC / 8	00
7:6	R	Reserved	-
5:4	R/W	I2S Source Clock Select 00: Clock disable 01: External Clock 10: APB Clock 11: Capture Input[0]	01
3:0	R/W	I2S Clock Divide Value 0000: I2S Source Clock 0001: I2S Source Clock / 2 0010: I2S Source Clock / 3 … 1110: I2S Source Clock / 15 1111: I2S Source Clock / 16	0

4.3.5 AHB Clock Control Register (HCLKCON)

Address : 0x8002_3C2C

Bit	R/W	Description	Default Value
31:13	R	Reserved	-
12	R/W	USB Host AHB Clock Enable	1
11	R/W	USB Device AHB Clock Enable	1
10	R/W	LCDC AHB Master Clock Enable	1
9	R/W	SDHC Clock Enable	1
8	R/W	NAND Flash Controller Clock Enable	1
7	R/W	External SRAM Controller Clock Enable	1
6	R/W	Flash Controller Clock Enable	1
5	R/W	DMA Clock Enable	1
4	R/W	GPIO Clock Enable	1
3	R/W	Interrupt Controller Clock Enable	1
2	R/W	SDRAM Clock Enable	1
1	R/W	SDRAM Controller Clock Enable	1
0	R/W	AHB Bus Clock Enable	1

4.3.6 APB Clock Control Register (PCLKCON)

Address : 0x8002_3C30

Bit	R/W	Description	Default Value
31:13	R	Reserved	-
12	R/W	Pin MUX Clock Enable	1
11	R/W	ADC APB Clock Enable	1
10	R/W	QEI Clock Enable	1
9	R/W	Dedicated PWM Clock Enable	1
8	R/W	Sound Mixer APB Clock Enable	1
7	R/W	TWI Clock Enable	1
6	R/W	SPI1 Clock Enable	1
5	R/W	SPI0 Clock Enable	1
4	R/W	UART Clock Enable	1
3	R/W	Timer Clock Enable	1
2	R/W	Watch Dog Timer Clock Enable800	1
1	R/W	LCDC APB Slave Clock Enable	1
0	R/W	APB Bus Clock Enable	1

4.3.7 USB PHY Control Register (USBPHYCON)

Address : 0x8002_3C34

Bit	R/W	Description	Default Value
31:9	R	Reserved	-
8	R/W	USB Function Select bit 0: USB Device 1: USB Host	0
7	R	Reserved	-
6	R/W	D- Pull-down Enable bit 0: Pull-down Disable 1:Pull-down Enable	0
5	R/W	D+ Pull-down Enable bit 0: Pull-down Disable 1:Pull-down Enable	0
4	R/W	Receive Enable bit 0: USB PHY does not receive external signal. 1: USB PHY receives external signal	1
3	R/W	D- Weak Pull-up Enable bit 0: Pull-up Disable 1: Pull-up Enable	0
2	R/W	D- Pull-up Enable bit 0: Pull-up Disable 1: Pull-up Enable	0
1	R/W	D+ Weak Pull-up Enable bit 0: Pull-up Disable 1: Pull-up Enable	0
0	R/W	D+ Pull-up Enable bit 0: Pull-up Disable 1: Pull-up Enable	0

5 COPROCESSOR

Coprocessor of *adstar* includes Memory Management Unit (MMU) and I-Cache, D-Cache functional blocks. It controls the functional blocks and additional blocks.

5.1 Features

- Memory Management Unit
  - Real Memory mode
- 2 Way Set Associative Harvard Cache
  - 8KBytes I-Cache
  - 8KBytes D-Cache
  - Write Through
  - 16 Bytes / Line
  - LRU Replacement
  - Cache Invalidation by Software
- 4 Words Deep Write Buffer (FIFO)

With the Real Memory mode, CPU can access reserved portion of memory space for 4GB linear memory space. The accessing address of CPU exactly matches with physical memory address.

Table 5-1 Real Memory map

Address Range	*Sector Number*	*Size*
0x0000_0000~0x000F_FFFF (Memory Bank0)	Flash	512KBytes
0x1000_0000~0x1000_07FF (Memory Bank0)	Internal SRAM for Instruction	2KBytes
0x1800_0000~0x1800_77FF (Memory Bank1)	Internal SRAM for Data	30KBytes
0x2000_0000 ~ 0x2FFF_FFFF	SDRAM	8 or 16Mbytes
0x5000_0000 ~ 0x5FFF_FFFF	External SRAM	-

5.2 Coprocessor Description

Table 5-2 Coprocessor Register Description

Register	*R/W*	*Description*
SCPR15	R	System Coprocessor Status Register
	W	Master Command Register
SCPR14	R/W	Supervisor Stack Point Register
SCPR13	R/W	User Stack Pointer
SCPR12	R/W	Vector Base Register
SCPR11	W	Invalidate Cache Line and Lock Register
SCPR10	-	Reserved
SCPR9	R/W	Memory Bank Configuration Register
SCPR8	R/W	Sub-Bank Configuration Register
SCPR7	R/W	Reserved
SCPR6	R/W	Reserved
SCPR5	R/W	Sub-Bank Address Register
SCPR4	R/W	General Access Point Data Register
SCPR3	R/W	General Access Point Index Register
SCPR2	R/W	Reserved
SCPR1	R/W	Reserved
SCPR0	R/W	Reserved

5.3 Coprocessor Control Registers

5.3.1 System Coprocessor Status Register (SCPR15)

Bit	R/W	Description	Default Value
31	R	System Co-Processor Access Right (Privileged) 0 : Supervisor/User Accessible 1 : Supervisor Access only	1
30 : 28	R	Coprocessor Type	001
27 : 25	R	Coprocessor Subtype	000
24 : 19	R	Reserved	-
18	R	L1 Cache Presented 0 : Presented 1 : Not Presented	0
17	R	L1 Cache Snooping Capability 0 : Support Snooping 1 : Not support Snooping	1
16 : 7	R	Reserved	-
6	R	Misalign Correction Support for Data Access 0 : Not support Misalign Correction 1 : Support Misalign Correction	0
5 : 2	R	SCP Rending Exception Number 0000 : Inst. Fetch - Access Violation 0010 : Privilege Violation Exception 0011 : Data Access - Address Misalignment 0100 : Data Access - Access Violation 1000 : Inst. Fetch - Address Misalignment 1111 : N/A	1111
1	R	SCP Pending Exception status 0 : No Pending Exception 1 : Pending Exception Exist	0
0	R	Reserved	-

5.3.2 Master Command Register (SCPR15)

Bit	R/W	Description	Default Value
31 : 6	W	Reserved	-
5 : 2	W	End of Exception 0000 : Inst. Fetch - Access Violation 0010 : Privilege Violation Exception 0011 : Data Access - Address Misalignment 0100 : Data Access - Access Violation 1000 : Inst. Fetch - Address Misalignment 1111 : Privilege Violation Exception	1111
1 : 0	W	Reserved	-

5.3.3 Supervisor Stack Point Register (SCPR14)

Bit	R/W	Description	Default Value
31 : 2	R/W	Supervisor Stack Pointer	0x0000_0000
1 : 0	R/W	Always 0	00

5.3.4 User Stack Point Register (SCPR13)

Bit	R/W	Description	Default Value
31 : 2	R/W	User Stack Pointer	0x0000_0000
1 : 0	R/W	Always 0	00

5.3.5 Vector Base Register (SCPR12)

Bit	R/W	Description	Default Value
31 : 2	R/W	Vector Base for Exception	0x0000_0000
1 : 0	R/W	Always 0	00

5.3.6 Invalidate Cache Line and Lock Register (SCPR11)

Bit	R/W	Description	Default Value
31 : 7	W	Invalidation Target Address/Way	-
6 : 4	W	Invalidation Target Address/Way	-
3	W	Invalidation Mode 0 : Address Based Invalidation 1 : Way Based Invalidation	-
2	W	Copy-back Selection in Invalidation 0 : Invalidation without Copy-back 1 : Invalidation with Copy-back if need	-
1	W	Cache Line Locking in Invalidation 0 : Invalidation without Locking 1 : Invalidation with Locking	-
0	W	Cache Type in Invalidation 0 : I-Cache 1 : D-Cache	-

5.3.7 Memory Bank Configuration Register (SCPR9)

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	0
15	R/W	Always 0	0
14	R/W	Memory Bank 3 Access Right 0 : Supervisor only Accessible 1 : Supervisor/User Accessible	0
13 : 12	R/W	Memory Bank 3 Cache Configuration 00 : Disable Cache 01 : Reserved 10 : Enable Cache with Write-through 11 : N/A	00
11	R/W	Always 0	0
10	R/W	Memory Bank 2 Access Right 0 : Supervisor only Accessible 1 : Supervisor/User Accessible	0
9 : 8	R/W	Memory Bank 2 Cache Configuration 00 : Disable Cache 01 : Reserved 10 : Enable Cache with Write-through 11 : N/A	00
7	R/W	Always 0	0
6	R/W	Memory Bank 1 Access Right 0 : Supervisor only Accessible 1 : Supervisor/User Accessible	0
5 : 4	R/W	Memory Bank 1 Cache Configuration 00 : Disable Cache 01 : Reserved 10 : Enable Cache with Write-through 11 : N/A	00
3	R/W	Always 0	0
2	R/W	Memory Bank 0 Access Right 0 : Supervisor only Accessible 1 : Supervisor/User Accessible	0
1 : 0	R/W	Memory Bank 0 Cache Configuration 00 : Disable Cache 01 : Reserved 10 : Enable Cache with Write-through 11 : N/A	00

5.3.8 Sub-Bank Configuration Register (SCPR8)

Bit	R/W	Description	Default Value
31 : 7	R	Reserved	-
6 : 4	R/W	Sub-Bank Index	000
3	R/W	Sub-Bank Valid Control bit 0 : Invalid 1 : Valid	0
2	R/W	Sub-Bank Access Right 0 : Supervisor only Accessible 1 : Supervisor/User Accessible	0
1 : 0	R/W	Sub-Bank Cache Property Control bit 00 : Disable Cache 01 : N/A 10 : Enable Cache with Write-through 11 : N/A	00

*** The SCPR8 is configured with SCPR5 and Specifies Sub-Bank.
*** The memory space that is configured with Sub-Bank has higher priority than the memory bank configuration of SCPR9.

5.3.9 Sub-Bank Address Register (SCPR5)

Bit	R/W	Description	Default Value
31 : 12	R/W	Sub-Bank Base Address[31:12]	0x00000
11 : 0	R/W	Sub-Bank Size Enable 0x000 : 4KBytes 0x001 : 8KBytes 0x003 : 16KBytes 0x007 : 32KBytes 0x00F : 64KBytes 0x01F : 128KBytes 0x03F : 256KBytes 0x07F : 512KBytes 0x0FF : 1MBytes	0x000

*** An alignment should be Nature Align when Sub-Bank is enabled.

5.3.10 General Access Point Data Register (SCPR4)

Bit	R/W	Description	Default Value
31 : 0	R/W	General Access Point Data Register value that is configured at SCPR3	0x0000_0000

5.3.11 General Access Point Index Register (SCPR3)

Bit	R/W	Description	Default Value
31 : 0	R/W	General Access Point Index - Core Debugging Information 0x0000_0000 : Backup IR 0x0000_0001 : Backup ER 0x0000_0002 : Backup PC 0x0000_0010 : Backup EAD - System Coprocessor Debugging Information 0x0000_0303 : Inst. Bus Error Address 0x0000_0304 : Data Bus Error Address - Cache Lock Information 0x0000_0500 : Inst. Lock Condition 0x0000_0501 : Data Lock Condition - Memory Bank Management Information 0x0000_0600 : Inst. MBMB Violation Address 0x0000_0601 : Data MBMB Violation Address - Internal SRAM Configuration Information 0x0000_0700 : Global Control Reg. Address Local Control Registers 0x0000_0701 : Local I-Control Reg.0 Address 0x0000_0711 : Local I-Control Reg.1 Address 0x0000_0721 : Local I-Control Reg.2 Address 0x0000_0731 : Local I-Control Reg.3 Address 0x0000_0704 : Local D-Control Reg.0 Address 0x0000_0714 : Local D-Control Reg.1 Address 0x0000_0724 : Local D-Control Reg.2 Address 0x0000_0734 : Local D-Control Reg.3 Address Local Start Address Registers 0x0000_0702 : Local I-Start Reg.0 Address 0x0000_0712 : Local I-Start Reg.1 Address 0x0000_0722 : Local I-Start Reg.2 Address 0x0000_0732 : Local I-Start Reg.3 Address 0x0000_0705 : Local D-Start Reg.0 Address 0x0000_0715 : Local D-Start Reg.1 Address 0x0000_0725 : Local D-Start Reg.2 Address 0x0000_0735 : Local D-Start Reg.3 Address Local End Address Registers 0x0000_0703 : Local I-End Reg.0 Address 0x0000_0713 : Local I-End Reg.1 Address	0x0000_0000

		0x0000_0723 : Local I-End Reg.2 Address 0x0000_0733 : Local I-End Reg.3 Address 0x0000_0706 : Local D-End Reg.0 Address 0x0000_0716 : Local D-End Reg.1 Address 0x0000_0726 : Local D-End Reg.2 Address 0x0000_0736 : Local D-End Reg.3 Address	

6 WATCHDOG TIMER

Watchdog Timer is responsible for rollback the system when CPU operates wrong execution due to system errors, device's wrong response, and noise.

If the watchdog time is enabled, the counter value WDTCNT is decreased by 1, and when the value becomes 0, Watchdog Reset is occurred.

If the Watchdog Reset is signaled, the status of the system is stored into WDTST bit.

In order to prevent Watchdog Reset from system under Watchdog Timer enabled, because 32-bit Watchdog Counter value should not be 0, developer should re-configure the WDTCNT.

If WDTMOD bit is set as Interrupt mode, system occurs Interrupt rather Watchdog Reset. In that case, the system informs that WDTCNT value is 0.

6.1 Register Description

6.1.1 Watchdog Timer Control Register (WDTCTRL)

Address : 0x8002_0000

Bit	R/W	Description	Default Value
31 : 5	R	Reserved	-
4	R	WDTST : Watchdog timer status bit When watchdog timer is reset mode, 0 : No watchdog reset 1 : Watchdog reset When watchdog timer is interrupt mode, 0 : No watchdog interrupt 1 : Watchdog interrupt Clear at read	0
3 : 2	R	Reserved	-
1	R/W	WDTMOD : Watchdog timer mode select bit 0 : Reset mode 1 : Interrupt mode	0
0	R/W	WDTEN : Watchdog timer enable bit 0 : Disable 1 : Enable	0

6.1.2 Watchdog Timer Counter Value Register (WDTCNT)

Address : 0x8002_0004

Bit	R/W	Description	Default Value
31 : 0	R/W	Watchdog timer counter 32-bit value. Down-counter	0xFFFF_FFFF

7 GPIO (GENERAL PURPOSE I/O)

The GPIO Ports are composed of 8-bit 9 blocks and 3-bit 1 block. The GPIO provides totally 74 or 69 I/O ports. Each port can be configured with register easily, and can be used for various input/output and system organization.

7.1 Features

- GP0.x has 8 I/O Ports(adStar-8/16M) or 5 I/O Ports(adStar-8/16MF512)
- GP1.x has 8 I/O Ports
- GP2.x has 8 I/O ports
- GP3.x has 8 I/O ports
- GP4.x has 8 I/O Ports
- GP5.x has 8 I/O Ports
- GP6.x has 8 I/O ports
- GP7.x has 8 I/O ports
- GP8.x has 8 I/O Ports
- GP9.x has 3 I/O Ports(adStar-8/16M Only)

7.2 Block Diagram

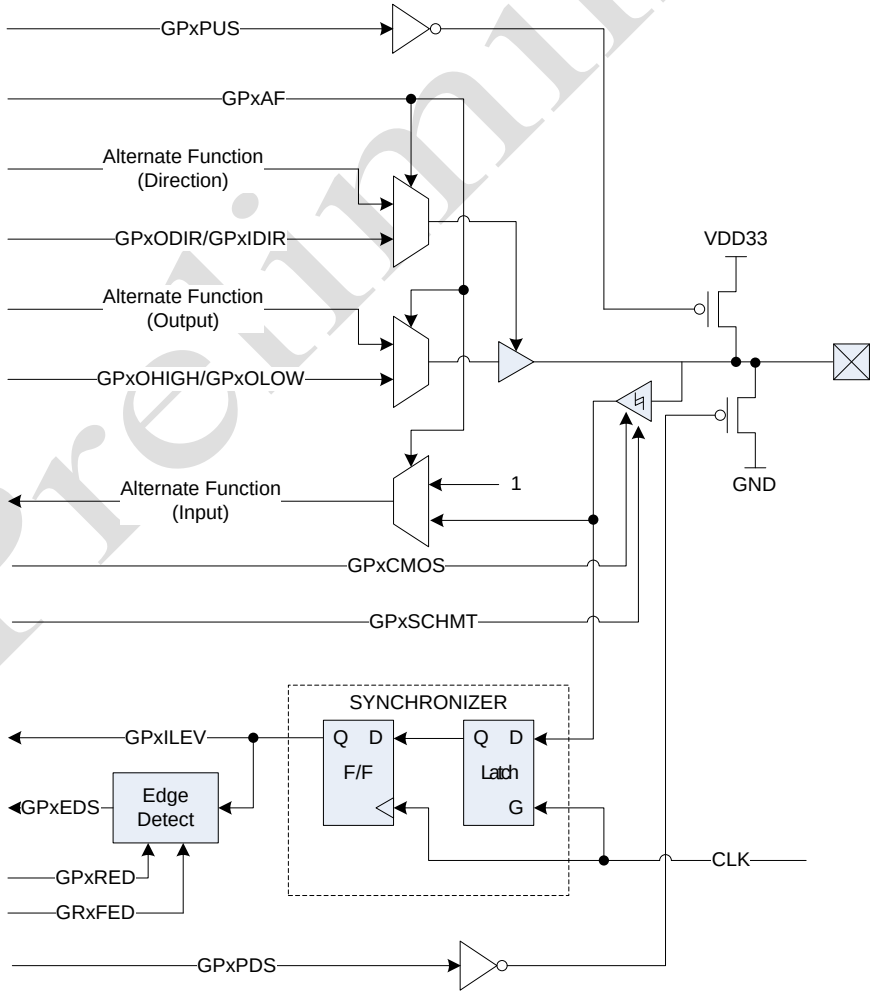


Figure 7-1 GPIO Block Diagram

7.3 Function Description

7.3.1 Port Control

GPIO Ports are configured as Output mode by GPxODIR register and configured as Input mode by GPxIDIR register port by port. The configured status of each port is stored into GPxDIR register. When user configures GPxODIR register and GPxIDIR register, the value of bit is 1 is configured as the corresponding operation and that of bit is 0 does not affect anything.

The output level of GPIO Ports is set to High Level via GPxOHIGH register under Output mode and is set to Low Level via GPxOLOW register. The status of Output Level can be confirmed by checking GPxOLEV register.

The Input level of GPIO can be confirmed by checking GPxILEV. The Pull-up resistance is connected to each port. User can reduce leakage current if use removes Pull-up under the external input exists or ouput.

Table 7-1 Internal Pull-up Resistance Characteristics

Parameter	*Min*	*Typ*	*Max*	*Unit*
Pull-Up Resistance	34	41	64	KΩ
Pull-Down Resistance	33	44	79	KΩ

7.3.2 Port Edge Detect

External interrupt can be performed for each group by GPIO's Port Edge Detect as well as EIRQ pin. The port provides Rising Edge, Falling Edge and Any Edge modes.

7.3.3 Port Alternate Functions

The initial value of GPIO Ports is Input stat, and shares peripheral functions that are external interface by configuring Alternate Functions. The default selection is GPIO, but developer can use other functions by setting register. In addition, according to the booting mode, the default value of port is changed and a part of GPIO is reserved for specific purpose by nTEST pin.

Register	*bit*	*1st*	*2nd*	*3rd*	*4th*	*Default*
		00	*01*	*10*	*11*	
PAF0 0x80023400	1:0	-	spi_cs0	twi_scl	P0.0	11b
	3:2	-	spi_miso0	twi_sda	P0.1	
	5:4	snd2_pwmr_p	spi_mosi0	sram_cs1#	P0.2	
	7:6	snd2_pwmr_n	spi_sck0	sram_cs2#	P0.3	
	9:8	snd3_pwml_p	flash_cs	cap_in1	P0.4	Flash Boot: 01b Etc.: 11b *adStar 8/16M Only
	11:10	snd3_pwml_n	flash_dq1	tm_out1	P0.5	
	13:12	snd3_pwmr_p	flash_dq2	uart_tx4	P0.6	

	15:14	snd3_pwmr_n	TAP_SEL	uart_rx4	P0.7	nTEST = 0 : fixed 01b Etc. : 11b
PAF1 0x80023404	1:0	uart_tx0	snd_mclk	twi_scl	P1.0	11b
	3:2	uart_rx0	snd0_sdi	twi_sda	P1.1	
	5:4	nf_cs#	pwm_fault1	sram_cs1#	P1.2	NAND Boot: 00b NOR Boot: 10b Etc.: 11b
	7:6	nf_ale	sdhc_cmd	sram_cs3#	P1.3	
	9:8	nf_cle	sdhc_clk	sram_be1#	P1.4	
	11:10	nf_we	snd0_sclk	sram_a17	P1.5	
	13:12	nf_re	snd0_lrclk	sram_a18	P1.6	
	15:14	nf_busyx	snd0_sdo	sram_wait#	P1.7	
PAF2 0x80023408	1:0	nf_d0	uart_tx3	sram_a8/d8	P2.0	NAND Boot: 00b NOR Boot: 10b Etc.: 11b
	3:2	nf_d1	uart_rx3	sram_a9/d9	P2.1	
	5:4	nf_d2	uart_tx4	sram_a10/d10	P2.2	
	7:6	nf_d3	uart_rx4	sram_a11/d11	P2.3	
	9:8	nf_d4	sdhc_d0	sram_a12/d12	P2.4	
	11:10	nf_d5	sdhc_d1	sram_a13/d13	P2.5	
	13:12	nf_d6	sdhc_d2	sram_a14/d14	P2.6	
	15:14	nf_d7	sdhc_d3	sram_a15/d15	P2.7	
PAF3 0x8002340C	1:0	sram_a0/a8/d0	pwm_h0	cap_in0	P3.0	NOR Boot: 00b Etc.: 11b
	3:2	sram_a1/a9/d1	pwm_l0	tm_out0	P3.1	
	5:4	sram_a2/a10/d2	pwm_h1	uart_tx3	P3.2	
	7:6	sram_a3/a11/d3	pwm_l1	uart_rx3	P3.3	
	9:8	sram_a4/a12/d4	pwm_h2	cap_in2	P3.4	
	11:10	sram_a5/a13/d5	pwm_l2	tm_out2	P3.5	
	13:12	sram_a6/a14/d6	pwm_h3	ohci_overcurrent	P3.6	
	15:14	sram_a7/a15/d7	pwm_l3	ohci_portpower	P3.7	
PAF4 0x80023410	1:0	sram_a16	pwm_fault0	eirq0	P4.0	NOR Boot: 00b Etc.: 11b
	3:2	sram_ale0		eirq1	P4.1	
	5:4	sram_ale1		uart_tx1	P4.2	
	7:6	sram_re#		uart_rx1	P4.3	
	9:8	sram_we#	twi_scl	uart_tx2	P4.4	
	11:10	sram_cs0#	twi_sda	uart_rx2	P4.5	
	13:12	snd_mclk	spi_sck1	cap_in3	P4.6	11b
	15:14	snd0_sdi	spi_cs1	tm_out3	P4.7	
PAF5 0x80023414	1:0	snd0_sclk	spi_miso1	sram_a0	P5.0	NOR Boot: 10b
	3:2	snd0_lrclk	spi_mosi1	sram_a1	P5.1	
	5:4	snd0_sdo	uart_tx0	sram_a2	P5.2	
	7:6	lcdc_clk_in	uart_rx0	sram_a3	P5.3	
	9:8	vsync	eirq0	sram_a4	P5.4	
	11:10	hsync	eirq1	sram_a5	P5.5	
	13:12	disp_en	uart_tx1	sram_a6	P5.6	
	15:14	lcdc_clk_out	uart_rx1	sram_a7	P5.7	
PAF6	1:0	r0	nTRST		P6.0	Default : 01b
	3:2	r1	TCK		P6.1	

0x80023418	5:4	r2	TDI		P6.2	
	7:6	r3	sdhc_cmd	snd1_sclk	P6.3	11b
	9:8	r4	sdhc_d0	snd1_lrclk	P6.4	
	11:10	r5	sdhc_d1	snd1_sdo	P6.5	
	13:12	r6	sdhc_d2	uart_tx2	P6.6	
	15:14	r7	sdhc_d3	uart_rx2	P6.7	
PAF7 0x8002341C	1:0	g0	TMS	sram_cs1#	P7.0	Default: 01b
	3:2	g1	TDO	sram_cs2#	P7.1	
	5:4	g2	sdhc_clk	sram_a10	P7.2	NOR Boot: 10b Etc.: 11b
	7:6	g3	cfg0	sram_a11	P7.3	
	9:8	g4	cfg1	sram_a12	P7.4	
	11:10	g5	cfg2	sram_a13	P7.5	
	13:12	g6	cfg3	sram_a14	P7.6	
	15:14	g7	cfg4	sram_a15	P7.7	
PAF8 0x80023420	1:0	b0	snd2_pwml_p	sram_a8	P8.0	NOR Boot: 10b Etc.: 11b
	3:2	b1	snd2_pwml_n	sram_a9	P8.1	
	5:4	b2	snd2_pwmr_p	cap_in1	P8.2	11b
	7:6	b3	snd2_pwmr_n	tm_out1	P8.3	
	9:8	b4	snd3_pwml_p	cap_in2	P8.4	
	11:10	b5	snd3_pwml_n	tm_out2	P8.5	
	13:12	b6	snd3_pwmr_p	cap_in3	P8.6	
	15:14	b7	snd3_pwmr_n	tm_out3	P8.7	
PAF9 0x80023424	1:0	snd1_sclk	flash_dq0	cap_in0	P9.0	Flash Boot: 01b Etc.: 11b *adStar 8/16M Only
	3:2	snd1_lrclk	flash_clk	tm_out0	P9.1	
	5:4	snd1_sdo	flash_dq3	sram_cs3#	P9.2	

7.4 Register Description

7.4.1 Port Direction Registers (GPxDIR)

Address: 0xFFFF_3000 / 0xFFFF_3040 / 0xFFFF_3080 / 0xFFFF_30C0 / 0xFFFF_3100 / 0xFFFF_3140 / 0xFFFF_3180 / 0xFFFF_31C0 / 0xFFFF_3200 / 0xFFFF_3240

Bit	R/W	Description	Default Value
31 : 9	R	Reserved	-
8	R	GPx.OMD : GPx. Output Control Mode bit 0 : Control individual ports 1 : Control a group of 8 ports	0
7 : 0	R	GPx.yDIR : GPx.y Direction bit 0 : Input 1 : Output	0x00

7.4.2 Port Direction Output Mode Setting Registers (GPxODIR)

Address: 0xFFFF_3000 / 0xFFFF_3040 / 0xFFFF_3080 / 0xFFFF_30C0 / 0xFFFF_3100 / 0xFFFF_3140 / 0xFFFF_3180 / 0xFFFF_31C0 / 0xFFFF_3200 / 0xFFFF_3240

Bit	R/W	Description	Default Value
31 : 9	R	Reserved	-
8	W	GPx.OPRT : Output Control by Port Mode Setting bit	-
7	W	GPx.7ODIR : GPx.7 Direction Output Mode Setting bit	-
6	W	GPx.6ODIR : GPx.6 Direction Output Mode Setting bit	-
5	W	GPx.5ODIR : GPx.5 Direction Output Mode Setting bit	-
4	W	GPx.4ODIR : GPx.4 Direction Output Mode Setting bit	-
3	W	GPx.3ODIR : GPx.3 Direction Output Mode Setting bit	-
2	W	GPx.2ODIR : GPx.2 Direction Output Mode Setting bit	-
1	W	GPx.1ODIR : GPx.1 Direction Output Mode Setting bit	-
0	W	GPx.0ODIR : GPx.0 Direction Output Mode Setting bit	-

*** Port Direction Output Mode Setting bit
0 : No effect 1 : Set to output mode the corresponding bit

7.4.3 Port Direction Input Mode Setting Registers (GPxIDIR)

Address: 0xFFFF_3004 / 0xFFFF_3044 / 0xFFFF_3084 / 0xFFFF_30C4 / 0xFFFF_3104 / 0xFFFF_3144 / 0xFFFF_3184 / 0xFFFF_31C4 / 0xFFFF_3204 / 0xFFFF_3244

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
8	W	GPx.IPRT : Output Control by Port Mode Setting bit	-
7	W	GPx.7IDIR : GPx.7 Direction Input Mode Setting bit	-
6	W	GPx.6IDIR : GPx.6 Direction Input Mode Setting bit	-
5	W	GPx.5IDIR : GPx.5 Direction Input Mode Setting bit	-
4	W	GPx.4IDIR : GPx.4 Direction Input Mode Setting bit	-
3	W	GPx.3IDIR : GPx.3 Direction Input Mode Setting bit	-
2	W	GPx.2IDIR : GPx.2 Direction Input Mode Setting bit	-
1	W	GPx.1IDIR : GPx.1 Direction Input Mode Setting bit	-
0	W	GPx.0IDIR : GPx.0 Direction Input Mode Setting bit	-

*** Port Direction Input Mode Setting bit
0 : No effect 1 : Set to input mode the corresponding bit

7.4.4 Port Output Data Level Registers (GPxOLEV)

Address: 0xFFFF_3008 / 0xFFFF_3048 / 0xFFFF_3088 / 0xFFFF_30C8 / 0xFFFF_3108 / 0xFFFF_3148 / 0xFFFF_3188 / 0xFFFF_31C8 / 0xFFFF_3208 / 0xFFFF_3248

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R	GPx.yOLEV : GPx.y Output Level bit 0 : Low Level 1 : High Level	0xFF

7.4.5 Port Output Data Registers (GPxDOUT)

Address: 0xFFFF_3008 / 0xFFFF_3048 / 0xFFFF_3088 / 0xFFFF_30C8 / 0xFFFF_3108 / 0xFFFF_3148 / 0xFFFF_3188 / 0xFFFF_31C8 / 0xFFFF_3208 / 0xFFFF_3248

Bit	R/W	Description	Default Value
7 : 0	R/W	GPx.DO : GPx.Port Output Data	0xFF

*** If the value of GPxDIR[8] is 1, It decides GPIO Port ouput by the register.

7.4.6 Port Output Data High Level Setting Registers (GPxOHIGH)

Address: 0xFFFF_3008 / 0xFFFF_3048 / 0xFFFF_3088 / 0xFFFF_30C8 / 0xFFFF_3108 / 0xFFFF_3148 / 0xFFFF_3188 / 0xFFFF_31C8 / 0xFFFF_3208 / 0xFFFF_3248

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	W	GPx.7OH : GPx.7 Output Data High Level Setting bit	-
6	W	GPx.6OH : GPx.6 Output Data High Level Setting bit	-
5	W	GPx.5OH : GPx.5 Output Data High Level Setting bit	-
4	W	GPx.4OH : GPx.4 Output Data High Level Setting bit	-
3	W	GPx.3OH : GPx.3 Output Data High Level Setting bit	-
2	W	GPx.2OH : GPx.2 Output Data High Level Setting bit	-
1	W	GPx.1OH : GPx.1 Output Data High Level Setting bit	-
0	W	GPx.0OH : GPx.0 Output Data High Level Setting bit	-

*** Port Output Data High Level Setting bit (It is effective only when GPxDIR[8] is 0.)
0 : No effect
1 : Set to high level output data the corresponding bit

7.4.7 Port Output Data Low Level Setting Registers (GPxOLOW)

Address: 0xFFFF_300C / 0xFFFF_304C / 0xFFFF_308C / 0xFFFF_30CC / 0xFFFF_310C / 0xFFFF_314C / 0xFFFF_318C / 0xFFFF_31CC / 0xFFFF_320C / 0xFFFF_324C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	W	GPx.7OL : GPx.7 Output Data Low Level Setting bit	-
6	W	GPx.6OL : GPx.6 Output Data Low Level Setting bit	-
5	W	GPx.5OL : GPx.5 Output Data Low Level Setting bit	-
4	W	GPx.4OL : GPx.4 Output Data Low Level Setting bit	-
3	W	GPx.3OL : GPx.3 Output Data Low Level Setting bit	-
2	W	GPx.2OL : GPx.2 Output Data Low Level Setting bit	-
1	W	GPx.1OL : GPx.1 Output Data Low Level Setting bit	-
0	W	GPx.0OL : GPx.0 Output Data Low Level Setting bit	-

*** Port Output Data Low Level Setting bit (It is effective only when GPxDIR[8] is 0.)
0 : No effect
1 : Set to low level output data the corresponding bit

7.4.8 Port Input Data Level Registers (GPxILEV)

Address: 0xFFFF_3010 / 0xFFFF_3050 / 0xFFFF_3090 / 0xFFFF_30D0 / 0xFFFF_3110 / 0xFFFF_3150 / 0xFFFF_3190 / 0xFFFF_31D0 / 0xFFFF_3210 / 0xFFFF_3250

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	R	GPx.7ILEV : GPx.7 Input Level bit 0 : Low Level 1 : High Level	-
6	R	GPx.6ILEV : GPx.6 Input Level bit 0 : Low Level 1 : High Level	-
5	R	GPx.5ILEV : GPx.5 Input Level bit 0 : Low Level 1 : High Level	-
4	R	GPx.4ILEV : GPx.4 Input Level bit 0 : Low Level 1 : High Level	-
3	R	GPx.3ILEV : GPx.3 Input Level bit 0 : Low Level 1 : High Level	-
2	R	GPx.2ILEV : GPx.2 Input Level bit 0 : Low Level 1 : High Level	-
1	R	GPx.1ILEV : GPx.1 Input Level bit 0 : Low Level 1 : High Level	-
0	R	GPx.0ILEV : GPx.0 Input Level bit 0 : Low Level 1 : High Level	-

7.4.9 Port Pull-up Status Registers (GPxPUS)

Address: 0xFFFF_3018 / 0xFFFF_3058 / 0xFFFF_3098 / 0xFFFF_30D8 / 0xFFFF_3118 / 0xFFFF_3158 / 0xFFFF_3198 / 0xFFFF_31D8 / 0xFFFF_3218 / 0xFFFF_3258

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R	GPx.yUP : GPx.y Pull-up Status bit 0 : Pull-up Disable 1 : Pull-up Enable	0x0

7.4.10 Port Pull-up Enable Registers (GPxPUEN)

Address: 0xFFFF_3018 / 0xFFFF_3058 / 0xFFFF_3098 / 0xFFFF_30D8 / 0xFFFF_3118 / 0xFFFF_3158 / 0xFFFF_3198 / 0xFFFF_31D8 / 0xFFFF_3218 / 0xFFFF_3258

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	W	GPx.7PUEN : GPx.7 Pull-up enable bit	-
6	W	GPx.6PUEN : GPx.6 Pull-up enable bit	-
5	W	GPx.5PUEN : GPx.5 Pull-up enable bit	-
4	W	GPx.4PUEN : GPx.4 Pull-up enable bit	-
3	W	GPx.3PUEN : GPx.3 Pull-up enable bit	-
2	W	GPx.2PUEN : GPx.2 Pull-up enable bit	-
1	W	GPx.1PUEN : GPx.1 Pull-up enable bit	-
0	W	GPx.0PUEN : GPx.0 Pull-up enable bit	-

*** Port Pull-up enable bit

0 : No effect

1 : the pull up of corresponding bit is set to enable.

7.4.11 Port Pull-up Disable Registers (GPxPUDIS)

Address: 0xFFFF_301C / 0xFFFF_305C / 0xFFFF_309C / 0xFFFF_30DC / 0xFFFF_311C / 0xFFFF_315C / 0xFFFF_319C / 0xFFFF_31DC / 0xFFFF_321C / 0xFFFF_325C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	W	GPx.7PUDIS : GPx.7 Pull-up disable bit	-
6	W	GPx.6PUDIS : GPx.6 Pull-up disable bit	-
5	W	GPx.5PUDIS : GPx.5 Pull-up disable bit	-
4	W	GPx.4PUDIS : GPx.4 Pull-up disable bit	-
3	W	GPx.3PUDIS : GPx.3 Pull-up disable bit	-
2	W	GPx.2PUDIS : GPx.2 Pull-up disable bit	-
1	W	GPx.1PUDIS : GPx.1 Pull-up disable bit	-
0	W	GPx.0PUDIS : GPx.0 Pull-up disable bit	-

*** Port Pull-up disable bit

0 : No effect

1 : the pull down of corresponding bit is set to disable.

7.4.12 Port Rising Edge Detect Registers (GPxRED)

Address: 0xFFFF_3020 / 0xFFFF_3060 / 0xFFFF_30A0 / 0xFFFF_30E0 / 0xFFFF_3120 / 0xFFFF_3160 / 0xFFFF_31A0 / 0xFFFF_31E0 / 0xFFFF_3220 / 0xFFFF_3260

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	R/W	GPx.7RED : GPx.7 Rising Edge Detect bit 0 : Disable 1 : Enable	0
6	R/W	GPx.6RED : GPx.6 Rising Edge Detect bit 0 : Disable 1 : Enable	0
5	R/W	GPx.5RED : GPx.5 Rising Edge Detect bit 0 : Disable 1 : Enable	0
4	R/W	GPx.4RED : GPx.4 Rising Edge Detect bit 0 : Disable 1 : Enable	0
3	R/W	GPx.3RED : GPx.3 Rising Edge Detect bit 0 : Disable 1 : Enable	0
2	R/W	GPx.2RED : GPx.2 Rising Edge Detect bit 0 : Disable 1 : Enable	0
1	R/W	GPx.1RED : GPx.1 Rising Edge Detect bit 0 : Disable 1 : Enable	0
0	R/W	GPx.0RED : GPx.0 Rising Edge Detect bit 0 : Disable 1 : Enable	0

*** When both Rising Edge and Falling Edge are set, Edge detect mode becomes Any Edge mode.

7.4.13 Port Falling Edge Detect Registers (GPxFED)

Address: 0xFFFF_3024 / 0xFFFF_3064 / 0xFFFF_30A4 / 0xFFFF_30E4 / 0xFFFF_3124 / 0xFFFF_3164 / 0xFFFF_31A4 / 0xFFFF_31E4 / 0xFFFF_3224 / 0xFFFF_3264

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	R/W	GPx.7FED : GPx.7 Falling Edge Detect bit 0 : Disable 1 : Enable	0
6	R/W	GPx.6FED : GPx.6 Falling Edge Detect bit 0 : Disable 1 : Enable	0
5	R/W	GPx.5FED : GPx.5 Falling Edge Detect bit 0 : Disable 1 : Enable	0
4	R/W	GPx.4FED : GPx.4 Falling Edge Detect bit 0 : Disable 1 : Enable	0
3	R/W	GPx.3FED : GPx.3 Falling Edge Detect bit 0 : Disable 1 : Enable	0
2	R/W	GPx.2FED : GPx.2 Falling Edge Detect bit 0 : Disable 1 : Enable	0
1	R/W	GPx.1FED : GPx.1 Falling Edge Detect bit 0 : Disable 1 : Enable	0
0	R/W	GPx.0FED : GPx.0 Falling Edge Detect bit 0 : Disable 1 : Enable	0

*** When both Rising Edge and Falling Edge are set, Edge detect mode becomes Any Edge mode.

7.4.14 Port Edge Detect Status Registers (GPxEDS)

Address: 0xFFFF_3028 / 0xFFFF_3068 / 0xFFFF_30A8 / 0xFFFF_30E8 / 0xFFFF_3128 / 0xFFFF_3168 / 0xFFFF_31A8 / 0xFFFF_31E8 / 0xFFFF_3228 / 0xFFFF_3268

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	R/W	GPx.7EDS : GPx.7 Edge Detect Status bit	0
6	R/W	GPx.6EDS : GPx.6 Edge Detect Status bit	0
5	R/W	GPx.5EDS : GPx.5 Edge Detect Status bit	0
4	R/W	GPx.4EDS : GPx.4 Edge Detect Status bit	0
3	R/W	GPx.3EDS : GPx.3 Edge Detect Status bit	0
2	R/W	GPx.2EDS : GPx.2 Edge Detect Status bit	0
1	R/W	GPx.1EDS : GPx.1 Edge Detect Status bit	0
0	R/W	GPx.0EDS : GPx.0 Edge Detect Status bit	0

*** Port Edge Detect Status bit
0 : No edge detect has occurred on port
1 : Edge detect has occurred on port

*** Status bits are cleared by writing a one to them.
*** Writing a zero to a status bit are no effect.

7.4.15 Port Open Drain Mode Control Registers (GPxODM)

Address: 0xFFFF_302C / 0xFFFF_306C / 0xFFFF_30AC / 0xFFFF_30EC / 0xFFFF_312C / 0xFFFF_316C / 0xFFFF_31AC / 0xFFFF_31EC / 0xFFFF_322C / 0xFFFF_326C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R	GPx.yOD : GPx.y Open Drain Mode Setting bit 0 : Normal 1 : Open Drain	0

7.4.16 Port Schmitt Input Enable Registers (GPxSHMT)

Address: 0xFFFF_3034 / 0xFFFF_3074 / 0xFFFF_30B4 / 0xFFFF_30F4 / 0xFFFF_3134 / 0xFFFF_3174/0xFFFF_3174~~(B4)~~*/0xFFFF_31F4 / 0xFFFF_3234 / 0xFFFF_3274

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	W	GPx.7SHMT : GPx.7 Schmitt input enable bit	0
6	W	GPx.6SHMT : GPx.6 Schmitt input enable bit	0
5	W	GPx.5SHMT : GPx.5 Schmitt input enable bit	0
4	W	GPx.4SHMT : GPx.4 Schmitt input enable bit	0
3	W	GPx.3SHMT : GPx.3 Schmitt input enable bit	0
2	W	GPx.2SHMT : GPx.2 Schmitt input enable bit	0
1	W	GPx.1SHMT : GPx.1 Schmitt input enable bit	0
0	W	GPx.0SHMT : GPx.0 Schmitt input enable bit	0

*** Port Schmitt input enable bit
0 : CMOS input mode
1 : Schmitt input mode
*GP6.x SHMT bits are configured by GP5.x SHMT register(0xFFFF_3174)

7.4.17 Port Pull-down Status Registers (GPxPDS)

Address: 0xFFFF_3030 / 0xFFFF_3070 / 0xFFFF_30B0 / 0xFFFF_30F0 / 0xFFFF_3130 / 0xFFFF_3170 / 0xFFFF_31B0 / 0xFFFF_31F0 / 0xFFFF_3230 / 0xFFFF_3270

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R	GPx.yDN : GPx.y Pull-down Status bit 0 : Pull-down Disable 1 : Pull-down Enable	0x0

7.4.18 Port Pull-down Enable Registers (GPxPDEN)

Address: 0xFFFF_3030 / 0xFFFF_3070 / 0xFFFF_30B0 / 0xFFFF_30F0 / 0xFFFF_3130 / 0xFFFF_3170 / 0xFFFF_31B0 / 0xFFFF_31F0 / 0xFFFF_3230 / 0xFFFF_3270

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	W	GPx.7PDEN : GPx.7 Pull-down enable bit	-
6	W	GPx.6PDEN : GPx.6 Pull-down enable bit	-
5	W	GPx.5PDEN : GPx.5 Pull-down enable bit	-
4	W	GPx.4PDEN : GPx.4 Pull-down enable bit	-
3	W	GPx.3PDEN : GPx.3 Pull-down enable bit	-
2	W	GPx.2PDEN : GPx.2 Pull-down enable bit	-
1	W	GPx.1PDEN : GPx.1 Pull-down enable bit	-
0	W	GPx.0PDEN : GPx.0 Pull-down enable bit	-

*** Port Pull-down enable bit
0 : No effect
1 : the pull down of corresponding bit is set to enable.

7.4.19 Port Pull-down Disable Registers (GPxPDDIS)

Address: 0xFFFF_301C / 0xFFFF_305C / 0xFFFF_309C / 0xFFFF_30DC / 0xFFFF_311C / 0xFFFF_315C / 0xFFFF_319C / 0xFFFF_31DC / 0xFFFF_321C / 0xFFFF_325C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	W	GPx.7PDDIS : GPx.7 Pull-down disable bit	-
6	W	GPx.6PDDIS : GPx.6 Pull-down disable bit	-
5	W	GPx.5PDDIS : GPx.5 Pull-down disable bit	-
4	W	GPx.4PDDIS : GPx.4 Pull-down disable bit	-
3	W	GPx.3PDDIS : GPx.3 Pull-down disable bit	-
2	W	GPx.2PDDIS : GPx.2 Pull-down disable bit	-
1	W	GPx.1PDDIS : GPx.1 Pull-down disable bit	-
0	W	GPx.0PDDIS : GPx.0 Pull-down disable bit	-

*** Port Pull-down disable bit
0 : No effect
1 : the pull down of corresponding bit is set to disable.

8 INTERRUPT CONTROLLER

adStar provides 46-channel interrupt input that consists of 44 interrupts from internal devices such as Timer, SPI, TWI, UART and 2-external interrupts.

8.1 Features

- 46 channel interrupts (2-external interrupts and 44-interal interrupts
- 5 operating configurations for external interrupts
- 2 operating configurations for internal interrupts
- Interrupt enable for each channel
- Interrupt masking for each channel
- Programmable interrupt priority

8.2 Function Description

Interrupt handling processes are following steps.

1. Each interrupts source requests to interrupt controller.
2. After choose the interrupt according to Interrupt Enable Register, the interrupt controller stores the interrupt of Interrupt Pending Register.
3. After decide interrupt priority, the interrupt controller request to CPU.
4. If the CPU receive an interrupt request, CPU's interrupt is disabled and reads interrupt vector address from interrupt vector table. After CPU reads the address, the CPU calls Interrupt Service Routine (ISR).
5. Executes ISR
6. After finish executing ISR, CPU removes Interrupt value in the Interrupt Pending Register by writing Vector value into Interrupt Pending Clear Register.
7. CPU's interrupt is enabled after finish (return) ISR routine.

Nested Interrupt handling processes are following steps.

1. Each interrupts source requests to interrupt controller.
2. After choose the interrupt according to Interrupt Enable Register, the interrupt controller stores the interrupt of Interrupt Pending Register.
3. After decide interrupt priority, the interrupt controller request to CPU.
4. If the CPU receive an interrupt request, CPU's interrupt is disabled and reads interrupt vector address from interrupt vector table. After CPU reads the address, the CPU calls Interrupt Service Routine (ISR).
5. In order to allow nested interrupt, CPU removes interrupt that is already stored into Interrupt Pending Register by writing correspond vector value to Interrupt Pending Clear Register. After that CPU's interrupt is enabled by asm("set 13") instruction.
6. Executes ISR.
7. If interrupt are occurred during ISR execution, CPU allows the interrupt and then execute the corresponding ISR.
8. After finish the new ISR execution, CPU returns the old ISR and then continues to execute.
9. Finish the ISR.

8.2.1 Interrupt Vector and Priority

EIRQ0 has the highest priority. The size of interrupt address is 4-byte because interrupt vector address is 32-bit addressing mode.

Table 8-1 Interrupt Vector & Priority

Vector No.	Description	Vector Address
0x53	Reserved	0x0000014C
0x52	Dedicated PWM Interrupt	0x00000148
0x51	QEI Interrupt	0x00000144
0x50	Reserved	0x00000140
0x4F	Fault B Interrupt	0x0000013C
0x4E	Fault A Interrupt	0x00000138
0x4D	Capture Overflow Interrupt	0x00000134
0x4C	SPI 1 Interrupt	0x00000130
0x4B	GPIO 9 Interrupt	0x0000012C
0x4A	TWI Interrupt	0x00000128
0x49	GPIO 8 Interrupt	0x00000124
0x48	Reserved	0x00000120
0x47	GPIO 7 Interrupt	0x0000011C
0x46	UART 4 (IrDA) Interrupt	0x00000118
0x45	GPIO 6 Interrupt	0x00000114
0x44	Watch dog Interrupt	0x00000110
0x43	GPIO 5 Interrupt	0x0000010C
0x42	ADC Interrupt	0x00000108
0x41	GPIO 4 Interrupt	0x00000104
0x40	Reserved	0x00000100
0x3F	DMA CH7 Interrupt	0x000000FC
0x3E	UART 3 Interrupt	0x000000F8
0x3D	GPIO 3 Interrupt	0x000000F4
0x3C	SDHC Interrupt	0x000000F0
0x3B	DMA CH6 Interrupt	0x000000EC
0x3A	NAND Flash Interrupt	0x000000E8
0x39	Timer 3 Interrupt	0x000000E4
0x38	Reserved	0x000000E0
0x37	DMA CH5 Interrupt	0x000000DC
0x36	UART 2 Interrupt	0x000000D8
0x35	GPIO 2 Interrupt	0x000000D4
0x34	USB Host Interrupt	0x000000D0
0x33	DMA CH4 Interrupt	0x000000CC
0x32	USB Device Interrupt	0x000000C8
0x31	Timer 2 Interrupt	0x000000C4
0x30	Reserved	0x000000C0
0x2F	DMA CH3 Interrupt	0x000000BC
0x2E	UART 1 Interrupt	0x000000B8
0x2D	GPIO 1 Interrupt	0x000000B4
0x2C	SPI 0 Interrupt	0x000000B0
0x2B	DMA CH2 Interrupt	0x000000AC
0x2A	PMU Interrupt	0x000000A8

0x29	Timer 1 Interrupt	0x000000A4
0x28	EIRQ1 Interrupt	0x000000A0
0x27	DMA CH1 Interrupt	0x0000009C
0x26	UART 0 Interrupt	0x00000098
0x25	GPIO 0 Interrupt	0x00000094
0x24	Frame Sync. Interrupt	0x00000090
0x23	DMA CH0 Interrupt	0x0000008C
0x22	Sound Mixer Interrupt	0x00000088
0x21	Timer 0 Interrupt	0x00000084
0x20	EIRQ0 Interrupt (Highest Priority)	0x00000080

8.2.2 External Interrupt (EIRQx)

External Interrupt receives 5 types of external interrupt by configuring EINTMOD register.

- In the Low Level Mode, Interrupt is occurred every system cycle during External Interrupt signal keeps “Low“.
- In the High Level Mode, Interrupt is occurred every system cycle during External Interrupt signal keeps “High“.
- In the Falling Edge Mode, Interrupt is occurred when External Interrupt signal changes “High“ to “Low“.
- In the Rising Edge Mode, Interrupt is occurred when External Interrupt signal changes “Low“ to “High“
- In the Any Edge Mode, Interrupt is occurred when External Interrupt signal changes “Low“ to “High“ or “High“ to “Low“.

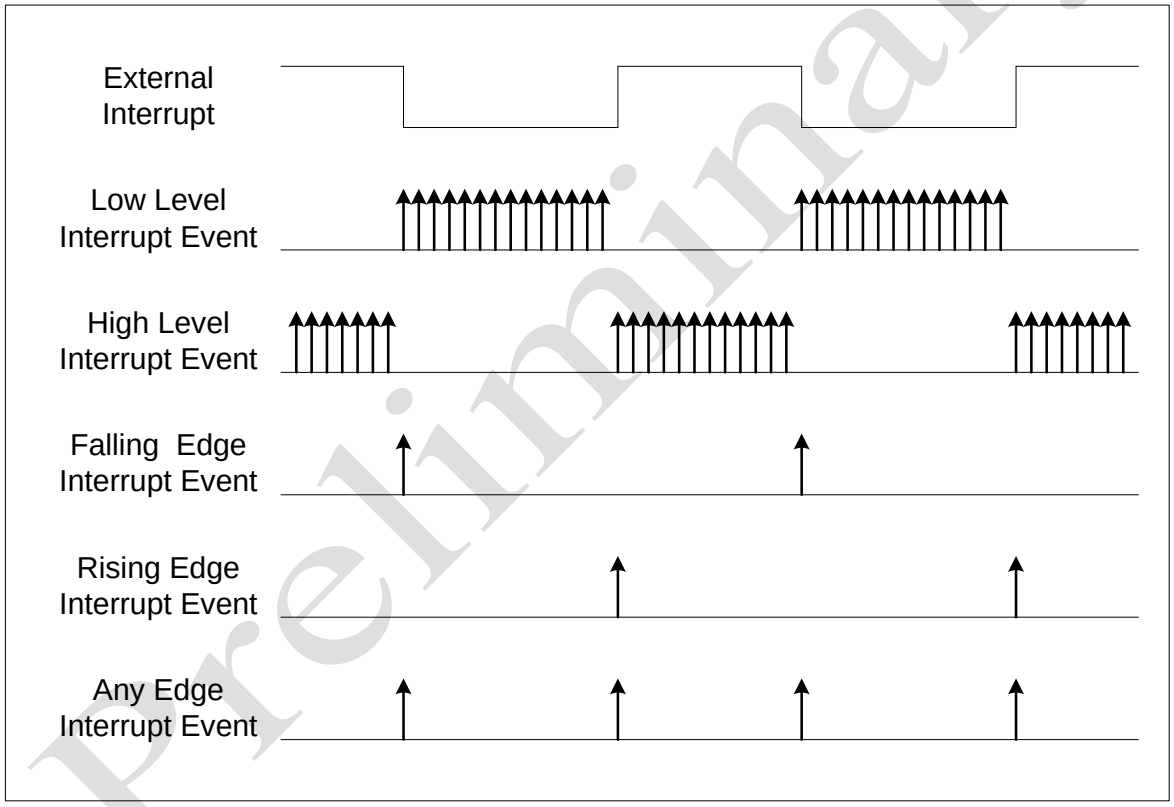


Figure 8-1 External Interrupt Mode

8.2.3 Internal Interrupt Mode

All of the internal interrupts are executed in “Rising Edge Mode”. However, if user wants to “High Level” interrupt handling, user can configures Internal Interrupt Mode Register.

8.2.4 Interrupt Pending and Interrupt Pending Clear

User can check interrupt status via Interrupt Pending Registers. An interrupt is stored into Interrupt Pending Register until be cleared by Interrupt Pending Clear Register. Also, if higher priority interrupt is stored in the Interrupt Pending Registers without Masking, the currently occurred interrupt is waiting for all of the higher priority interrupts are cleared.

In order to clear the interrupts that are stored in Interrupt Pending Registers, user should write the corresponding vector number into Interrupt Pending Clear Register.

8.2.5 Interrupt Enable

An interrupt, which is masked by Interrupt Mask Registers, is stored in Interrupt Pending Registers. However, an interrupt, which is disabled by Interrupt Enable Registers (IENR), is not stored in the Interrupt Pending Registers. Therefore, user can disable an interrupt that not allowed by using the registers (IENR).

8.2.6 Interrupt Mask Set/Clear Register

If the register is set, an interrupt request is enabled, otherwise disabled..

CPU executes corresponding interrupt request by Interrupt Mask Registers. If the Interrupt Mask Set bit is 1, the interrupt controller requests the interrupt service to CPU. However, if the Interrupt Mask Clear bit is 1, the interrupt controller does not request the interrupt service to CPU.

Although, the Mask bit is 0, because an interrupt is stored into Interrupt Pending Registers (IPR), if user sets the Mask bit to 1, the interrupt controller requests interrupt service stored in Interrupt Pending Registers in the order of priority.

8.3 Register Description

8.3.1 Interrupt Pending Clear Register (INTPENDCLR)

Address : 0xFFFF_0000

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	W	Interrupt Pending Register Clear Value (0x20 ~ 0x52)	0xFF

*** In order to clear Interrupt Pending Register, user should clear according to the Interrupt Vector No. (Refer to Interrupt Vector No.)

8.3.2 External Interrupt Mode and External PIN Level Register (EINTMOD)

Address : 0xFFFF_0004

Bit	R/W	Description	Default Value
31:8	R	Reserved	-
7	R	EIRQ1ST : EIRQ1 PIN Level	-
6 : 4	R/W	EIRQ1MOD : EIRQ1 Active State 000 : Low Level 001 : High Level 010 : Falling Edge 011 : Rising Edge 1xx : Any Edge	010
3	R	EIRQ0ST : EIRQ0 PIN Level	-
2 : 0	R/W	EIRQ0MOD : EIRQ0 Active State 000 : Low Level 001 : High Level 010 : Falling Edge 011 : Rising Edge 1xx : Any Edge	010

8.3.3 Internal Interrupt Mode Register (IINTMODn)

Address : 0xFFFF_0008 / 0xFFFF_0048

Bit	R/W	Description	Default Value
31	R/W	Vector No. 0x3F / 0x5F Interrupt Mode bit	0
30	R/W	Vector No. 0x3E / 0x5E Interrupt Mode bit	0
29	R/W	Vector No. 0x3D / 0x5D Interrupt Mode bit	0
28	R/W	Vector No. 0x3C / 0x5C Interrupt Mode bit	-
27	R/W	Vector No. 0x3B / 0x5B Interrupt Mode bit	0
26	R/W	Vector No. 0x3A / 0x5A Interrupt Mode bit	0
25	R/W	Vector No. 0x39 / 0x59 Interrupt Mode bit	0
24	-	Reserved	-
23	R/W	Vector No. 0x37 / 0x57 Interrupt Mode bit	0
22	R/W	Vector No. 0x36 / 0x56 Interrupt Mode bit	0
21	R/W	Vector No. 0x35 / 0x55 Interrupt Mode bit	0
20	R/W	Vector No. 0x36 / 0x54 Interrupt Mode bit	-
19	R/W	Vector No. 0x33 / 0x53 Interrupt Mode bit	0
18	R/W	Vector No. 0x32 / 0x52 Interrupt Mode bit	0
17	R/W	Vector No. 0x31 / 0x51 Interrupt Mode bit	0
16	-	Reserved	-
15	R/W	Vector No. 0x2F / 0x4F Interrupt Mode bit	0
14	R/W	Vector No. 0x2E / 0x4E Interrupt Mode bit	0
13	R/W	Vector No. 0x2D / 0x4D Interrupt Mode bit	0
12	R/W	Vector No. 0x2C / 0x4C Interrupt Mode bit	-
11	R/W	Vector No. 0x2B / 0x4B Interrupt Mode bit	0
10	R/W	Vector No. 0x2A / 0x4A Interrupt Mode bit	0
9	R/W	Vector No. 0x29 / 0x49 Interrupt Mode bit	0
8	-	Reserved	-
7	R/W	Vector No. 0x27 / 0x47 Interrupt Mode bit	0
6	R/W	Vector No. 0x26 / 0x46 Interrupt Mode bit	0
5	R/W	Vector No. 0x25 / 0x45 Interrupt Mode bit	0
4	R/W	Vector No. 0x24 / 0x44 Interrupt Mode bit	-
3	R/W	Vector No. 0x23 / 0x43 Interrupt Mode bit	0
2	R/W	Vector No. 0x22 / 0x42 Interrupt Mode bit	0
1	R/W	Vector No. 0x21 / 0x41 Interrupt Mode bit	0
0	-	Reserved	-

*** Internal Interrupt Mode bit

0 : High Level Mode

1 : Rising Edge Mode

8.3.4 Interrupt Pending Register (INTPENDn)

Address : 0xFFFF_000C / 0xFFFF_004C

Bit	R/W	Description	Default Value
31	R	Vector No. 0x3F / 0x5F Interrupt Pending bit	-
30	R	Vector No. 0x3E / 0x5E Interrupt Pending bit	-
29	R	Vector No. 0x3D / 0x5D Interrupt Pending bit	-
28	R	Vector No. 0x3C / 0x5C Interrupt Pending bit	-
27	R	Vector No. 0x3B / 0x5B Interrupt Pending bit	-
26	R	Vector No. 0x3A / 0x5A Interrupt Pending bit	-
25	R	Vector No. 0x39 / 0x59 Interrupt Pending bit	-
24	R	Vector No. 0x38 / 0x58 Interrupt Pending bit	-
23	R	Vector No. 0x37 / 0x57 Interrupt Pending bit	-
22	R	Vector No. 0x36 / 0x56 Interrupt Pending bit	-
21	R	Vector No. 0x35 / 0x55 Interrupt Pending bit	-
20	R	Vector No. 0x34 / 0x54 Interrupt Pending bit	-
19	R	Vector No. 0x33 / 0x53 Interrupt Pending bit	-
18	R	Vector No. 0x32 / 0x52 Interrupt Pending bit	-
17	R	Vector No. 0x31 / 0x51 Interrupt Pending bit	-
16	R	Vector No. 0x30 / 0x50 Interrupt Pending bit	-
15	R	Vector No. 0x2F / 0x4F Interrupt Pending bit	-
14	R	Vector No. 0x2E / 0x4E Interrupt Pending bit	-
13	R	Vector No. 0x2D / 0x4D Interrupt Pending bit	-
12	R	Vector No. 0x2C / 0x4C Interrupt Pending bit	-
11	R	Vector No. 0x2B / 0x4B Interrupt Pending bit	-
10	R	Vector No. 0x2A / 0x4A Interrupt Pending bit	-
9	R	Vector No. 0x29 / 0x49 Interrupt Pending bit	-
8	R	Vector No. 0x28 / 0x48 Interrupt Pending bit	-
7	R	Vector No. 0x27 / 0x47 Interrupt Pending bit	-
6	R	Vector No. 0x26 / 0x46 Interrupt Pending bit	-
5	R	Vector No. 0x25 / 0x45 Interrupt Pending bit	-
4	R	Vector No. 0x24 / 0x44 Interrupt Pending bit	-
3	R	Vector No. 0x23 / 0x43 Interrupt Pending bit	-
2	R	Vector No. 0x22 / 0x42 Interrupt Pending bit	-
1	R	Vector No. 0x21 / 0x41 Interrupt Pending bit	-
0	R	Vector No. 0x20 / 0x40 Interrupt Pending bit	-

*** Each bit of Interrupt Pending Register indicates the corresponding interrupt is occurred. The value of the Interrupt Pending Register is cleared by Interrupt Pending Clear Register. Generally, the interrupt is cleared when the interrupt request is finished.

8.3.5 Interrupt Enable Register (INTENn)

Address : 0xFFFF_0010 / 0xFFFF_0050

Bit	R/W	Description	Default Value
31	R/W	Vector No. 0x3F / 0x5F Interrupt Enable bit	0
30	R/W	Vector No. 0x3E / 0x5E Interrupt Enable bit	0
29	R/W	Vector No. 0x3D / 0x5D Interrupt Enable bit	0
28	R/W	Vector No. 0x3C / 0x5C Interrupt Enable bit	0
27	R/W	Vector No. 0x3B / 0x5B Interrupt Enable bit	0
26	R/W	Vector No. 0x3A / 0x5A Interrupt Enable bit	0
25	R/W	Vector No. 0x39 / 0x59 Interrupt Enable bit	0
24	R/W	Vector No. 0x38 / 0x58 Interrupt Enable bit	0
23	R/W	Vector No. 0x37 / 0x57 Interrupt Enable bit	0
22	R/W	Vector No. 0x36 / 0x56 Interrupt Enable bit	0
21	R/W	Vector No. 0x35 / 0x55 Interrupt Enable bit	0
20	R/W	Vector No. 0x34 / 0x54 Interrupt Enable bit	0
19	R/W	Vector No. 0x33 / 0x53 Interrupt Enable bit	0
18	R/W	Vector No. 0x32 / 0x52 Interrupt Enable bit	0
17	R/W	Vector No. 0x31 / 0x51 Interrupt Enable bit	0
16	R/W	Vector No. 0x30 / 0x50 Interrupt Enable bit	0
15	R/W	Vector No. 0x2F / 0x4F Interrupt Enable bit	0
14	R/W	Vector No. 0x2E / 0x4E Interrupt Enable bit	0
13	R/W	Vector No. 0x2D / 0x4D Interrupt Enable bit	0
12	R/W	Vector No. 0x2C / 0x4C Interrupt Enable bit	0
11	R/W	Vector No. 0x2B / 0x4B Interrupt Enable bit	0
10	R/W	Vector No. 0x2A / 0x4A Interrupt Enable bit	0
9	R/W	Vector No. 0x29 / 0x49 Interrupt Enable bit	0
8	R/W	Vector No. 0x28 / 0x48 Interrupt Enable bit	0
7	R/W	Vector No. 0x27 / 0x47 Interrupt Enable bit	0
6	R/W	Vector No. 0x26 / 0x46 Interrupt Enable bit	0
5	R/W	Vector No. 0x25 / 0x45 Interrupt Enable bit	0
4	R/W	Vector No. 0x24 / 0x44 Interrupt Enable bit	0
3	R/W	Vector No. 0x23 / 0x43 Interrupt Enable bit	0
2	R/W	Vector No. 0x22 / 0x42 Interrupt Enable bit	0
1	R/W	Vector No. 0x21 / 0x41 Interrupt Enable bit	0
0	R/W	Vector No. 0x20 / 0x40 Interrupt Enable bit	0

*** Interrupt Enable bit

0 : Interrupt Disable and Pending Clear

1 : Interrupt Enable

8.3.6 Interrupt Mask Status Register (INTMASKn)

Address : 0xFFFF_0014 / 0xFFFF_0054

Bit	R/W	Description	Default Value
31 : 0	R	Interrupt Mask Status Register	0x0000_0000

*** Can check all of the Mask bit status.

8.3.7 Interrupt Mask Set Register (INTMASKSETn)

Address : 0xFFFF_0014h / 0xFFFF_0054

Bit	R/W	Description	Default Value
31	W	Vector No. 0x3F / 0x5F Interrupt Request Set bit	0
30	W	Vector No. 0x3E / 0x5E Interrupt Request Set bit	0
29	W	Vector No. 0x3D / 0x5D Interrupt Request Set bit	0
28	W	Vector No. 0x3C / 0x5C Interrupt Request Set bit	0
27	W	Vector No. 0x3B / 0x5B Interrupt Request Set bit	0
26	W	Vector No. 0x3A / 0x5A Interrupt Request Set bit	0
25	W	Vector No. 0x39 / 0x59 Interrupt Request Set bit	0
24	W	Vector No. 0x38 / 0x58 Interrupt Request Set bit	0
23	W	Vector No. 0x37 / 0x58 Interrupt Request Set bit	0
22	W	Vector No. 0x36 / 0x56 Interrupt Request Set bit	0
21	W	Vector No. 0x35 / 0x55 Interrupt Request Set bit	0
20	W	Vector No. 0x34 / 0x54 Interrupt Request Set bit	0
19	W	Vector No. 0x33 / 0x53 Interrupt Request Set bit	0
18	W	Vector No. 0x32 / 0x52 Interrupt Request Set bit	0
17	W	Vector No. 0x31 / 0x51 Interrupt Request Set bit	0
16	W	Vector No. 0x30 / 0x50 Interrupt Request Set bit	0
15	W	Vector No. 0x2F / 0x4F Interrupt Request Set bit	0
14	W	Vector No. 0x2E / 0x4E Interrupt Request Set bit	0
13	W	Vector No. 0x2D / 0x4D Interrupt Request Set bit	0
12	W	Vector No. 0x2C / 0x4C Interrupt Request Set bit	0
11	W	Vector No. 0x2B / 0x4B Interrupt Request Set bit	0
10	W	Vector No. 0x2A / 0x4A Interrupt Request Set bit	0
9	W	Vector No. 0x29 / 0x49 Interrupt Request Set bit	0
8	W	Vector No. 0x28 / 0x48 Interrupt Request Set bit	0
7	W	Vector No. 0x27 / 0x47 Interrupt Request Set bit	0
6	W	Vector No. 0x26 / 0x46 Interrupt Request Set bit	0
5	W	Vector No. 0x25 / 0x45 Interrupt Request Set bit	0
4	W	Vector No. 0x24 / 0x44 Interrupt Request Set bit	0
3	W	Vector No. 0x23 / 0x43 Interrupt Request Set bit	0
2	W	Vector No. 0x22 / 0x42 Interrupt Request Set bit	0
1	W	Vector No. 0x21 / 0x41 Interrupt Request Set bit	0
0	W	Vector No. 0x20 / 0x40 Interrupt Request Set bit	0

*** Interrupt Request Set bit

0 : No Effect interrupt Mask.

1 : Pending interrupt is allowed to become active (interrupts sent to CPU).

8.3.8 Interrupt Mask Clear Register (INTMASKCLRn)

Address : 0xFFFF_0018 / 0xFFFF_0058

Bit	R/W	Description	Default Value
31	W	Vector No. 0x3F / 0x5F Interrupt Req. Clear bit	0
30	W	Vector No. 0x3E / 0x5E Interrupt Req. Clear bit	0
29	W	Vector No. 0x3D / 0x5D Interrupt Req. Clear bit	0
28	W	Vector No. 0x3C / 0x5C Interrupt Req. Clear bit	0
27	W	Vector No. 0x3B / 0x5B Interrupt Req. Clear bit	0
26	W	Vector No. 0x3A / 0x5A Interrupt Req. Clear bit	0
25	W	Vector No. 0x39 / 0x59 Interrupt Req. Clear bit	0
24	W	Vector No. 0x38 / 0x58 Interrupt Req. Clear bit	0
23	W	Vector No. 0x37 / 0x57 Interrupt Req. Clear bit	0
22	W	Vector No. 0x36 / 0x56 Interrupt Req. Clear bit	0
21	W	Vector No. 0x35 / 0x55 Interrupt Req. Clear bit	0
20	W	Vector No. 0x34 / 0x54 Interrupt Req. Clear bit	0
19	W	Vector No. 0x33 / 0x53 Interrupt Req. Clear bit	0
18	W	Vector No. 0x32 / 0x52 Interrupt Req. Clear bit	0
17	W	Vector No. 0x31 / 0x51 Interrupt Req. Clear bit	0
16	W	Vector No. 0x30 / 0x50 Interrupt Req. Clear bit	0
15	W	Vector No. 0x2F / 0x4F Interrupt Req. Clear bit	0
14	W	Vector No. 0x2E / 0x4E Interrupt Req. Clear bit	0
13	W	Vector No. 0x2D / 0x4D Interrupt Req. Clear bit	0
12	W	Vector No. 0x2C / 0x4C Interrupt Req. Clear bit	0
11	W	Vector No. 0x2B / 0x4B Interrupt Req. Clear bit	0
10	W	Vector No. 0x2A / 0x4A Interrupt Req. Clear bit	0
9	W	Vector No. 0x29 / 0x49 Interrupt Req. Clear bit	0
8	W	Vector No. 0x28 / 0x48 Interrupt Req. Clear bit	0
7	W	Vector No. 0x27 / 0x47 Interrupt Req. Clear bit	0
6	W	Vector No. 0x26 / 0x46 Interrupt Req. Clear bit	0
5	W	Vector No. 0x25 / 0x45 Interrupt Req. Clear bit	0
4	W	Vector No. 0x24 / 0x44 Interrupt Req. Clear bit	0
3	W	Vector No. 0x23 / 0x43 Interrupt Req. Clear bit	0
2	W	Vector No. 0x22 / 0x42 Interrupt Req. Clear bit	0
1	W	Vector No. 0x21 / 0x41 Interrupt Req. Clear bit	0
0	W	Vector No. 0x20 / 0x40 Interrupt Req. Clear bit	0

*** Interrupt Request Clear bit

0 : No Effect Interrupt Mask.

1 : Pending interrupt is masked from becoming active (interrupts not sent to CPU).

8.3.9 Programmable Interrupt Priority Enable Register (PIPENR)

Address : 0xFFFF_001C

Bit	R/W	Description	Default Value
31 : 1	R	Reserved	-
0	R/W	Programmable Priority Enable bit 0 : Programmable Priority Disable 1 : Programmable Priority Enable	0

8.3.10 Interrupt Priority Vector n Register (IPVRn)

Address : 0xFFFF_0020 / 0xFFFF_0024 / 0xFFFF_0028 / 0xFFFF_002C /
0xFFFF_0030 / 0xFFFF_0034 / 0xFFFF_0038 / 0xFFFF_003C

Bit	R/W	Description	Default Value
31 : 28	R/W	8th Priority Interrupt Number	0x07
27 : 24	R/W	7th Priority Interrupt Number	0x06
23 : 20	R/W	6th Priority Interrupt Number	0x05
19 : 16	R/W	5th Priority Interrupt Number	0x04
15 : 12	R/W	4th Priority Interrupt Number	0x03
11 : 8	R/W	3rd Priority Interrupt Number	0x02
7 : 4	R/W	2nd Priority Interrupt Number	0x01
3 : 0	RW	1st Priority Interrupt Number	0x00

The priority of interrupts can be changed in a group that includes 8-interrupt.

9 DMA

9.1 Features

- Compatibility with AMBA AHB Specification

- Provides 8 channels. Each channels supports DMA.

- 16-port DMA Request.
DMAC provides 16-port DMA Request signal for Peripherals.

- Provides Single Request and Burst Request.
DMA request that provides to peripherals supports both Single Request and Burst Request.

- 4 types of DMA communication
DMA provides memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral communications.

- Provides Scatter and Gather by using Auto Reload functionality.

- Provides Scatter and Gather by using Linked list

- Priority of the DMA channel is fixed by hardware. Channel 0 has the highest priority and channel 7 has the lowest priority.

- Provides Multi-Layer AHB Bus by embedding 2 AHB Master.

- Provides Programmable Burst Size. In order to achieve higher efficiency of DAM transmit, user can configure Burst Size. The Burst Size is generally configured as half size of that of FIFO which is embedded in Peripheral.

- Each channel has 4 Word FIFO.

- Each channel has separated DMA Error Interrupt and DMA Terminal Count Interrupt.

- Supports Interrupt Enable.
DMA has an enable bit for both DMA Error Interrupt and DMA Terminal Count Interrupt.

9.2 Block Description

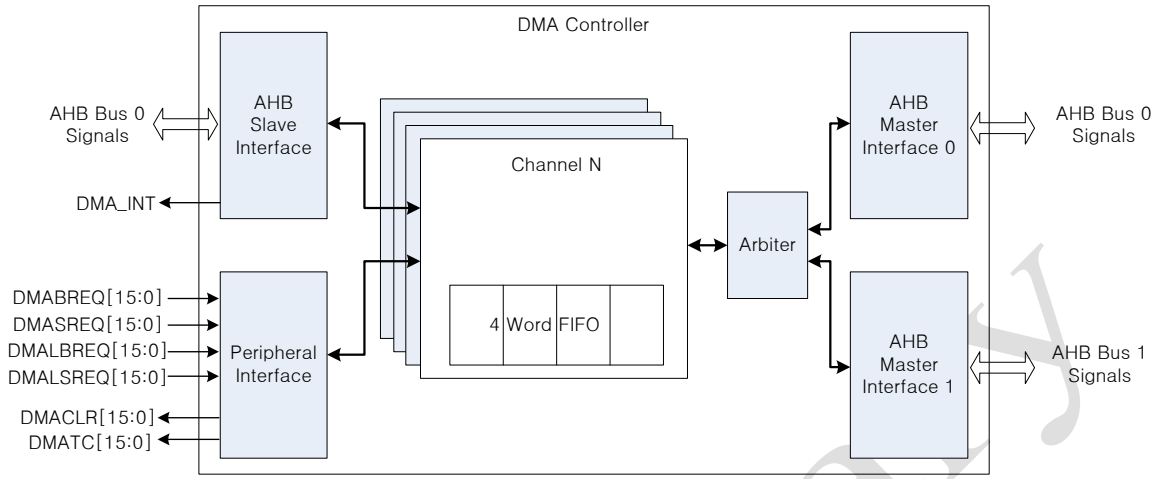


Figure 9-1 DMA Block Diagram

DMA has 8-channel. Each channel controls data flow that one-direction transfers from Source Peripheral to Destination Peripheral and contains 4x4 byte FIFO.

AHB Master Interface is responsible for data transmit from/to AHB Bus after receive data transfer requests from each channel. Inside the DMA Controller, because there are 2 AHB Master Interface, the DMA Controller can connect to other bus interface. Due to that reason, in spite of both Source Peripheral and Destination Peripheral connect to other bus, they can transfer data.

The Arbiter transmits data to AHB Master Interface0 or AHB Master Interface1 according to priority of data transfer request. It is determined by data address which AHB Master Interface should be use.

AHB Slave Interface is responsible for configures registers of each channel and requests interrupt.

Peripheral Interface receives DMA Request signal from Peripherals and send a signal to the corresponding channel according to Peripheral Selection bit. The Peripheral Interface can receive maximum 16 DMA Request signals. The channel can receive 2 DMA request signals Source DMA Request signal and Destination DMA Request signal.

9.3 Function Description

9.3.1 DMA Operation

- **Transfer Hierarchy**

DMA transfer has 3-layer hierarchy as figure 9-2.

The highest layer is called DMA Transfer. DMA Transfer indicates total size of data that is transferred by DMA. The size of transmit is determined by Transfer size of Control register.

The second layer is called Burst Transaction. Amount of data that is transferred from Burst Transaction is determined by Burst Size of Control register. Generally, the size is set to FIFO size of peripherals. Because the peripherals cannot transfer all of data at one time, the peripherals separates data in the unit of FIFO size and sends it.

** The burst size of control register is not AMBA Burst Transfer's burst size.

The lowest layer is called AMBA Burst Transfer. The Burst Transaction is divided into AMBA Burst Transfer unit. In this layer, data transfer is controller by hardware not user.

User can configure smaller Transfer Size than Burst Size. In that case, the Burst Transaction sends data with configured Transfer size.

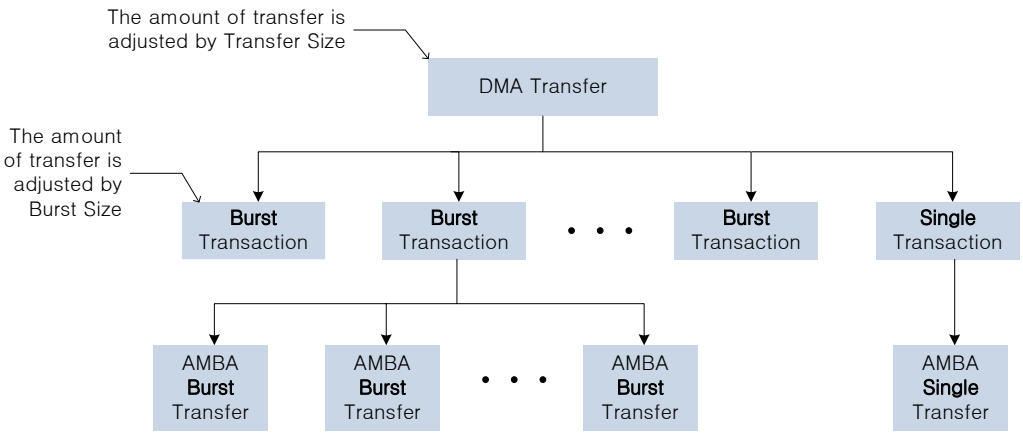


Figure 9-2 DMA Transfer hierarchy

- **Transfer type**

User should specify that Transfer type in DMA configuration. The transfer type is one of following 4 types.

1. Memory to Memory
2. Memory to Peripheral
3. Peripheral to Memory
4. Source Peripheral to Destination Peripheral

Memory to Memory type indicates that a source address is Memory and also a destination address is memory.
Memory to Peripheral type indicates that a source address is Memory and Destination address is Peripheral. In order words, with this type, DMA transfers data from Memory to Peripheral buffer.

The reason that user should specify the Transfer type is informing to DMA that whether handshake process is necessary or not. DMA uses handshake method when transfers data between peripherals not memory. To transfer data between peripherals not memory, the peripherals needs preparation and time. Also, the size of transmit is limited. With the handshake method, DMA Controller transfers data only when the data is ready. However, in the case of the peripheral is memory, it is not necessary that handsake process, because Memory can be accessed anytime. Therefore, user should specify the transfer type and inform to DMA Controller that data transmit is handshake method or not.

- **Flow Controller**

Flow Controller is a module that determines DMA Transfer size. Flow Controller is DMA Controller or one of Peripherals. If DMA Controller is Flow Controller, then the DMA data transfer size is determined as configured Transfer Size.
Also, a peripheral can be Flow Controller. In this case, DMA Controller transfers data according to request signal of Peripheral and ignores configured Transfer size. In order to finish DMA Transmit, when Flow Controller requires the last data, DMA Controller sends Last Request. Once the DMA Controller receives Last Request, the DAM transmit is finished after sending the last data.

9.3.2 Linked List Operation

- LLI

LLI (Linked List Item) is a data structure that contains basic information to DMA transmits. The contents of LLI are Source Address, Destination Address, Next LLI Address, and Control information. Linked List Operation is that reading first LLI and updates internal registers. After that, the operation does DMA Transfer. When the DMA transfer is finished, the operation reads the next LLI according to the next LLI address. Following figure 9-3 depicts LLI structure

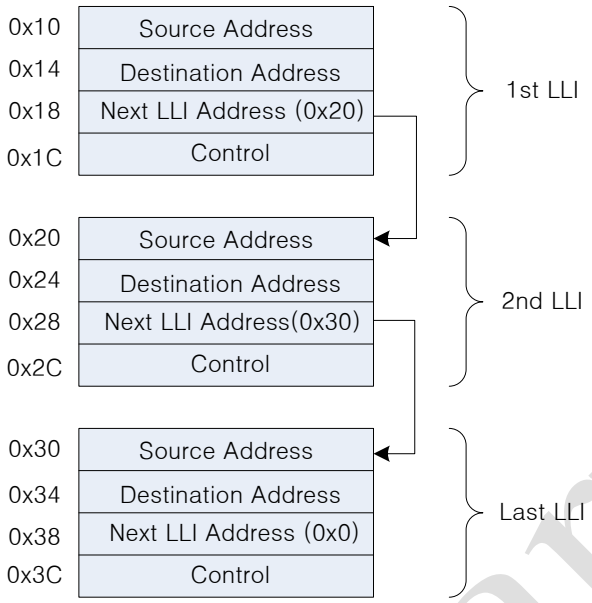


Figure 9-3 Linked list

The next LLI address of the last LLI is reserved as 0. If DMA Controller confirms the Next LLI address is 0, the DMAC can know the LLI is the last. Therefore, if an address of LLI is 0, the LLI operation cannot be executed.

- **Multi Block Transfer**

Transfers data that is described as LLI structure is called Multi Block Transfer. In order words, LLI data is defined as Block. The number of LLI refers to the number of Block. Also, the size of Block is defined as Control register's Transfer Size. The following figure 9-4 shows hierarchical view of Multi Block Transfer.

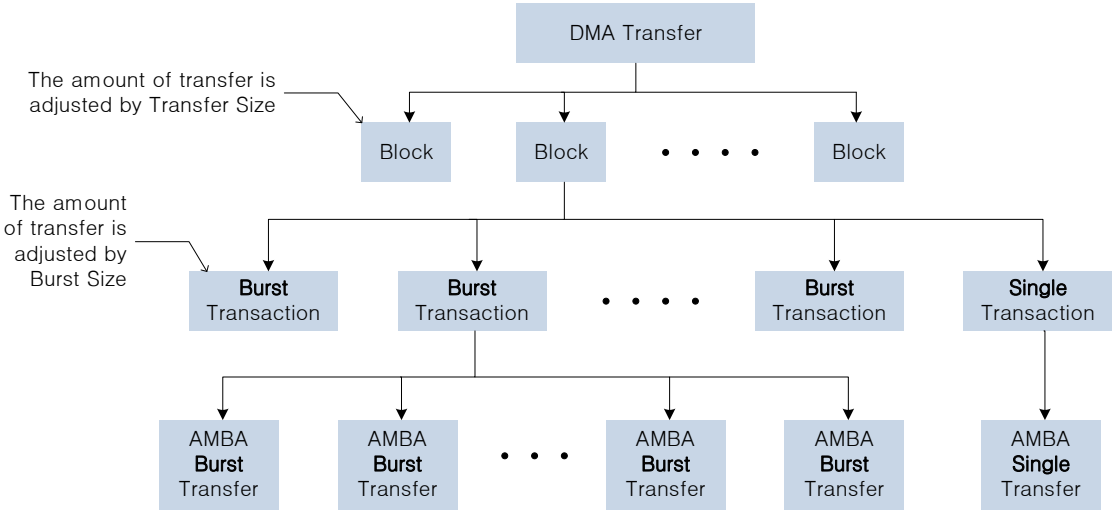


Figure 9-4 Multi Block Transfer

- **Scatter & Gather with Liked list**

Scatter indicates spread data by DMA Transfer and Gather indicates that putting

together the separated data. User can the Scatter and Gather operations by using LLI.

The following figure 9-5 shows an example for Gather operation by using LLI. In the figure, data is depicted as rectangle and the data is copied into peripheral.

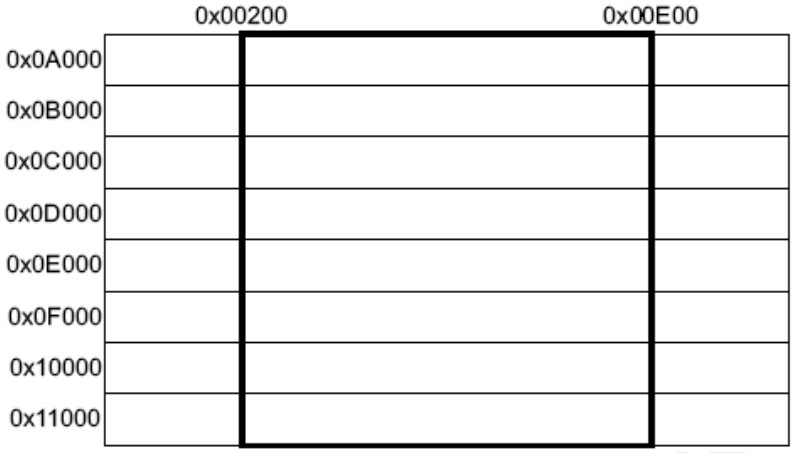


Figure 9-5 Gathering by using LLI

LLI starts from address 0x20000

The contents of the first LLI
- Source Address: 0x0A200
- Destination Address: Peripheral Address
- Source and Destination transfer width: 8bit
- Source and Destination burst Size: 16 burst
- Transfer Size: 3072 byte, 0xC00
- Next LLI Address: 0x20010

The contents of the second LLI
- Source Address: 0x0B200
- Destination Address: Peripheral Address
- Source and Destination transfer width: 8bit
- Source and Destination burst Size: 16 burst
- Transfer Size: 3072 byte, 0xC00
- Next LLI Address: 0x20020

The Contents of the last LLI
- Source Address: 0x11200
- Destination Address: Peripheral Address
- Source and Destination transfer width: 8bit
- Source and Destination burst Size: 16 burst
- Transfer Size: 3072 byte, 0xC00
- Next LLI Address: 0x0

9.3.3 Auto Reload Operation

The basic operation of Auto Reload Operation is when DMA Transfer is finished; reload Control register value to repeat DMA Transfer. The number of repeat count is determined by Auto Reload Count Register. The value of Auto Reload Count decreases by 1 when Auto Reload is occurred. If the value is 0, the Auto Reload Operation is stopped. The Auto Reload Operation is not necessary to mode configuration additionally. When finish DMA Transfer, if the value of Auto Reload Count Register is not 0, the Auto Reload Operation does not operate.

- **Transfer Hierarchy**

Auto Reload Operation is categorized in Multi Block Transfer like as Linked List Operation. The number of Block is Auto Reload Count + 1, and the size of data transferred is set to Transfer Size.

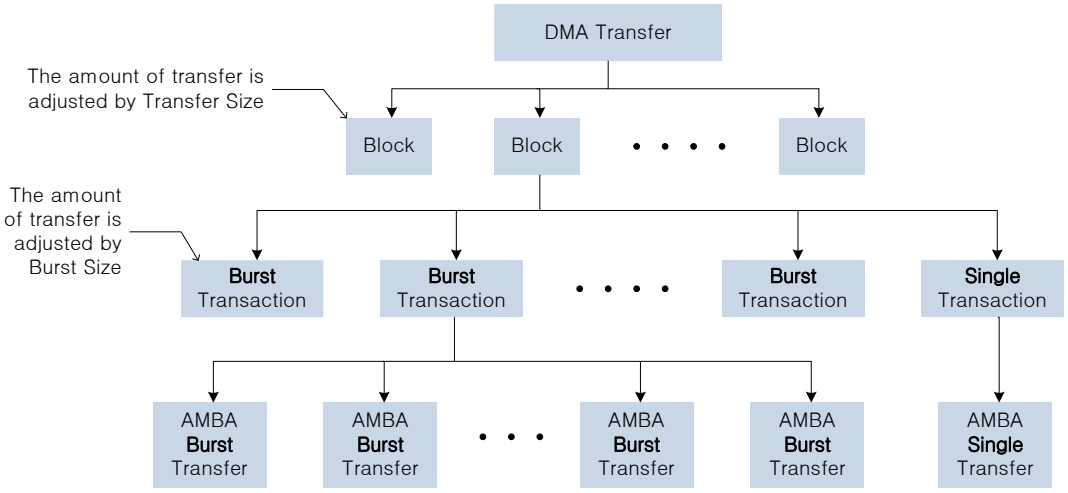


Figure 9-6 Auto Reload Operation Transfer Hierarchy

- **Scatter with Auto reload**

The following figure 9-7 shows an example for Scatter with Auto Reload Operation. Whenever finishing Block data transfer, Destination Scatter Address indicates uniform size of space between Destination Blocks' start address. User can separate between Blocks and can implement Scatter operation by using the Destination Block Address Register.

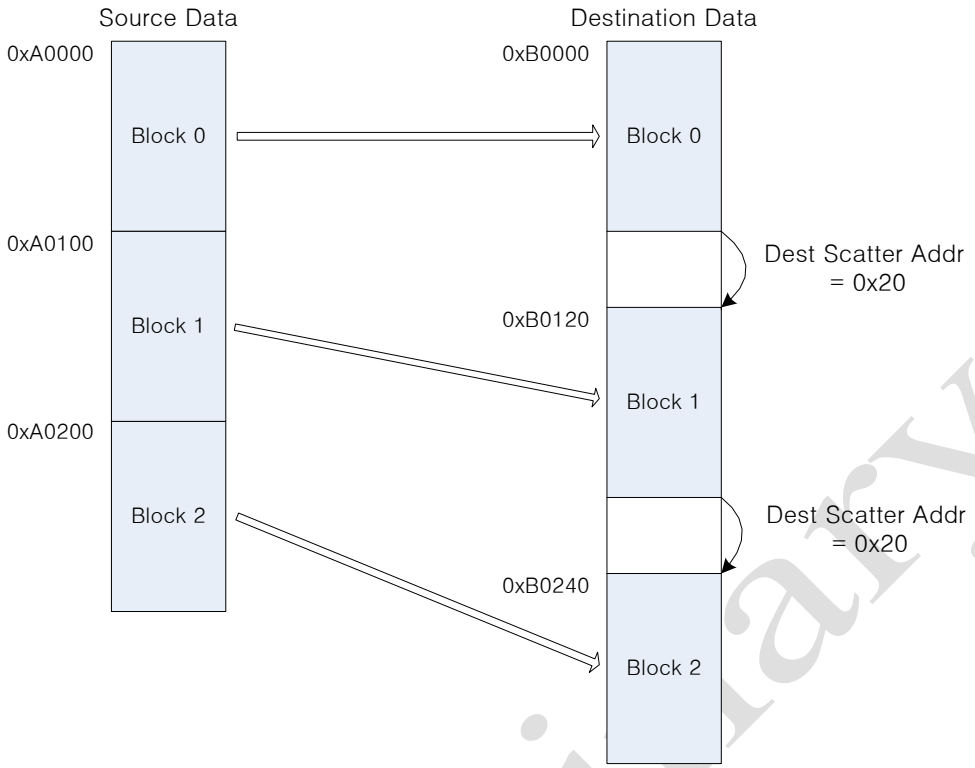


Figure 9-7 Scatter with Auto Reload Operation

Register Configuration

Source Address: 0xA0000
Destination Address: 0xB0000
Source and Destination transfer width: 32bit
Source and Destination burst Size: 4 burst
Transfer Size: 0x40
Auto Reload Count: 2
Destination scatter Address: 0x20

- Gather with Auto reload

The following figure 9-8 shows an example for Gather with Auto Reload Operation. Whenever finishing Block data transfer, Source Gather Address indicates uniform size of space between Source Blocks' start address. User can separate between Blocks and can implement Gather operation by using the Source Block Address Register.

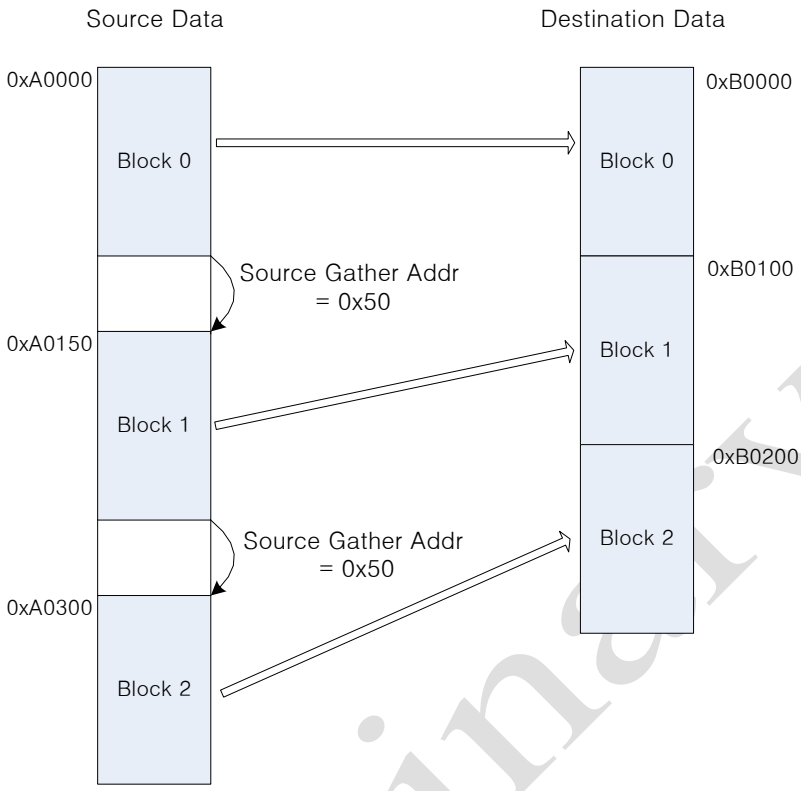


Figure 9-8 Gather with Auto Reload Operation

Register Configuration

Source Address: 0xA0000
Destination Address: 0xB0000
Source and Destination transfer width: 32bit
Source and Destination burst Size: 4 burst
Transfer Size: 0x40
Auto Reload Count: 2
Source gather Address: 0x50

9.3.4 Peripheral Interface

- ***Hand Shake Signals***

DMA Request signal and DMA Clear signal is used for Handshake DMA data transfer between Peripherals not memory.

Four DMA Request signals are used when peripheral requests data transfer to DMA Controller (Refer to Figure 9-9). Peripheral selects one signal of the 4, and requests. It is not allow to select multiple signal at the same time.

DMA Clear signal is a response of DMA Request. DMA Controller sends the signal to Peripheral.

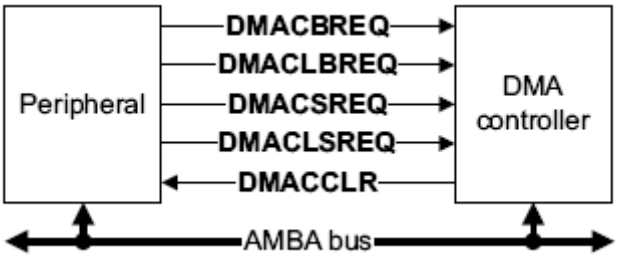


Figure 9-9 DMA Handshake Signals

- DMABREQ
  Burst Request signal. If the signal is activated, DMA Data Transfer becomes Burst Transaction by DMA Controller and the size of data is determined by Burst Size.

- DMASREQ
  Single Request signal. If the signal is activated, DMA Data Transfer becomes Single Transaction.

- DMALBREQ
  Last Burst Request. When peripheral is Flow Controller, this signal is used for informing that data is the last DMA Burst Request. If DMALBREQ is activated, the last Burst Transaction is operated and DMA Transfer is finished.

- DMALSREQ
  Last Single Request. When peripheral is Flow Controller, this signal is used for informing that data is the last DMA Single Request. If DMALBREQ is activated, the last Single Transaction is operated and DMA Transfer is finished.

- DMACLR
  DMA Clear signal. With this signal, all of the Requests from peripheral are inactivated.

- **Time diagram of DMA Request**

If peripheral send request to DMA Controller, the DMA Controller programed transfer data amount of Burst Size, and then send DMA Clear signal. At that time, when all of data transfer is finished, DMATC (DMA Terminal Count) signal is activated. With the signal, peripheral can check whether the DMA data transfer is finished or not.

When peripheral receives DMA Clean signal (DMACLR), DMA Request signal is inactivated. If peripheral inactivates DMA Request before receives DMA Clear signal, it can be a problem. Also, peripheral tries to send Next DMA Request signal, it is possible only when the current DMA Clear signal is inactivated.

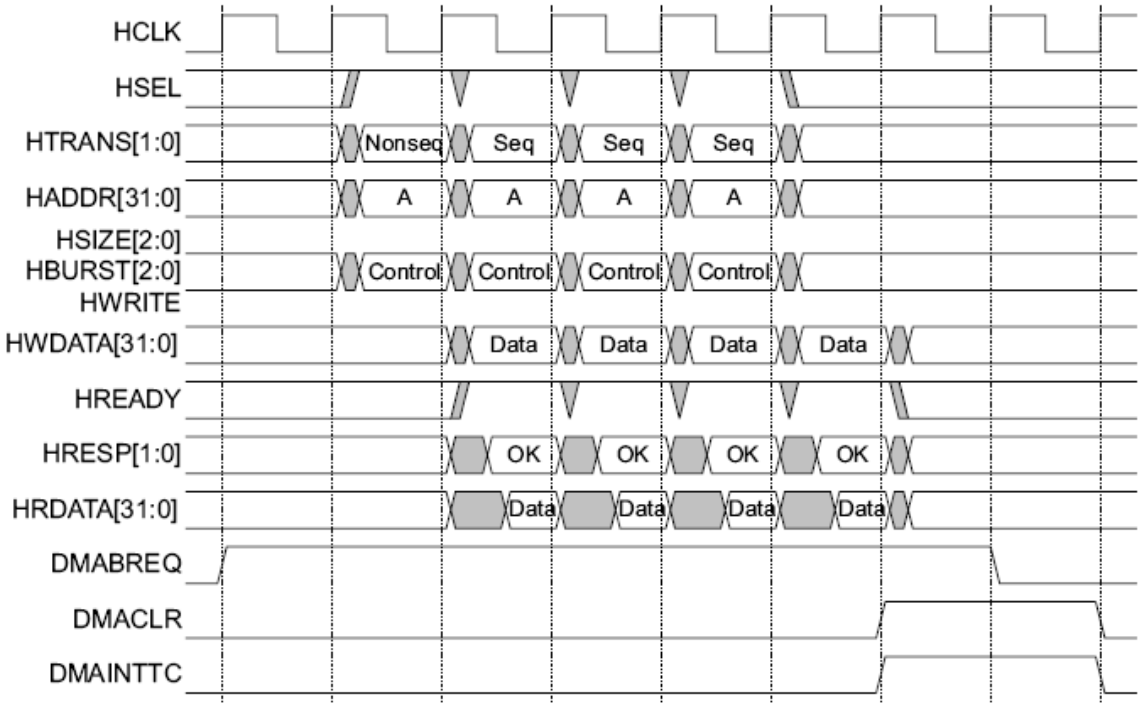


Figure 9-10 Time Diagram of DMA Request

9.4 Register Description

9.4.1 DMA Interrupt Status (DMAIntStatus)

Address: 8000_1400

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R	Interrupt Status of Channel This register indicates interrupt request status from each channel. ex) If bit 0 is set, interrupt is occurred from channel 0. If bit 1 is set, interrupt is occurred from channel 1. Because there are 2 types of interrupt, user should check interrupt type by reading DMATCIS and DMATCIC registers.	0

9.4.2 DMA Terminal Count Interrupt Status (DMATCIntStatus)

Address: 8000_1404

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R	Terminal Count Interrupt Status of Channel This register indicates whether Terminal Count Interrupt is occurred or not from each channel.	0

9.4.3 DMA Terminal Count Interrupt Clear (DMATCIntClr)

Address: 8000_1408

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	W	Terminal Count Interrupt Clear Each bit of this register has responsible for clear Terminal count interrupt. If the bit is set, a correspond channel's interrupt is cleared.	0

9.4.4 DMA Error Interrupt Status (DMAErrorIntStatus)

Address: 8000_140C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R	Error Interrupt Status of Channel The register indicated that whether the DMA Transfer error interrupt is occurred or not.	0

9.4.5 DMA Error Interrupt Clear (DMAErrorIntClr)

Address: 8000_1410

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	

7 : 0	W	Error Interrupt Clear Each bit has responsible for clearing DMA Transfer error interrupt. If the bit is set, the corresponding channel's interrupt is cleared.	0

9.4.6 DMA Block Interrupt Status (DMABlockIntStatus)

Address: 8000_1414

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R	Block Interrupt Status of Channel With this register, user can know whether DMA Block interrupt is occurred or not.	0

9.4.7 DMA Block Interrupt Clear (DMABlockIntClr)

Address: 8000_1418

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	W	Block Interrupt Clear Each bit has responsible for clearing DMA Block interrupt. If the bit is set, the corresponding channel's interrupt is cleared.	0

9.4.8 DMA Raw Terminal Count Interrupt Status (DMARawTCIntStatus)

Address: 8000_141C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R	Raw Terminal Count Interrupt Status of Channel This register informs that each channel's Terminal Count Interrupt is occurred when the channel is disabled by interrupt Enable bit.	0

9.4.9 DMA Raw Error Interrupt Status (DMARawErrorIntStatus)

Address: 8000_1420

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R	Error Interrupt Status of Channel This register informs that each channel's Error Interrupt is occurred.	0

9.4.10 DMA Enabled Channel Status (DMAEnbldChn)

Address: 8000_1424

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	

7 : 0	R	Enabled Channel Status Each bit informs that DAM is Enabled or Disabled.	0

9.4.11 DMA Software Burst Request (DMASoftBReq)

Address: 8000_1428

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	
15 : 0	RW	Software Burst Request The register generates DMA Burst Request signal in software. If user write 1 to correspond bit, DMA Burst Request signal is sent and Clear is automatically operates	0

9.4.12 DMA Software Single Request (DMASoftSReq)

Address: 8000_142C

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	
15 : 0	RW	Software Single Request The register generates DMA Single Request signal in software. If user writes 1 to corresponding bit, DMA Single Request signal is sent and Clear is automatically operates.	0

9.4.13 DMA Software Last Burst Request (DMASoftLBReq)

Address: 8000_1430

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	
15 : 0	RW	Software Last Burst Request The register generates DMA Last Burst Request signal in software. If user writes 1 to correspond bit, DMA Last Burst Request signal is sent and Clear is automatically operates.	0

9.4.14 DMA Software Last Single Request (DMASoftLSReq)

Address: 8000_1434

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	
15 : 0	RW	Software Last Single Request The register generates DMA Last Single Request signal in software. If user writes 1 to correspoing bit, DMA Last Single Request signal is sent and Clear is automatically operates.	0

9.4.15 Channel Source Address Register (ChnSrcAddr)

Address: 8000_1500 / 8000_1520 / 8000_1540 / 8000_1560
8000_1580 / 8000_15A0 / 8000_15C0 / 8000_15E0

Bit	R/W	Description	Default Value
31 : 0	RW	Source Address This register sets Source Address of each channel. The configured address value should fit alignment according to Source transfer width. Source Address automatically increases as data transfer. Due to this reason, this register should hold data address to send always. However, the source address value during a channel operation (Data transfer) is insignificant. Because the channel keeps operating data transfer, even though program reads the source address. But, after finishing the channel's data transmit, if user checks the register, user can confirm that all of data is read or not.	0

9.4.16 Channel Destination Address Register (ChnDstAddr)

Address: 8000_1504 / 8000_1524 / 8000_1544 / 8000_1564
8000_1584 / 8000_15A4 / 8000_15C4 / 8000_15E4

Bit	R/W	Description	Default Value
31 : 0	RW	Destination Address This register sets Destination Address of each channel. The configured address value should fit alignment according to Destination transfer width. Destination Address automatically increases as data transfer. Due to this reason, this register should hold data address to send always. However, the destination address value during a channel operation (Data transfer) is insignificant. Because the channel keeps operating data transfer, even though program reads the source address. But, after finishing the channel's data transmit, if	0

		user checks the register, user can confirm that all of data is read or not.	

9.4.17 Channel Linked List Item Register (ChnLLI)

Address: 8000_1508 / 8000_1528 / 8000_1548 / 8000_1568
8000_1588 / 8000_15A8 / 8000_15C8 / 8000_15E8

Bit	R/W	Description	Default Value
31 : 2	RW	Linked List Item Address This register specifies start address of Linked List Item of each channel. If the value of the register is not 0x0 and the channel is enabled, DMA Controller loads Linked List Item from the start address. After that, DMA Controller updates internal registers and executes Linked List Operation. With the default value (0x0) of the register DMA Controller does not executes Linked List Operation.	0
1 : 0	R	Reserved	0

9.4.18 Channel Control Register (ChnCntl)

Address: 8000_150C / 8000_152C / 8000_154C / 8000_156C
8000_158C / 8000_15AC / 8000_15CC / 8000_15EC

Bit	R/W	Description	Default Value
31 : 30	R	Reserved	-
29	RW	Destination Increment If set this bit, destination address is automatically increased according to data transfer.	0
28	RW	Source Increment If set this bit, source address is automatically increased according to data transfer.	0
26 : 24	RW	Destination transfer width 000 : 8bit 100 : Reserved 001 : 16bit 101 : Reserved 010 : 32bit 110 : Reserved 011 : Reserved 111 : Reserved This bit configures data width of destination. It can be set differently from source transfer width. If the destination transfer width is smaller than source transfer width, user should carefully configure Transfer size. (Refer to Program Consideration)	0
23	R	Reserved	
22 : 20	RW	Source transfer width 000 : 8bit 100 : Reserved 001 : 16bit 101 : Reserved 010 : 32bit 110 : Reserved 011 : Reserved 111 : Reserved This bit configures data width of source.	0

19	R	Reserved	
18 : 16	RW	Destination burst size 000 : 1 100 : 32 001 : 4 101 : 64 010 : 8 110 : 128 011 : 16 111 : 256 This bits configures Burst Transaction Size of destination peripheral. It is almost same as AHB Burst Size, but it is upper level transaction that includes the AHB Burst Size. (Refer to Transfer Hierarchy). In the case of the destination is memory, the register works same manner.	0
15	R	Reserved	
14 : 12	RW	Source burst size 000 : 1 100 : 32 001 : 4 101 : 64 010 : 8 110 : 128 011 : 16 111 : 256 This bits configures Burst Transaction Size of source peripheral. It is almost same as AHB Burst Size, but it is upper level transaction that includes the AHB Burst Size. (Refer to Transfer Hierarchy). In the case of the source is memory, the register works same manner.	0
11 : 0	RW	Transfer Size When DMA Controller is Flow Controller, this register indicates the total size of transferred data from DMA channel. The unit of transfer is not Byte but Source Transfer Width. In order words, the total size of data transfer is calculated as (Transfer size) x (source transfer width) This value is decreased as 1 when transfers data. Once the value is 0, DMA Transfer is finished. Therefore, user can know remain data size to transfer if user reads the value. If DMA Controller is not Flow Controller, the value is ignored but the value should be 0 in Program.	000

9.4.19 Channel Configuration Register (ChnCfg)

Address: 8000_1510 / 8000_1530 / 8000_1550 / 8000_1570
8000_1590 / 8000_15B0 / 8000_15D0 / 8000_15F0

<table>
<tr><th>Bit</th><th>R/W</th><th>Description</th><th>Default Value</th></tr>
<tr><td>31 : 22</td><td>R</td><td>Reserved</td><td>0</td></tr>
<tr><td>21</td><td>RO</td><td>FIFO Active
0: FIFO is empty
1 : FIFO has data</td><td>-</td></tr>
<tr><td>20</td><td>RW</td><td>Halt
0 : enable DMA request
1 : ignore DMA request.
User can disable DMA channel by using this bit and clears out FIFO</td><td>0</td></tr>
<tr><td>19</td><td>RW</td><td>Lock
If this bit is set, Locked transfer is operated.</td><td>0</td></tr>
<tr><td>18</td><td>RW</td><td>Block Interrupt Enable
Interrupt Enable bit when Block transfer is finished with Multi Block Transfer. If Block Interrupt is occurred, DMA does not transfer Next Block until the Block Interrupt is cleared.</td><td></td></tr>
<tr><td>17</td><td>RW</td><td>Terminal count interrupt Enable
Enable bit for DMA Transfer finish interrupt.</td><td>0</td></tr>
<tr><td>16</td><td>RW</td><td>Interrupt error Enable
Enable bit for DMA Error Interrupt.</td><td>0</td></tr>
<tr><td>15</td><td>R</td><td>Reserved</td><td>0</td></tr>
<tr><td>14 : 12</td><td>RW</td><td>Flow Control
<table>
<tr><th>Value</th><th>Transfer type</th><th>Flow controller</th></tr>
<tr><td>000</td><td>Memory-to-Memory (Default)</td><td>DMA</td></tr>
<tr><td>001</td><td>Memory-to-Peripheral</td><td>DMA</td></tr>
<tr><td>010</td><td>Peripheral-to-Memory</td><td>DMA</td></tr>
<tr><td>011</td><td>Source peripheral-to-destination peripheral</td><td>DMA</td></tr>
<tr><td>100</td><td>Source peripheral-to-destination peripheral</td><td>Dst. Peri.</td></tr>
<tr><td>101</td><td>Memory-to-Peripheral</td><td>Peripheral</td></tr>
<tr><td>110</td><td>Peripheral-to-Memory</td><td>Peripheral</td></tr>
<tr><td>111</td><td>Source peripheral-to-Destination peripheral</td><td>Src. Peri.</td></tr>
</table>
This bit determines both Transfer type and Flow Controller.</td><td></td></tr>
<tr><td>11 : 8</td><td>RW</td><td>Destination Peripheral
This bit selects one of the 16 DMA Requests.
0000: NAND Flash TX 0001: SDHC
0010: Reserved 0011: Reserved
0100: USB Device Bulk In 0101: Mixer Play CH0
0110: Mixer Play CH1 0111: Mixer Play CH2
1000: Mixer Play CH3 1001: Reserved
…
1110: Reserved 1111: Reserved</td><td>0</td></tr>
<tr><td>7 : 4</td><td>RW</td><td>Source Peripheral
This bit selects one of the 16 DMA Requests.
0000: Reserved 0001: SDHC
0010: NAND Flash RX 0011: USB Device Bulk Out</td><td>0</td></tr>
</table>

		0100: Reserved 0101: Reserved 0110: Reserved 0111: Reserved 1000: Reserved 1001: Mixer Record 1010: ADC … 1110: Reserved 1111: Reserved	
3 : 1	R	Reserved	0
0	RW	Channel Enable Channel can be activated by this bit. In order to do DMA Transfer, user sets this bit. If the bit is set to 1, DMA Transfer is started with configuration. If the DMA Transfer is finished, this bit is automatically cleared. Auto Clear conditions are following. 1. Finish DMA Transfer 2. Finish Linked List Operation 3. Finish Auto Reload Operation 4. Finished by Error User can finish the activated channel manually by clearing the Enable bit. However, in this case, all of channel FIFO data is removed.	0

9.4.20 Channel Source Gather Address Register (ChnSrcGaAddr)

Address: 8000_1514 / 8000_1534 / 8000_1554 / 8000_1574
8000_1594 / 8000_15B4 / 8000_15D4 / 8000_15F4

Bit	*R/W*	*Description*	*Default Value*
31 : 16	R	Reserved	-
16	RW	Auto Reload Source Address If this bit is set, Source Address is reloaded with initially configured source address when Auto Reload.	
15 : 0	RW	Source Gather Address When Auto Reload is operated, the Source Address is added with Source Gather Address.	0

9.4.21 Channel Destination Scatter Address Register (ChnDstScaAddr)

Address: 8000_1518 / 8000_1538 / 8000_1558 / 8000_1578
8000_1598 / 8000_15B8 / 8000_15D8 / 8000_15F8

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
16	RW	Auto Reload Destination Address If this bit is set, Destination Address is reloaded with initially configured source address when Auto Reload.	
15 : 0	RW	Destination Scatter Address When Auto Reload is operated, the Destination Address is added with Destination Scatter Address.	0

9.4.22 Channel Auto Reload Count Register (ChnAutoReloadCnt)

Address: 8000_151C / 8000_153C / 8000_155C / 8000_157C
8000_159C / 8000_15BC / 8000_15DC / 8000_15FC

Bit	R/W	Description	Default Value
31 : 22	R	Reserved	-
21	RW	Uncountable Auto Reload If this bit is set, Auto Reload is operated regardless of Auto Reload Count.	
20 : 0	RW	Auto Reload Count User can specify Auto Reload Count to this bits and can repeat DMA Transfer. The Auto Reload count is decreased when Block transfer is finished (Transfer Size becomes 0). If the value becomes 0, Auto Reload Operation is finished.	0

9.5 Program Guide

9.5.1 Sumary of Register

Name	Address	Type	Description
DMAIntStatus	0x000	R	DMA Interrupt Status
DMATCIntStatus	0x004	R	DMA Terminal Count Interrupt Status
DMATCIntClr	0x008	W	DMA Terminal Count Interrupt Clear
DMAErrorIntStatus	0x00C	R	DMA Error Interrupt Status
DMAErrorIntClr	0x010	W	DMA Error Interrupt Clear
DMABlockIntStatus	0x014	R	DMA Block Interrupt Status
DMABlockIntClr	0x018	W	DMA Block Interrupt Clear
DMARawTCIntStatus	0x01C	R	DMA Raw Terminal Count Interrupt Status
DMARawErrorIntStatus	0x020	W	DMA Raw Error Interrupt Status
DMAEnbldChns	0x024	R	DMA Enabled Channels
DMASoftBReq	0x028	RW	DMA Software Burst Request
DMASoftSReq	0x02C	RW	DMA Software Single Request
DMASoftLBReq	0x030	RW	DMA Software Last Burst Request
DMASoftLSReq	0x034	RW	DMA Software Last Single Request
ChnSrcAddr	0x100	RW	Channel Source Address
ChnDestAddr	0x104	RW	Channel Destination Address
ChnLLI	0x108	RW	Channel Linked List Item
ChnCntl	0x10C	RW	Channel Control
ChnCfg	0x110	RW	Channel Configuration
ChnSrcGaAddr	0x114	RW	Channel Source Gather Address
ChnDestScatAddr	0x118	RW	Channel Destination Scatter Address
ChnAutoReloadCnt	0x11C	RW	Channel Auto Reload Count

9.5.2 Programming Sequence

- **DMA Operation (Memory to Memory)**
  1. Choose a channel to transfer
  2. Configures Source Address of the channel (ChnSrcAddr Register)
  3. Configures Destination Address of the channel (ChnDstAddr Register)
  4. Configures Transfer Width of source and destination (ChnCntl Register)
  5. Configures Burst Size of source and destination (ChnCntl Register)
  6. Configures Transfer Size (DMA Transfer size) (ChnCntl Register)
  7. Enables the Channel (ChnCfg Register)
  8. Check the DMA Transfer is finished (DMAEnbldChns Register)
  9. Finish

- **DMA Operation (Memory to Peripheral)**
  1. Choose a channel to transfer
  2. Configures Source Address of the channel (ChnSrcAddr Register)
  3. Configures Destination Address of the channel (ChnDstAddr Register)
  4. Configures Transfer Width of source and destination (ChnCntl Register)
  5. Configures Burst Size of source and destination (ChnCntl Register)
  6. Configures Transfer Size (DMA Transfer size) (ChnCntl Register)

7. Configures Transfer Type (ChnCfg Register)
8. Enables the Channel (ChnCfg Register)
9. Check the DMA Transfer is finished (DMAEnbldChns Register)
10. Finsh

- **Linked List Operation (Memory to Memory)**

  Assumes that the Linked List Item is already prepared.

  1. Choose a channel to operate
  2. Configures the first LLI address (ChnLLI Register)
  3. Enables the channel (ChnCgf Register)
  4. Checks the operation is finished (DMAEnbldChns Register)
  5. Finish

- **Auto Reload Operation Program (Memory to Memory)**

  1. Choose a channel to operate
  2. Configures Source Address of the channel (ChnSrcAddr Register)
  3. Configures Destination Address of the channel (ChnDstAddr Register)
  4. Configures Transfer Width of source and Destination (ChnCntl Register)
  5. Configures Burst Size of source and destination (ChnCntl Register)
  6. Configures Transfer Size (DMA Transfer size) (ChnCntl Register)
  7. Specifies Auto Reload Size (ChnAutoReloadCnt Register)
  8. Enables the Channel (ChnCfg Register)
  9. Check the DMA Transfer is finished (DMAEnbldChns Register)
  10. Finsh

9.5.3 Program Consideration

User program should consider following restrictions.

1. User should not change the channel's register value after the channel is enabled. Because DMA Transfer is operated after the channel is enabled, modifying register value may induce problem. Due to that reason, user should check whether the channel is enabled or disabled to modify register value.

2. DMA Transfer size is set to times of Destination transfer width if source transfer width is smaller than destination transfer width. DMA Transfer size is calculated with the size of read data in source (Source width x Transfer size). If the DMA Transfer size does not match with Destination width x N, the size of written data in destination is smaller or larger.

3. Linked List Item does not allocate in address 0x0.

10 FLASH MEMORY CONTROLLER

Maximum capacity of Flash memory is 16Mbytes and maximum clock frequency is 80MHz. However Flash Memory Controller uses divided AHB Clock frequency. Due to that reason, Flash Memory operates half of the maximum frequency.

10.1 Feature

- Provides Single, Double, and Quad bit data transfer
- Provides Flash Erase and Flash Program in both H/W and S/W
- Provides XIP (eXecute In Place)

10.2 Function Description

10.2.1 Flash Mode Register (FLMOD)

Determines Flash operation mode.
It can access flash data by Single, Dual and Quad bit size.

10.2.2 Flash Baudrate Register (FLBRT)

Determines Flash Baudrate.
It can configure width between high pulse and low pulse of clock frequency..

10.2.3 Flash Chip Select High Pulse Width Register (FLCSH)

It determines deselect time of Chips select signal.
If the chips select signal is deselected, current status should not be changed.
After read operation, in the case of program tries to read, user keeps 50ns to access Status register after Erase or Program execution.
User connects external Flash memory to *adstar,* the value of time is different according to flash type. Due to that reason, user should check the Flash deselect time.

10.2.4 Flash Command Register (FLCMD)

Commands Chip Erase (C7h/60h), Power-down (B9h) and Release Power-down (ABh).

- Chip Erase (C7h/60h)

If user writes C7h or 60h to the register, entire flash data is erased.

- Power-Down (B9h)

If user writes B9h to the register, flash becomes power-down state after 3us (tDP).
** (caution) Before power-down state, program should be executed in another memory space.

- Release Power-down (ABh)

If user writes ABh to the register, flash becomes stand-by state from power-down state after 3us (tRES1).

10.2.5 Flash Status Register (FLSTS)

The register access the lowest 1byte of Flash status register.
It is used for checking bit0 (BUSY) that indicates write operation is finished or not.

10.2.6 Flash 2nd Status Register (FLSTS2)

The register access the highest 1byte of Flash status register.
It is used for support Quad mode that can be done by setting bit1 (QE).

10.2.7 Flash Sector/Block Erase Address Register (FLSEA/FLBEA)

With this register, user can erase flash in the unit of sector or block.
If user writes sector or block address to erase, the corresponding memory address is removed.

10.2.8 Flash WIP Check Period Register (FLWCP)

This register determines the period of check in hardware, when user writes Flash such as program and erase. According to the value, Flash controller reads status register 0bit (BUSY). If the value of the bit is changed 1 into 0, the write operation is finished.

10.2.9 Flash Clock Delay Register (FLCKDLY)

The register is user for correction of Flash read timing.
User can delay read clock according to the value of the register.

10.3 Register Description

10.3.1 Flash Mode Register (FLMOD)

Address : 0x8000_0000

Bit	R/W	Description	Default Value
31:9	R	Reserved	-
8	R/W	Chip select control 1: Chip select signal is controlled by H/W 0: Fix Chip select signal to Low Level	1b
7	R/W	Bus Error Enable 1: When user accesses to Flash in order to write, incurs Bus Error. 0: Allows Flash write access.	1b
6	R	Reserved	-
5	R	EQIO Mode Flag (Check Flash support) 1: EQIO Mode 0: Normal Mode If user writes EQIO (38h) to Command Register, Flash changes to EQIO mode.	0
4	R	Performance Enhance Mode (Check Flash support) 1: Applied Performance Enhance Mode 0: Normal Mode. If user enables Enhance Mode by writing 1 to FLPEM Register, It is enabled only when the Flash mode is Quad read or EQIO mode.	0
3	R/W	Bus Ready Control 0: Controls bus ready in case of write operation. S/W needs not check flash status. 1: After write operation, S/W checks flash status.	0b
2	R	Reserved	-
1:0	R/W	Flash Read Mode 00: Single Read Mode 01: Dual Read Mode 10: Quad Read Mode 11: Reserved	00b

10.3.2 Flash Baudrate Register (FLBRT)

Address : 0x8000_0004

Bit	R/W	Description	Default Value
31:8	R	Reserved	-
7:4	R/W	SCK High Pulse Width 0000: 1clock 0001: 2clocks 0010: 3clocks … 1110: 15clocks 1111: 16clocks	111b
3:0	R/W	SCK Low Pulse Width 0000: 1clock 0001: 2clocks 0010: 3clocks … 1110: 15clocks 1111: 16clocks	111b

10.3.3 Flash Chip Select High Pulse Width Register (FLCSH)

Address : 0x8000_0008

Bit	R/W	Description	Default Value
31:4	R	Reserved	-
3:0	R/W	Chip Select High Pulse Width (100ns 필요) 0000: 1clock 0001: 2clocks 0010: 3clocks … 11111110: 255clocks 11111111: 256clocks	FFh

10.3.4 Flash Performance Enhance Mode Register (FLPEM)

Address : 0x8000_000C

Bit	R/W	Description	Default Value
31:1	R	Reserved	-
0	R/W	Performance Enhance Mode 1: Enable 0: Disable	0b

10.3.5 Flash Command Register (FLCMD)

Address : 0x8000_0010

Bit	R/W	Description	Default Value
31:8	R	Reserved	-
7:0	R/W	Flash Command	0b

10.3.6 Flash Status Register (FLSTS)

Address : 0x8000_0014

Bit	R/W	Description	Default Value
31:8	R	Reserved	-
7:0	R/W	Flash Status	0b

10.3.7 Flash Sector Erase Address Register (FLSEA)

Address : 0x8000_0018

Bit	R/W	Description	Default Value
31:24	R	Reserved	-
23:0	R/W	Flash Sector Address to Erase	0b

10.3.8 Flash Block Erase Address Register (FLBEA)

Address : 0x8000_001C

Bit	R/W	Description	Default Value
31:24	R	Reserved	-
23:0	R/W	Flash Block Address to Erase	0b

10.3.9 Flash Data Register (FLDAT)

Address : 0x8000_0020

Bit	R/W	Description	Default Value
31:0	R/W	Flash Data (8, 16, 32-bit supported)	0b

10.3.10 Flash WIP Check Period Register (FLWCP)

Address : 0x8000_0024

Bit	R/W	Description	Default Value
31:0	R/W	Flash WIP Status Check Period	FFFh

10.3.11 Flash Clock Delay Register (FLCKDLY)

Address : 0x8000_0028

Bit	R/W	Description	Default Value
3:0	R/W	Serial Flash Feed-back Clock Delay Value	0h

10.3.12 Flash 2nd Status Register (FLSTS2)

Address : 0x8000_002C

Bit	R/W	Description	Default Value
15:8	W	Flash 2nd Status (Winbond only)	-
7:0	R/W	READ 시] Flash 2nd Status (Winbond only) WRITE 시] Flash 1nd Status (Winbond only)	-

11 LOCAL MEMORY CONTROLLER

11.1 Register Description

11.1.1 SDRAM Control Register (MEMCON)

Address : 0x8000_0400

Bit	*R/W*	*Description*	*Default Value*
31 : 8	R	Reserved	-
7 : 6	R/W	Row Address Line Number 00 : 11 bit 01 : 12 bit 10 : 13 bit 11 : 14 bit	11b
5 : 4	R/W	Column Address Line Number 00 : 8 bit 01 : 9 bit 10 : 10 bit 11 : 11 bit	11b
3	R/W	Timing Constraint Select (0 : Upper 100MHz , 1 : Under 100 MHz) 0 : tRCD = 3 Clock, tRP = 3 Clock, tRAS = 7 Clock, tRC = 10 Clock 1 : tRCD = 2 Clock, tRP = 2 Clock, tRAS = 5 Clock, tRC = 7 Clock	0b
2	R/W	CAS Latency 0 : 2 Clock 1 : 3 Clock	0b
1 : 0	R/W	This bit determine data bus width 00 : 8 bit 01 : 16 bit 10 : 32 bit 11 : Reserved	01b

< Register Bit field description >

1. Bit [7:6]: Selects the number of SDRAM Row Address.
2. Bit [5:4]: Selects the number of SDRAM Column Address.
3. Bit [3]: It determines Timing condition to operate SDRAM.
   If the clock frequency is upper 100MHz, the bit is set to 0, otherwise 1.
4. Bit [2]: Selects CAS Latency Cycle of SDRAM operation.
5. Bit [1:0]: It determines SRAM Data Bus Width of its bank.

11.1.2 SDRAM Clock Delay Register (MEMCLKCON)

Address : 0x8000_0404h

Bit	*R/W*	*Description*	*Default Value*
31 : 12	R	Reserved	-
11 : 8	R/W	Local SDRAM Clock Generation (Clock delay) 0000 : CLOCK 1000 : Invert CLOCK 0001 : CLOCK+ 1ns 1001 : Invert CLOCK+ 1ns 0010 : CLOCK+ 2ns 1010 : Invert CLOCK+ 2ns 0011 : CLOCK+ 3ns 1011 : Invert CLOCK+ 3ns 0100 : CLOCK+ 4ns 1100 : Invert CLOCK+ 4ns 0101 : CLOCK+ 5ns 1101 : Invert CLOCK+ 5ns 0110 : CLOCK+ 6ns 1110 : Invert CLOCK+ 6ns	0h

		0111 : CLOCK+ 7ns 1111 : Invert CLOCK+ 7ns	
7 : 0	R/W	1Mhz Clock generation Divider Value	FFh

< Register bit field description >

1. Bit [11:8]: It determines delay of SDRAM Feedback Clock for SDRAM Data read operation.
2. Bit [7:0]: It configures Clock generation Divider value to generate1MHz frequency. Because its value is (Main Clock/(n+ 1)), divider value should be set to n-1.

11.1.3 SDRAM Refresh Control Register (MEMREFCON)

Address : 0x8000_0408h

Bit	*R/W*	*Description*	*Default Value*
31 : 10	R	Reserved	-
9	R/W	Refresh Period < Refresh Source : 1Mhz > 0 : 15 usec 1 : 30 usec	0b
8	R/W	Number of Refresh Cycle / Period < Refresh Source : 1Mhz > 0 : 1 Cycle 1 : 2 Cycle	0b
7 : 1	R	Reserved	-
0	R/W	0: Auto Refresh 1: Self Refresh	0b

< Register bit field description >

1. Bit [9]: It determines Refresh Period when Refresh Source frequency is 1MHz.
2. Bit [8]: It determines the number refresh cycle per period.
3. Bit [0]: Refresh Mode Select.

12 EXTERNAL SRAM CONTROLLER

12.1 Function Description

adstar supports 8/16-bit external NOR Flash, PROM, and SRAM. In addition it supports 4 memories with maximum 512KB size.

For External Static Memory Interface, SRAM Controller supports SRAM_ALE1, SRAM_ALE0, SRAM_nCS[3:0], SRAM_nRE, SRAM_nWE, AD[15:0], A[18:16], and nBE1.

When SRAM controller interfaces external 8-bit SRAM Memory, AD[7:0] generates Address[15:0] and Data[7:0] signals. If SRAM_ALE1 latches AD[7:0], then the AD[7:0] generates Address[15:8]. If SRAM_ALE0 latches AD[7:0], then the AD[7:0] generates Address[7:0]. After these operation, AD[7:0] reads/writes Data[7:0] in SRAM_nCS, SRAM_nRE, and SRAM_nWE periods.

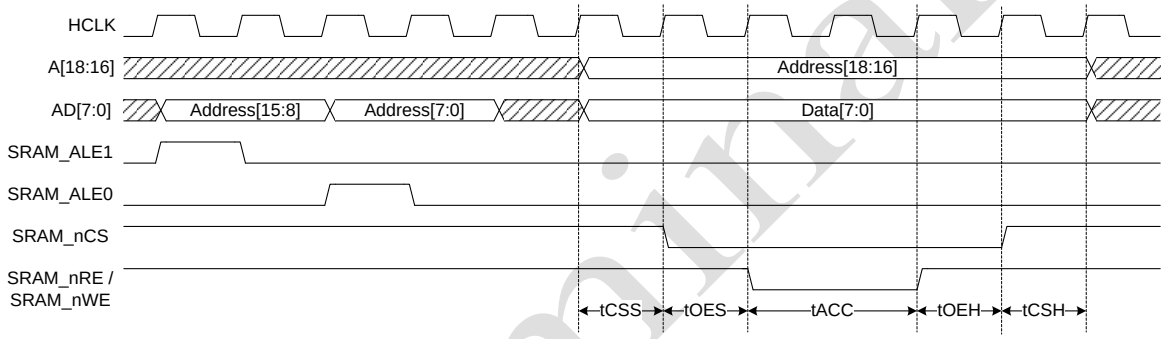


Figure 12-1 External 8-bit SRAM Memory Timing Diagram

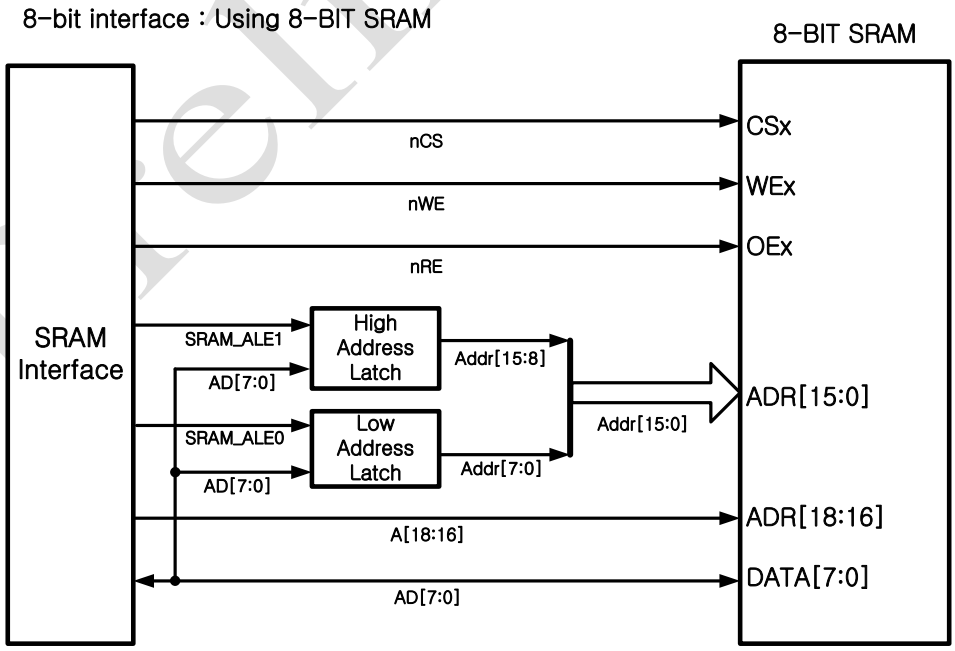


Figure 12-2 Connection 8-bit SRAM Memory

When SRAM controller interfaces external 86-bit SRAM Memory, AD[15:0] generates Address[15:0] and Data[15:0] signals. If SRAM_ALE0 latches AD[15:0], then the AD[15:0] generates Address[15:0]. After that operation, AD[15:0] reads/writes Data[15:0] in SRAM_nCS, SRAM_nRE, and SRAM_nWE periods.

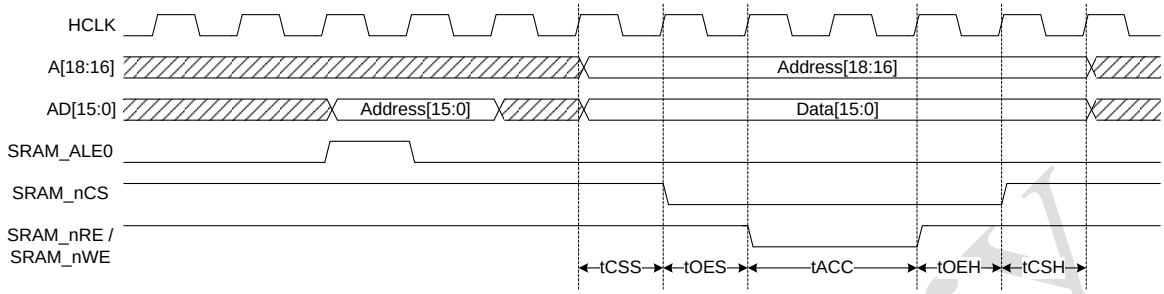


Figure 12-3 External 16-bit SRAM Memory Timing Diagram

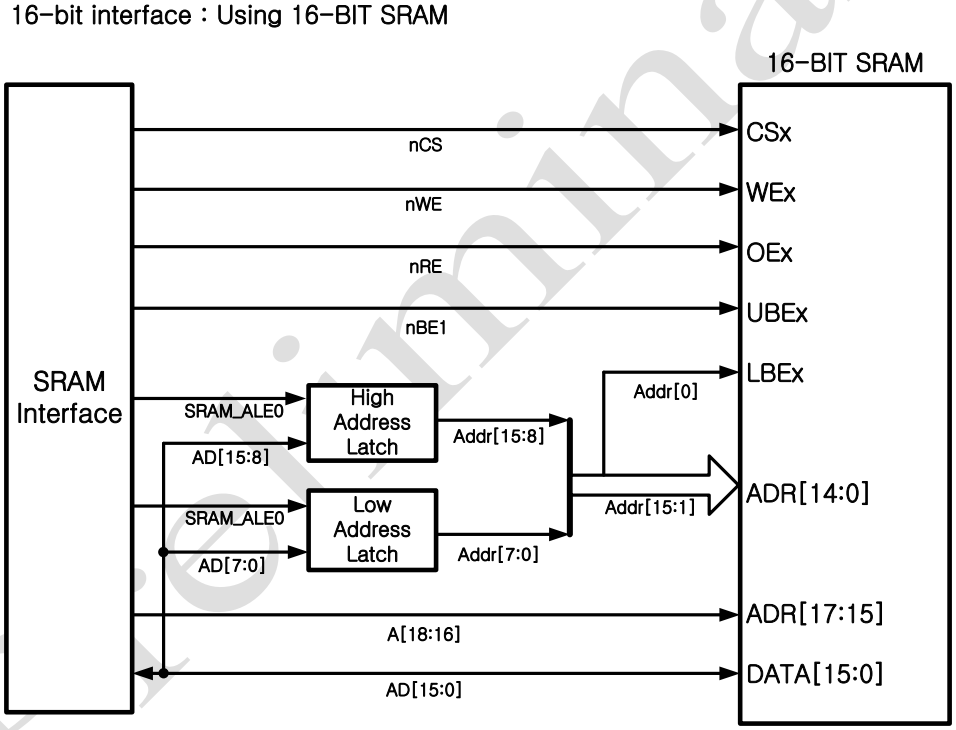


Figure 12-4 Connection 16-bit SRAM Memory

12.2 Register Description

12.2.1 External SRAM_nCS0 Area Control Register (CS0CTRL)

Address : 0x8000_0800

Bit	R/W	Description	Default Value
23 : 22	R/W	tALE1H : Address Latch Enable Hold 00 : 0 Clock 01 : 1 Clock 10 : 2 Clock 11 : 4 Clock	11
21 : 20	R/W	tALE1S : Address Latch Enable Setup 00 : 0 Clock 01 : 1 Clock 10 : 2 Clock 11 : 4 Clock	11
19 : 18	R/W	tALE0H : Address Latch Enable Hold 00 : 0 Clock 01 : 1 Clock 10 : 2 Clock 11 : 4 Clock	11
17 : 16	R/W	tALE0S : Address Latch Enable Setup 00 : 0 Clock 01 : 1 Clock 10 : 2 Clock 11 : 4 Clock	11
15 : 14	R/W	tCSS : Address Set-up before SRAM_nCS0 00 : 0 Clock 01 : 1 Clock 10 : 2 Clock 11 : 4 Clock	11
13 : 12	R/W	tOES : Chip Selection Set-up nRE / nWE 00 : 0 Clock 01 : 1 Clock 10 : 2 Clock 11 : 4 Clock	11
11 : 8	R/W	tACC : Access Cycle 0000 : 1 Clock 0001 : 2 Clock 0010 : 3 Clock 0011 : 4 Clock 0100 : 6 Clock 0101 : 8 Clock 0110 : 10 Clock 0111 : 12 Clock 1000 : 14 Clock 1001 : 16 Clock 1010 : 18 Clock 1011 : 20 Clock 1100 : 22 Clock 1101 : 24 Clock 1110 : 26 Clock 1111 : 30 Clock	1111
7 : 6	R/W	tOEH : Chip Selection Hold on nRE / nWE 00 : 0 Clock 01 : 1 Clock 10 : 2 Clock 11 : 4 Clock	11
5 : 4	R/W	tCSH : Address Holding Time after SRAM_nCS0 00 : 0 Clock 01 : 1 Clock 10 : 2 Clock 11 : 4 Clock	11
3	R/W	This bit determines whether using nBE1 pin for 16bit Data bus 0 : Not using nBE1 1 : Using nBE1	0
2	R/W	This bit determines WAIT status 0 : nWAIT Disable 1 : nWAIT Enable	0
1	R/W	This bit determines data bus width 0 : 8 bit 1 : 16 bit	0
0	R/W	Error Response Enable bit in Read only Memory 0 : Error Response Disable 1 : Error Response Enable	0

12.2.2 External SRAM_nCS[3:1] Area Control Register (CSxCTRL)

Address : 0x8000_0804 / 0x8000_0808 / 0x8000_080C

Bit	R/W	Description	Default Value
31 : 24	R	Reserved	-
23 : 22	R/W	tALE1H : Address Latch Enable Hold 00 : 0 Clock 01 : 1 Clock 10 : 2 Clock 11 : 4 Clock	11
21 : 20	R/W	tALE1S : Address Latch Enable Setup 00 : 0 Clock 01 : 1 Clock 10 : 2 Clock 11 : 4 Clock	11
19 : 18	R/W	tALE0H : Address Latch Enable Hold 00 : 0 Clock 01 : 1 Clock 10 : 2 Clock 11 : 4 Clock	11
17 : 16	R/W	tALE0S : Address Latch Enable Setup 00 : 0 Clock 01 : 1 Clock 10 : 2 Clock 11 : 4 Clock	11
15 : 14	R/W	tCSS : Address Set-up before SRAM_nCSx 00 : 0 Clock 01 : 1 Clock 10 : 2 Clock 11 : 4 Clock	11
13 : 12	R/W	tOES : Chip Selection Set-up nRE / nWE 00 : 0 Clock 01 : 1 Clock 10 : 2 Clock 11 : 4 Clock	11
11 : 8	R/W	tACC : Access Cycle 0000 : 1 Clock 0001 : 2 Clock 0010 : 3 Clock 0011 : 4 Clock 0100 : 6 Clock 0101 : 8 Clock 0110 : 10 Clock 0111 : 12 Clock 1000 : 14 Clock 1001 : 16 Clock 1010 : 18 Clock 1011 : 20 Clock 1100 : 22 Clock 1101 : 24 Clock 1110 : 26 Clock 1111 : 30 Clock	1111
7 : 6	R/W	tOEH : Chip Selection Hold on nRE / nWE 00 : 0 Clock 01 : 1 Clock 10 : 2 Clock 11 : 4 Clock	11
5 : 4	R/W	tCSH : Address Holding Time after SRAM_nCSx 00 : 0 Clock 01 : 1 Clock 10 : 2 Clock 11 : 4 Clock	11
3	R/W	This bit determines whether using nBE1 pin for 16bit Data bus 0 : Not using nBE1 1 : Using nBE1	0
2	R/W	This bit determines WAIT status 0 : nWAIT Disable 1 : nWAIT Enable	0
1	R/W	This bit determines data bus width 0 : 8 bit 1 : 16 bit	0
0	R/W	Error Response Enable bit in Read only Memory 0 : Error Response Disable 1 : Error Response Enable	0

13 NAND FLASH CONTROLLER

NAND Flash controls data transfer of 8-bit I/O NAND Flash Memory.

13.1 Features

- 8bit I/O support
- 3-cycle/4-cycle/5-cycle Address support
- 1bit for SLC and 4bit/24bit ECC for MLC
- Auto ECC Decoding support

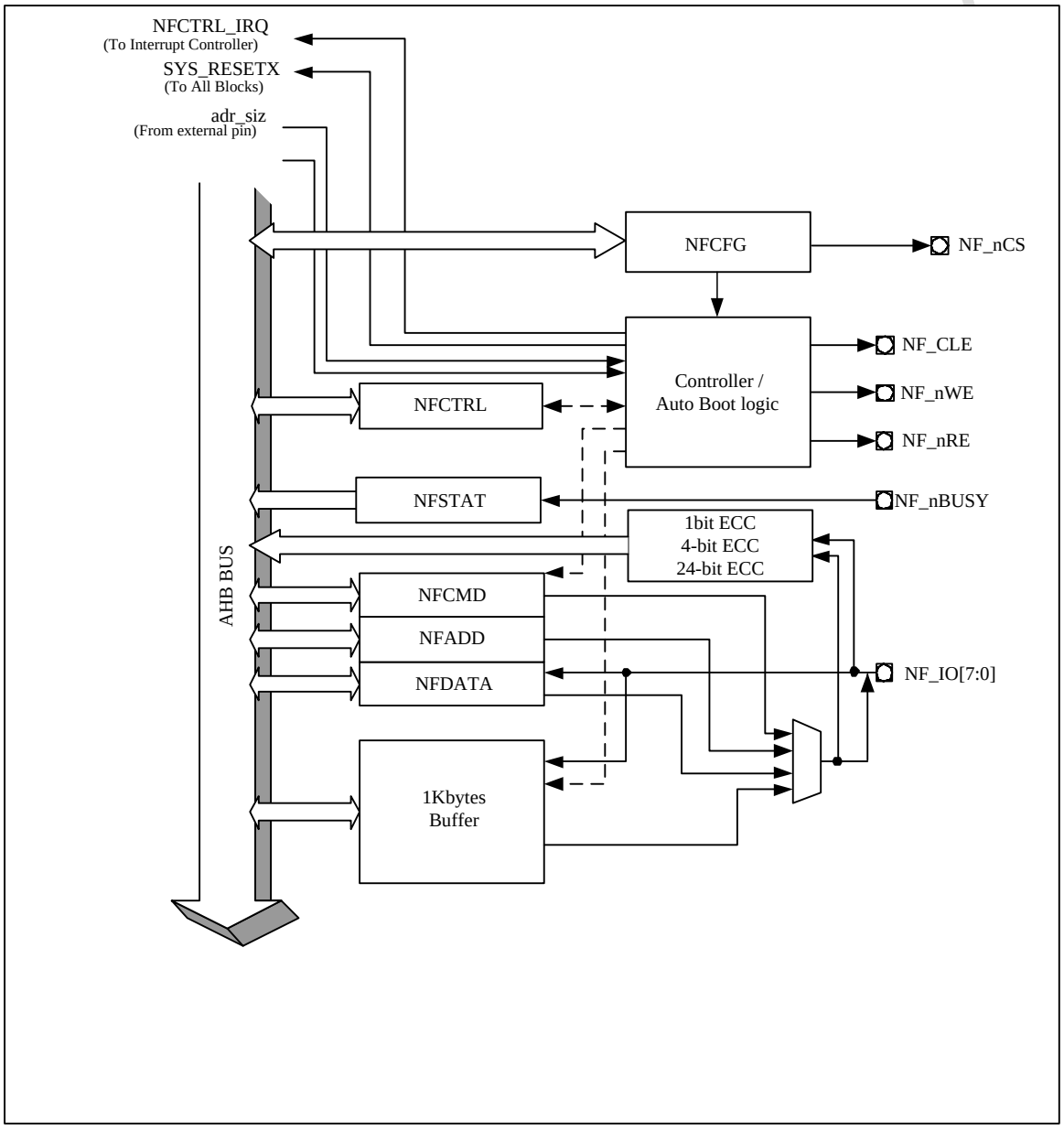


Figure 13-1 NAND Flash Controller Block Diagram

13.2 Function Desciption

Data Read/Write

1. Configures timing for data transfer to NFCFG register.
2. Configures NAND Flash Memory Command to NFCMD register.
3. Configures NAND Flash Memory address for access to NFADR register. At that time, repeatedly configures the register as Address cycle to NAND Flash access.
4. Operates Read/Write by NFCPUDATA. Before/After read data, user should check NDFL_nBUSY.

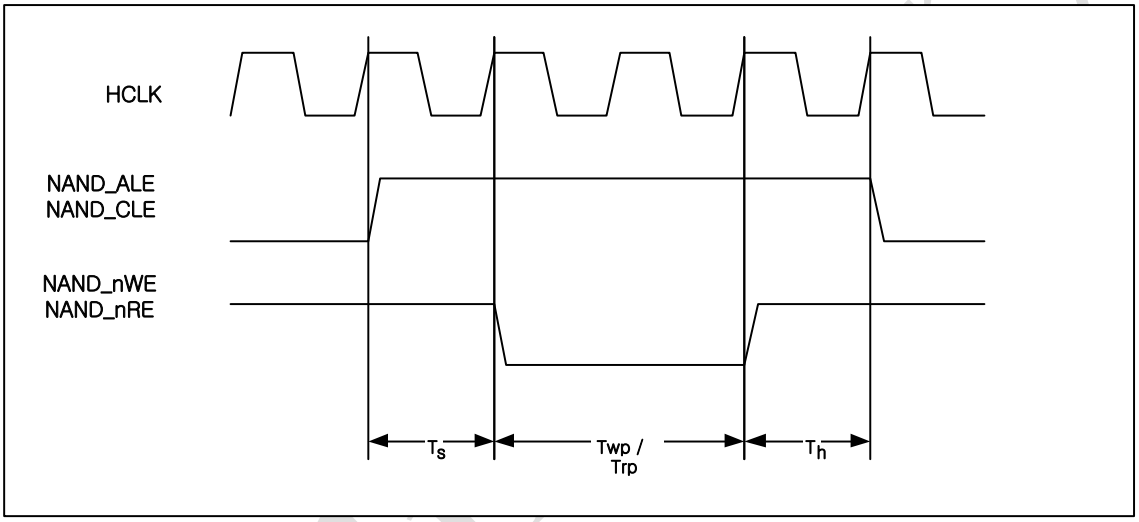


Figure 13-2 Read/Write Timing Diagram of NAND Flash Memory

DMA Operation

NAND Flash controller supports DMA Data Transfer. First of all, configures DMA Controller, then configures NAND Flash controller. If User configures DMA operation by NFCTRL register, NAND Flash Memory starts to DMA data transfer. In the case of the NAND Flash Memory is Large type (second generation), user can configures maximum 2Kbytes data transfer unit. In the case of the NAND Flash Memory is Small type (first generation), user can configures maximum 512Bytes for data transfer

13.3 ECC Operation

adStar provides not only SLC type, but MLC type NAND Flash. Because MLC type NAND Flash has higher error probability than SLC type, programmer should correct the error.

NAND Flash Controller generates Parity bit by using BCH algorithm. With the parity bit, *adStar* can correct data error. *adStar* provides error detection and error correction in 4-bit error for 512Bytes data and 24-bit error for 1Kbytes data.

ECC Encoding

1. After configures NFCFG register to use NAND Flash, Command and Address are sent.
2. After read NFECC1 register, clears ECC status and ECC registers.
3. Set ECC GEN bit of NFCTRL register to 1. (ECC Generation Enable)
4. Send 512Bytes or 1024Bytes data. Whenever data is transmitted, 52-bit or 336-bit Parity bits are generated and stored into NFECCn registers.
5. After finish sending data, reads the data in the order of NFECC0 register, NFECC1 register and stores into memory.
6. In order to continue to 512Bytes or 1024Bytes data transfer, repeats step 2~5.
7. If the1-page data transfer is finished, sets ECC GEN bit of NFCTRL register to 1. (ECC Generation disable)
8. Stores Parity bits of 512Bytes or 1024Bytes data in memory into spare space of NAND Flash.

ECC Decoding by S/W

1. After configures NFCFG register to use NAND Flash, Command and Address are sent.
2. After read NFECC1 register, clears ECC status and ECC registers.
3. Selects 4-bit or 24-bit ECC mode form NFCTRL register, then sets ECC GEN bit to 1. (ECC Decoding enable)
4. Reads 512Bytes or 1024Bytes data.
5. After read the data, accesses spare space and read parity bits.
6. After read the parity bits, automatically starts decoding. User can check the decoding is finished and succeeded by read NFSTAT register.
7. After finish decoding, NFERRLOC0~3 or NFERRLOC23 register holds error location, and NFERRPTN0~3 or NFERRPTN23 register holds 8-bit error pattern.
8. Correcting error data by Exclusive-OR Error location of NFERRLOCn register and error pattern of NFERRPTNn.
9. Repeats step 2~8 until finish reading 1-page.

ECC Decoding by H/W (Auto ECC Decoding)

1. After configures NFCFG register to use NAND Flash, Command and Address are sent.
2. After read NFECC10 register, clears ECC status and ECC registers.
3. Selects 4-bit or 24-bit ECC mode from NFCTRL register, and set Auto ECC

Decode bit to 1, then automatically reads data and parity from NAND Flash.

4. Check the Auto ECC Done bit of NFSTAT register is 1.
5. Reads error correction data from NFECD register
6. Repeats step 2~5 until finish reading 1-page.

13.4 Register Description

13.4.1 NAND Flash Memory Control Register (NFCTRL)

Address: 0xA000_0C00

Bit	R/W	Description	Default Value
16	R/W	Auto ECC Enable bit 0: Auto ECC done 1: Auto ECC Start If the bit is set, Auto ECC is stated, and automatically clear when finished.	0
15	R/W	4-bit ECC Mode Set bit 0: 24-bit ECC Mode 1: 4-bit ECC Mode	1
14:13	R	Reserved	-
12	R/W	ECC Generation Enable bit 0 : Disable 1 : Enable	0
11	R/W	Endian Select bit 0 : Little Endian 1 : Big Endian	0
10	R/W	Data Swap Size 0 : 8bit 1 : 16bit	0
9	R/W	DMA Write Request bit 0 : DMA Write Request Clear 1 : DMA Write Request If the bit is set, DMA Transfer is stated, and automatically clear when finished.	0
8	R/W	DMA Read Request bit 0 : DMA Read Request Clear 1 : DMA Read Request If the bit is set, DMA Transfer is stated, and automatically clear when finished.	0
7	R/W	Busy End Interrupt Enable bit 0 : Interrupt Disable 1 : Interrupt Enable	0
6	R/W	DMA Clear Interrupt Enable bit 0 : Interrupt Disable 1 : Interrupt Enable	0
5	R/W	BCH ECC Decoding Done Interrupt Enable bit 0 : Interrupt Disable 1 : Interrupt Enable	0
4	R/W	Auto ECC Done Interrupt Enable bit 0 : Interrupt Disable 1 : Interrupt Enable	0
3:0	R/W	Reserved	0

13.4.2 NAND Flash Memory Command Set Register (NFCMD)

Address: 0xA000_0C04

Bit	R/W	Description	Default Value
7 : 0	R/W	NAND Flash Memory Command	00h

13.4.3 NAND Flash Memory Address Register (NFADR)

Address: 0xA000_0C08

Bit	R/W	Description	Default Value
7 : 0	R/W	NAND Flash Memory Address	00h

13.4.4 NAND Flash Memory Data Register (NFDATA)

Address: 0xA000_0C0C

Bit	R/W	Description	Default Value
31 : 0	R/W	NAND Flash Memory Read/Program Data 32/16/8-bit accessible	0000_0000h

13.4.5 NAND Flash Memory Operation Status Register (NFSTAT)

Address: 0xA000_0C14

Bit	R/W	Description	Default Value
16:12	R	Error bit count The number of Error bit when ECC is finished.	0
11	R	Read data not FF Flag After erase, this bit is used for check all data for NAND Flash is 0xFF. If the read data is not 0xFF, this bit is set to 1. After read the register, this bit is cleared.	0
10	R	Reserved	-
9	R	DMA Write Done It is set when DMA Write is finished. After read the register, this bit is cleared.	0
8	R	DMA Read Done It is set when DMA Read is finished. After read the register, this bit is cleared.	0
7	R	BCH Decoding Done Status It is set when ECC Decoding is finished. After read the register, this bit is cleared.	0
6 : 4	R	Reserved	-
3	R	BCH Decoding Result 0 : Decoding Fail 1 : Decoding Success	0
2	R	Auto ECC Done bit If the value of the bit is set, it indicates Auto ECC is finished. After read the register, this bit is cleared.	0
1	R	NAND Flash Memory nBusy Level 0 : Busy 1 : Ready	nBUSY Level
0	R	NAND Flash Memory Busyx Rising Edge Status If Ready/Busyx signal changes low to high, this bit is set to 1. After read the register, this bit is	0

		cleared.	

13.4.6 NAND Flash Memory ECC(Error Correction Code) Register (NFECC)

Address: 0xA000_0C18

Bit	*R/W*	*Description*	*Default Value*
23 : 16	R/Clear	ECC2 (~P4, ~P4', ~P2, ~P2', ~P1, ~P1', ~P2048, ~P2048')	FFh
15 : 8	R/Clear	ECC1 (~P1024, ~P1024', ~P512, ~P512', ~P256, ~P256', ~P128, ~P128')	FFh
7 : 0	R/Clear	ECC0 (~P64, ~P64', ~P32, ~P32', ~P16, ~P16', ~P8, ~P8')	FFh

******* P1~P4 : Column Parity , P8~P2048 : Row Parity

*** ~ : Logically inverse operation

13.4.7 NAND Flash Memory Configuration Register (NFCFG)

Address: 0xA000_0C1C

Bit	R/W	Description	Default Value
20	R/w	Read data Latch timing Adjust bit. Configure as system clock. 0 : Minimum ~ 60Mhz 1 : 40Mhz ~ Maximum	1
19 : 17	R	Reserved	-
16	R/W	NDFL_nCS Control 0 : Chip Enable 1 : Chip Disable	1
15	R	Reserved	-
14 : 12	R/W	Ts : NDFL_ALE/NDFL_CLE Set-up Time 000 : 1 Clock 001 : 2 Clocks 010 : 3 Clocks 011 : 4 Clocks 100 : 5 Clocks 101 : 6 Clocks 110 : 7 Clocks 111 : 8 Clocks	111
11	R	Reserved	-
10 : 8	R/W	Twp : NDFL_nWE Pulse Width 000 : 1 Clock 001 : 2 Clocks 010 : 3 Clocks 011 : 4 Clocks 100 : 5 Clocks 101 : 6 Clocks 110 : 7 Clocks 111 : 8 Clocks	111
7	R	Reserved	-
6 : 4	R/W	Trp : NDFL_nRE Pulse Width 000 : 1 Clock 001 : 2 Clocks 010 : 3 Clocks 011 : 4 Clocks 100 : 5 Clocks 101 : 6 Clocks 110 : 7 Clocks 111 : 8 Clocks	111
3	R	Reserved	-
2 : 0	R/W	Th : NDFL_ALE/ NDFL_CLE/ NDFL_nCS Hold Time 000 : 1 Clock 001 : 2 Clocks 010 : 3 Clocks 011 : 4 Clocks 100 : 5 Clocks 101 : 6 Clocks 110 : 7 Clocks 111 : 8 Clocks	111

13.4.8 NAND Flash Memory ECC Code for LSN data (NFECCL)

Address: 0xA000_0C20

Bit	R/W	Description	Default Value
15 : 8	R	S_ECC1 (1, 1, 1, 1, 1, 1, ~P4_s, ~P4'_s)	FFh
7 : 0	R	S_ECC0 (~P2_s, ~P2'_s, ~P1_s, ~P1'_s, ~P16_s, ~P16'_s, ~P8_s, ~P8'_s)	FFh

*** P1_s~P4_s : Column Parity, P8_s~P16_s : Row Parity

*** ~ : Logically inverse operation

13.4.9 NAND Flash Memory Error Corrected Data Register (NFECD)

Address: 0xA000_0C24

Bit	R/W	Description	Default Value
31 : 0	R	Automatically Error Corrected Data	-

13.4.10 NAND Flash Memory Spare Address Register (NFSPADR)

Address: 0xA000_0C28

Bit	R/W	Description	Default Value
15 : 0	R/W	Spare address to access during Auto ECC	0000h

13.4.11 NAND Flash Memory MLC ECCn Register (NFECCn)

Address: 0xA000_0C2C / 0xA000_0C30 / 0xA000_0C34 / 0xA000_0C38 / 0xA000_0C3C / 0xA000_0C40 / 0xA000_0C44 / 0xA000_0C48 / 0xA000_0C4C / 0xA000_0C50 / 0xA000_0C54

Bit	R/W	Description	Default Value
31 : 0	R	4-bit ECC Parity Value 52-bit parity[31:0] / 52-bit parity[52:32] 24-bit ECC Parity Value 336-bit parity[31:0] , 336-bit parity[63:32], 336-bit parity[95:64] , 336-bit parity[127:96], 336-bit parity[159:128], 336-bit parity[191:160], 336-bit parity[223:192], 336-bit parity[255:224], 336-bit parity[287:256], 336-bit parity[319:288], 336-bit parity[335:320]	0000_0000h

13.4.12 NAND Flash Memory Error Location n Register (NFERRLOCn)

Address: 0xA000_0C58 / 0xA000_0C5C / 0xA000_0C60 / 0xA000_0C64 / 0xA000_0C68 / 0xA000_0C6C / 0xA000_0C70 / 0xA000_0C74 / 0xA000_0C78 / 0xA000_0C7C / 0xA000_0C80 / 0xA000_0C84 / 0xA000_0C88 / 0xA000_0C8C / 0xA000_0C90 / 0xA000_0C94 / 0xA000_0C98 / 0xA000_0C9C / 0xA000_0CA0 / 0xA000_0CA4 / 0xA000_0CA8 / 0xA000_0CAC / 0xA000_0CB0 / 0xA000_0CB4

Bit	R/W	Description	Default Value
10 : 0	R	Error byte location 1^{st}~24^{th}	0000h

13.4.13 NAND Flash Memory Error Pattern n Register (NFERRPTNn)

Address: 0xA000_0CB8 ~ 0xA000_0D14

Bit	R/W	Description	Default Value
7 : 0	R	Error byte pattern 1^{st}~24^{th}	00h

13.4.14 NAND Flash Memory ID Register (NFMID)

Address: 0xA000_0D18

Bit	R/W	Description	Default Value
31 : 0	R	NAND Flash ID	0000_0000h

14 SD HOST CONTROLLER

14.1 Features

- Support SD (ver 2.0) / MMC (ver 3.31) cards
- Provides High Speed (50MHz)
- Supports 1bit/4bit data bus
- Supports DMA Transfer
- Embeds 64 byte FIFO
- 40-bit Command Register
- 136-bit Response Register

14.2 Block Diagram

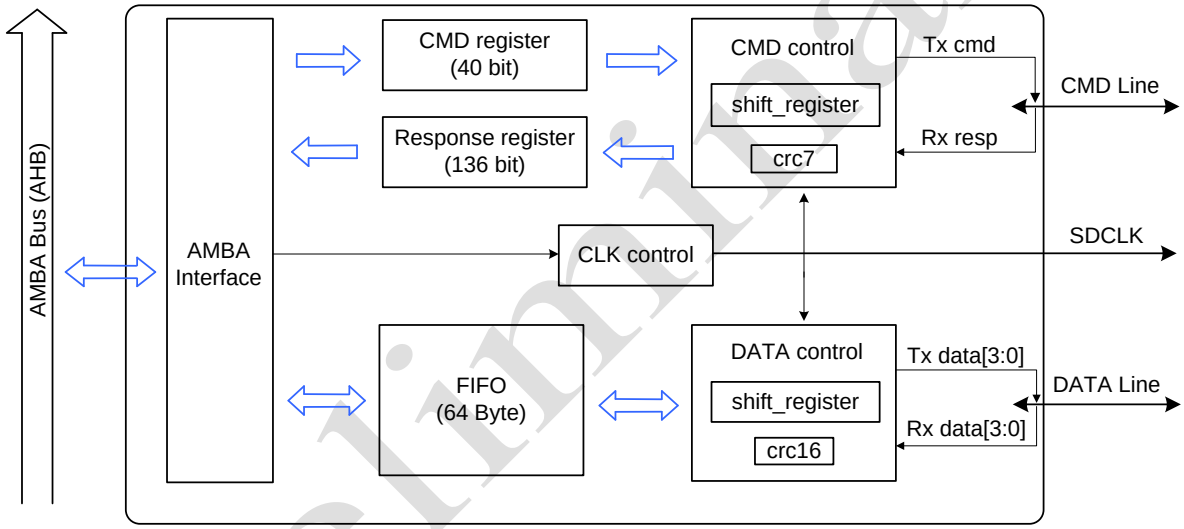


Figure 14-1 SDHC Block Diagram

14.3 SD Card Protocol

Communication between SD card and SD host is started with start bit and is stopped with stop bit based on Command, response, and data.

Command: Host (Controller) sends command line to SD Card. The commands can be categorized as Broadcast command that transfers data to multiple SD card, and Addressed command that transfers data to one SD cared.

Response: A response of host command. The selected SD Card send the response with command line.

Data: The data is sent from SD card to SD card or from SD card to host with Data line in the unit of Block. Generally the block size is 512byte or 1024byte.

For reliability of data transfer, SD Card protocol checks Command, Response, and Data within CRC7 and CRC16. The CRC code generation and error detection is automatically done by H/W.

14.4 Register Description

14.4.1 SDHC Control Register (SDHCCON)

Address : 0xA000_1000h

Bit	R/W	Description	Default Value
31 : 6	R	Reserved	-
5	R/W	MMC/SD HC Enable 0 : Disable (Controller is initialized) 1 : Enable Enable bit for HOST. If this bit is disabled, the status of controller is initialized and inside buffers are cleared.	0b
4 : 3	R/W	Memory access type 00 : byte align 01 : short align 10 : word align 11 : not use This bit determines alignment of data that stored in SD card.	00b
2	R/W	DMA mode selection 0 : Normal mode (data transfer by CPU) 1 : DMA mode (data transfer by DMA) Provides high speed data transfer via DMA.	0b
1	R/W	Bus width Selection 0 : 1bit data bus 1 : 4bit data bus	0b
0	R/W	MMC/SD clock enable 0 : Disable 1 : Enable	0b

14.4.2 SDHC Status Register (SDHCSTAT)

Address: 0xA000_1004h

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15	R	Card_Insertion 0 : No card insertion detection 1 : card insert detected This bit indicates that SD Card is inserted into a slot via Data line [3]. To use the bit, data line[3] should be connected with weak-pull-down resistance.	0b

14	R	Card_Removal 0 : No card removal detection 1 : card remove detected This bit indicates that SD Cared is removed from a slot via Data line [3].	0b
13	R	FIFO full This bit indicates 64-byte data FIFO is full or not.	0b
12	R	FIFO half full This bit indicates 64-byte data FIFO is half full.	0b
11	R	FIFO empty This bit indicates 64-byte data FIFO is empty.	1b
10	R/C	Command & response transaction done 0 : Command and response transaction is in progress 1 : Command and response transaction is done This bit informs that SD card received response when Host sent command. If the response does not reach, this bit is set to 1 by occurring Time out error.	0b
9	R/C	Data Write operation done 0 : Write operation is in progress or incomplete 1 : Write operation complete This bit informs that Data write operation is done. In the case of Data CRC error is occurred, the write operation is finished and then this bit is set to 1.	0b
8	R/C	Read operation done 0 : Read operation is in progress or incomplete 1 : Read operation complete This bit informs that Data write operation is done. In the case of Read Data CRC error is occurred, the read operation is finished and then this bit is set to 1.	0b
7 :6	R/C	Write CRC error code 00 : No CRC Error	00b

		01 : CRC Error (CRC error in data block) 10 : No CRC response (Ignored data block in SD card) 11 : Reserved During write operation, this bit informs CRC test result from SD Card. SD Card test CRC every time when Host sends one block data and send the result of CRC to the Host.	
5	R/C	Response CRC error 0 : No error 1 : Response CRC error occurred This bit informs CRC error occurred in response.	0b
4	R/C	Read data CRC error 0 : No error 1 : Read data CRC error occurred This bit informs that CRC error occured in read data from SD Card.	0b
3	R/C	Write data CRC error 0 : No error 1 : Write data CRC error occurred This bit informs that CRC error occured in write data to SD Card.	0b
2	R/C	Response time out error 0 : No error 1 : Command response was not received in time Specified This bit informs that command response is not received in time.	0b
1	R/C	Read data time out error 0 : No error 1 : The expected data from card was not received in time Specified This bit informs that read data from SD card is not received in time.	0b
0	R	Memory busy state 0 : Memory is ready 1 : Memory is busy This bit indicates busy status of SD Card.	0b

R/C indicates Read/Clear. In order to clear specific bit of status, writes 1 to corresponding bit.

Status [15:8] is an interrupt source. If one of the bits is set to 1, an interrupt is occurred and keeps requesting interrupt until the bit is cleared.

14.4.3 SDHC Clock Divide Register (SDHCCD)

Address : 0xA000_1008h

Bit	R/W	Description	Default Value
31 : 10	R	Reserved.	-
9 : 0	R/W	MMC/SD clock Divide Register $f_{SDCLK} = \frac{f_{AHB\_Clock}}{2 + Divide[9:0]}$	200h

14.4.4 SDHC Response Time Out Register (SDHLCDO)

Address: 0xA000_100Ch

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7 : 0	R/W	Response time out. This register is configured in maximum wait time for response after sending command. If the response does not reach in the specified time, response time out error is occurred. The unit of time is based on the clock of SD Card, and if the last bit of command is transferred, the clock count begins. 01h : 1 clock count 02h : 2 clock counts ... FFh : 255 clock counts	FFh

14.4.5 SDHC Read Data Time Out Register (SDHCRDTO)

Address: 0xA000_1010h

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 8	R/W	Data read time out. This register is configured in maximum wait time for read data after sending read command. User can configure upper 8-bit and lower 8-bit is fixed with 00h. Generally, FF00h is recommended.	FFh
7 : 0	R	Reserved.	00h

14.4.6 SDHC Block Length Register (SDHCBL)

Address: 0xA000_1014h

Bit	R/W	Description	Default Value
31 : 12	R	Reserved	-
11 : 0	R/W	Block length. This register determines the size of data block.	200h

14.4.7 SDHC Number of Block Register (SDHCNOB)

Address: 0xA000_1018h

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 0	R/W	This register specifies the number of blocks to transfer when using Multi-block command. Its value is decreased when one block is transferred and if the data transfer is finished, the value becomes 0.	0000h

14.4.8 SDHC Interrupt Enable Register (SDHCIE)

Address : 0xA000_101Ch

Bit	R/W	Description	Default Value
31 : 8		Reserved	-
7	R/W	Card insert detection Interrupt enable 0 : disable 1 : enable	0b
6	R/W	Card remove detection Interrupt enable 0 : disable 1 : enable	0b
5	R/W	FIFO full Interrupt enable 0 : disable 1 : enable	0b
4	R/W	FIFO half full Interrupt enable 0 : disable 1 : enable	0b
3	R/W	FIFO empty Interrupt enable 0 : disable 1 : enable	0b
2	R/W	End command response Interrupt enable 0 : disable 1 : enable	0b
1	R/W	Write operation done Interrupt enable 0 : disable 1 : enable	0b
0	R/W	Read operation done Interrupt enable 0 : disable 1 : enable	0b

SDHCSTAT [15:8] is an interrupt source, and SDHCIE register is an interrupt enable signal. If an interrupt is occurred, interrupt service routine is executed and sets to 0 in SDHCSTAT [15:8] according to the interrupt source. However, because card insert detection interrupt and card remove detection interrupt are not cleared in SDHCSTAT

[15] and SDHCSTAT [14], interrupt enable bit is set to 0 in the interrupt service routine (Interrupt disable).

14.4.9 SDHC Command Control Register (SDHCCMDCON)

SDHCCMDCON register is used for sending command. Once user writes to SDHCCMDCON register, user command is sent to SD card as the register configuration.

Address: 0xA000_1020h

Bit	R/W	Description	Default Value
31 : 11	R	Reserved	-
10	R/W	This bit determines that a command type needs response or not. In the case of the configuration is No response, response does not be stored into response buffer. 0 : no response 1 : wait response	0b
9 : 8	R/W	This bit determines response type. Because the response type can be changed according to the command, user should select the right response type. 00 : short response (response size : 48bit) 01 : short response with busy (response size : 48bit ,) 10 : long response (response size : 136bit)	00b
7	R/W	This bit determines a command uses data stream or not. In the case of read command or write command, this bit should be 1. 0 : without data 1 : with data	0b
6	R/W	This bit determines a direction of Data FIFO In/Out. In the case of read command, the bit is set to 0. In the case of write command, the bit is set to 1. 0 : read data 1 : write data	0b
5 : 0	R/W	This bit specifies command number. The command number of MMC and SD card is different. Refer to MMC and SD Card specification. 00h = CMD0 01h = CMD1 ... 3Fh = CMD63	00h

14.4.10 SDHC Command Argument Register (SDHCCMDA)

Address: 0xA000_1024h

Bit	R/W	Description	Default Value
31 : 0	R/W	Command argument. It configures argument of command token.	0000 0000h

14.4.11 SDHC Response FIFO Access Register (SDHCRFA)

Address: 0xA000_1028h

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 0	R/W	FIFO size to store response. the size is 8x16 bit.	0000h

14.4.12 SDHC Data FIFO Access Register (SDHCDFA)

Address: 0xA000_102Ch

Bit	R/W	Description	Default Value
31 : 0	R/W	Data FIFO size. (16x32bit)	-

15 USB DEVICE

USB Device of *adStar* supports 2.0 Full-speed (12Mbps) and consists of 5 endpoints.

USB Protocol is supported in hardware, and provides automatically data retry, data toggle, and power management (suspend and resume). The USB device includes PHY.

15.1 Features

- USB 2.0 Full Speed(12Mbps)
- 5 Endpoints
- USB protocol support in hardware
- Provides suspend and resume signaling

Table 15-1 Endpoint List

Endpoint	Max Size (bytes)	Direction	Transaction Type
0	16	IN/OUT	Control
1	64	OUT	Bulk
2	64	IN	Bulk
3	16	OUT	Interrupt
4	16	IN	Interrupt

15.2 Register Summary

Table 15-2 USB Core Register List

Register	Address	R/W	Description	Default Value
USBFA	0xA0001800	R/W	Function address register	0x00
USBPM	0xA0001804	R/W	Power management register	0x00
USBEPI	0xA0001808	R/W	Endpoint interrupt register	0x00
USBINT	0xA0001810	R/W	USB interrupt register	0x00
USBEPIEN	0xA0001814	R/W	Endpoint interrupt enable register	0x1F
USBINTEN	0xA0001818	R/W	USB interrupt enable register	0x04
USBLBFN	0xA000181C	R	Frame number1 register	0x00
USBHBFN	0xA0001820	R	Frame number2 register	0x00
USBIND	0xA0001824	R/W	Index register	0x00
USBMP	0xA0001828	R/W	MAXP register	0x00
USBEP0C	0xA000182C	R/W	EP0 control register	0x00
USBIC1	0xA000182C	R/W	EP2, 4 IN Control register1	0x00
USBIC2	0xA0001830	R/W	EP2, 4 IN Control register2	0x00
USBOC1	0xA0001838	R/W	EP1, 3 OUT Control register 1	0x00
USBOC2	0xA000183C	R/W	EP1, 3 OUT Control register 2	0x00
USBLBOWC	0xA0001840	R	Low Byte OEP Write count register	0x00
USBHBOWC	0xA0001844	R	High Byte OEP write count register	0x00
USBEP0D	0xA0001848	R/W	EP0 FIFO data register	0x00
USBEP1D	0xA000184C	R/W	EP1 FIFO data register	0x0000_0000
USBEP2D	0xA0001850	R/W	EP2 FIFO data register	0x0000_0000
USBEP3D	0xA0001854	R/W	EP3 FIFO data register	0x00
USBEP4D	0xA0001858	R/W	EP4 FIFO data register	0x00

15.2.1 USB Function Address Register

USBFAR register holds USB Device address that is assigned by host. MCU stores the data to the register by executing SET_ADDRESS Descript. This value is used for next token.

15.2.2 USB Power Management Register

Power management register is used by Suspend, Resume and Reset signals. Statuses of Suspend and Reset are stored into USB_INTERRUPT register.

15.2.3 USB Interrupt Registers

This register informs statuses of USB Host request and Endpoint..

15.2.4 USB Interrupt Enable Registers

Interrupt enables of each endpoint. Most of interrupts are enabled initially, but suspend interrupt is disabled.

15.2.5 Frame Number Registers

This register holds frame number at the end of frame packet.

15.2.6 Index Register

The index register is used for selecting control register of each endpoint.

15.2.7 MAXP Register

User can configure FIFO size that is times of 8byte. However, user cannot set larger the FIFO size than maximum FIFO size that is provided by each endpoint.

15.2.8 EP0 Control Register

This register represents control and status of Endpoint0.

15.2.9 IN Control Registers

This register represents control and status of IN Endpoint

15.2.10 Out Control Registers

This register represents control and status of OUT Endpoint

15.2.11 Out Write Count Registers

The 2 Out Write Count registers hold write count. The registers hold the number of packets that are used by MCU, if OPOPR bit is set at the OUT endpoint.

15.2.12 Endpoint FIFO Access Registers

The register accesses to an Endpoint FIFO..

15.3 Register Description

15.3.1 USB Function Address Register (USBFA)

Address : 0xA000_1800h

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 8			Reserved	
7	R/W	R/ Clear	ADDUP: ADDR_UPDATE bit. The MCU sets this bit whenever it updates the FUNCTION_ADDR field in this register. The FUNCTION_ADDR field is used after the Status phase of a Control transfer, which is signaled by the clearing of the DATA_END bit in the Endpoint 0 CSR.	0
6 : 0	R/W	R	FUNADD: FUNCTION_ADDR bits. MCU writes address into this bit.	0

15.3.2 USB Power Management Register (USBPM)

Address : 0xA000_1804h

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 4			Reserved	
3	R	Set	UBRST: USB_RESET bit. If USB receives Reset signal from host, USB sets this bit. If the Reset signal remains in bus, this bit keeps holding 1.	0
2	W/R	R	UBRSUM: USB_RESUME bit. In order to initialize Resume signal, MCU configures this bit during 10ms (Max 15ms). In the Suspend mode, USB generates Resume signal during this bit is set.	0
1	R	R/W	UBSPDMOD: SUSPEND_MODE bit. USB configures this bit when enters into Suspend mode. This bit is cleared by following conditions. - MCU clears MCU_RESUME to finish Resume signal. - MCU reads interrupt register 3 when USB_RESUME interrupt is occurred.	0
0	R/W	R	UBENSPD : ENABLE_SUSPEND bit = 1 Enable Suspend mode = 0 Disable Suspend mode (Default) If this bit is set to 0, USB Device does not enter suspend mode.	0

15.3.3 USB Endpoint Interrupt Register (USBEPI)

Address : 0xA000_1808h

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 5			Reserved	
4	R/ Clear	Set	EP4INT: EP4 Interrupt bit. (Interrupt in mode) This bit is for Endpoint4 interrupt. (Refer to USBIC1R, USBIC2R bit) - When ICIPR(In Control 1 In Packet Ready bit) bit is cleared - When FIFO is flushed. - When ICSTSTAL (In Control 1 Sent Stall bit) bit is set.	0
3	R/ Clear	Set	EP3INT: EP3 Interrupt bit. (Interrupt out mode) This bit is for Endpoint3 interrupt. (Refer to USBOC1R, USBOC2R bit) - When OCOPR (Out Control 1 Out Packet Ready bit) bit is set. - When OCSTSTAL (Out Control 1 Sent Stall bit) bit is set.	0
2	R/ Clear	Set	EP2INT: EP2 Interrupt bit. (Bulk in mode) This bit is for Endpoint2 interrupt. (Refer to USBIC1R, USBIC2R bit) - When ICIPR (In Control 1 In Packet Ready bit) bit is clear. - When FIFO is flushed. - When ICSTSTAL (In Control 1 Sent Stall bit) bit is set.	0
1	R/ Clear	Set	EP1INT: EP1 Interrupt bit. (Bulk out mode) This bit is for Endpoint1 interrupt. (Refer to USBOC1R, USBOC2R bit) - When OCOPR (Out Control 1 Out Packet Ready bit) bit is set. - When OCSTSTAL (Out Control 1 Sent Stall bit) bit is set.	0
0	R/ Clear	Set	EP0INT: EP0 Interrupt bit. (Control mode) This bit is for Endpoint0 interrupt. (Refer to USBEP0CR bit) - EP0OPR bit is set. - EP0IPR bit is cleared - EP0STSTAL bit is set - EP0STED bit is set - EP0DED bit is cleared(Indicates End of control transfer)	0

15.3.4 USB Interrupt Register (USBINT)

Address : 0xA000_1810h

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 3			Reserved	
2	R/ Clear	Set	RSTINT: USB Reset Interrupt bit. USB set this bit when receives Reset signal.	0
1	R/ Clear	Set	RSUMINT: Resume Interrupt bit. In the suspend mode, USB set this bit when receives Resume signal. If the resume is caused by USB Reset, MCU interrupt is occurred by Resume interrupt. If clock continues to operate and duration of SE0 status is 3ms, then USB Reset interrupt is occurred.	0
0	R/ Clear	Set	SPDINT : Suspend Interrupt bit USB sets this bit when receive suspend signal. If there are no operations in bus during 3ms, this bit is set. Therefore, if the MCU does not stop Clock after the first suspend interrupt, the interrupt is occurred every 3ms. The default value of this interrupt is disable.	0

15.3.5 Endpoint Interrupt Enable Register (USBEPIEN)

Address : 0xA000_1814h

Bit	R/W	Description	Default Value
4	R/W	EP4INTEN : Endpoint 4 Interrupt enable bit	1
3	R/W	EP3INTEN : Endpoint 3 Interrupt enable bit	1
2	R/W	EP2INTEN : Endpoint 2 Interrupt enable bit	1
1	R/W	EP1INTEN : Endpoint 1 Interrupt enable bit	1
0	R/W	EP0INTEN : Endpoint 0 Interrupt enable bit	1

15.3.6 USB Interrupt Enable Register (USBINTEN)

Address : 0xA000_1818h

Bit	R/W	Description	Default Value
31 : 3	R	Reserved	
2	R/W	RSTINTEN : USB RESET Interrupt enable bit	1
1	R	Reserved	
0	R/W	SPDINTEN : SUSPEND Interrupt enable bit	0

15.3.7 USB Low Byte Frame Number Register (USBLBFN)

Address : 0xA000_181Ch

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R/W	Frame Number 1 register	0x00

15.3.8 USB High Byte Frame Number Register (USBHBFN)

Address : 0xA000_1820h

Bit	*R/W*	*Description*	*Default Value*
31 : 8	R	Reserved	
7 : 0	R/W	Frame Number 2 register	0x00

15.3.9 USB Index Register (USBIND)

Address : 0xA000_1824h

Bit	*R/W*	*Description*	*Default Value*
31 : 3	R	Reserved	
2 : 0	R/W	Index register 000 : Endpoint 0 001 : Endpoint 1 010 : Endpoint 2 011 : Endpoint 3 100 : Endpoint 4 101 : Reserved 110 : Reserved 111 : Reserved	000

15.3.10 USB MAXP Register (USBMP)

Address : 0xA000_1828h

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R/W	Max FIFO Size 0000_0001 MAXP=8 0000_0010 MAXP=16 0000_0100 MAXP=32 0000_1000 MAXP=64	0x00

15.3.11 USB EP0 Control Register (USBEP0C)

Address : 0xA000_182Ch

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 8	R		Reserved	
7	Clear		EP0SUEC : EP0 Set Up End Clear bit. MCU write 1 to this bit in order to clear EP0STED bit.	0
6	Clear		EP0OPRC : EP0 Out Packet Ready Clear bit. MCU write 1 to this bit in order to clear EP0OPR bit.	0
5	Set	Clear	EP0SDSTAL: EP0 Send Stall bit. If the MCU recognizes the token is wrong, the MCU clears EP0OPR bit and sets this bit. USB generates STALL handshake to current control transfer. MCU write 0 in order to finish STALL.	0
4	R	Set	EP0STED: EP0 Setup End bit. Read Only bit. If control transfer is finished before set the EP0DED bit, USB set this bit. When USB sets this bit, MCU receives interrupt. In this case, USB flushed FIFO, and invalidates FIFO access from MCU. If the FIFO access is validated, this bit is cleared.	0
3	Set/R	Clear	EP0DED: EP0 Data End bit. MCU sets this bit at following conditions. - EP0OPR bit is cleared after takes the last data packet. - EP0OPR bit is cleared and EP0IPR is set in Zero length data phase. - MCU sets EP0IPR bit and this bit (EP0DED) after MCU loads packet data from FIFO.	0
2	Clear /R	Set	EP0STSTAL: Sent Stall bit. If control transaction is finished by protocol error, USB set this bit. If this bit is set, interrupt is occurred.	0

1	Set/R	Clear	EP0IPR: EP0 In Packet Ready bit. MCU set this bit after writes data into Endpoint0 FIFO. If the data packet is transferred to host successfully, USB clears this bit. If USB clears this bit, interrupt is occurred. Therefore, MCU can keep loading the next data. MCU set EP0IPR and EP0DED in Zero length data phase at the same time.	0
0	R	Set	EP0OPR: EP0 Out Packet Ready bit. Read only. if valid token is written in FIFO, USB set this bit. USB sets this bit, interrupt is occurred. By writing value 1 to EP0OPRC, MCU clears this bit.	0

15.3.12 USB IN Control 1 Register (USBIC1)

Address : 0xA000_182Ch

Bit	*R/W*		*Description*	*Default Value*
	MCU	*USB*		
31 : 7	R		Reserved	
6	Set	R/Clear	ICCDT: In Control 1 Clear Data Toggle bit. Write Only. If MCU writes 1 to this bit, data toggle bit is cleared.	0
5	R/ Clear	Set	ICSTSTAL: In Control 1 Sent Stall bit. Because MCU sets ICSDSTAL bit, STALL handshake is occurred in the In token. At the time, USB sets this bit. If USB generates STALL handshake, ICIPR bit is cleared. By writing 0, this bit is cleared.	0
4	R/W	R	ICSDSTAL: In Control 1 Send Stall bit. In order to generate STALL handshake to USB, MCU writes 1 to this bit. To finish the STALL, MCU clears this bit.	0
3	R/Set	Clear	ICFFLU: In Control 1 FIFO Flush bit. In order to flush IN FIFO, MCU set this bit. If FIFO is flushed, this bit is cleared by USB. In this circumstance, interrupt is occurred. If a token is processing, USB waits for finish the data transfer. If two packets are loaded into FIFO, the first packet (that will be sent to host) is flushed and the corresponding ICIPR bit is cleared.	0
2			Reserved	0
1	R	Set	ICFNE: In Control 1 FIFO Not Empty bit. This bit represents that FIFO contains at most 1 data packet. 0: No packet inside FIFO.	0

			1: The FIFO holds packets.	
0	Set / R	Clear	ICIPR: In Control 1 In Packet Ready bit. After write data to FIFO, MCU set this bit. If data packet transfer is success, USB clears this bit. If USB clears this bit, interrupt is occurred, and MCU can load the next packet. During this bit is set, MCU cannot write FIFO. If MCU set ICSDSTAL, this bit cannot be set.	0

15.3.13 USB IN Control 2 Register (USBIC2)

Address : 0xA000_1830h

Bit	*R/W*		*Description*	*Default Value*
	MCU	*USB*		
31 : 8	R		Reserved	
7	R/W	R	ICASET: In Control 2 Auto Set bit. If this bit is set, MCU set ICIPR bit automatically when MCU writes data as MAXP. In the case of write smaller size data than XAXP, MCU should set ICIPR bit.	0
6			Reserved	0
5	R/W	R	ICMODIN: In Control 2 Mode In bit. With this bit, the direction of Endpoint can be programmable. 1 = In Endpoint 0 = Out Endpoint	1
4 : 0			Reserved	

15.3.14 USB Out Control Register 1 (USBOC1)

Address : 0xA000_1838h

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 8	R		Reserved	
7	R/W	R	OCCDT: Out Control 1 Clear Data Toggle bit. If MCU write 1 to this bit, data toggle sequence bit is reset to DATA0.	0
6	Clear/ R	Set	OCSTSTAL: Out Control 1 Sent Stall bit. When OUT token is finished by the STALL handshake, USB set this bit. If OUT Token sends larger size of data than MAXP, USB generates STALL handshake to host. If MCU writes 0, this bit is cleared.	0
5	W/R	R	OCSDSTAL: Out Control 1 Send Stall bit. MCU writes 1 to this bit in order to generate STALL handshake to USB. In order to finish the STALL status, MCU write 0 into this bit.	0
4	R/W	Clear	OCFFLU: Out Control 1 FIFO Flush bit. MCU writes 1 to this bit in order to flush FIFO and write 0 to stop. Only during OCOPR bit is set, this bit can be set. Data packet that is taken by MCU will be flushed.	0
3	R	R/W	OCERR : Out Control 1 Data Error bit This bit represents that there are errors (bit stuffing or CRC) in received data. This bit is cleared automatically when OCOPR bit is cleared.	0
2	R	R	Reserved	
1	R	R/W	OCFFUL: Out Control 1 FIFO Full bit. This bit represents that FIFO is Full. 0: FIFO is not full. 1: FIFO is full.	0
0	R/ Clear	Set	OCOPR: Out Control 1 Out Packet Ready bit. When data packet is loaded into FIFO, USB set this bit. After MCU reads entire packet, this bit should be cleared by MCU. MCU write 0 to this bit in order to clear.	0

15.3.15 USB OUT Control Register 2 (USBOC2)

Address : 0xA000_183Ch

Bit	R/W		Description	Default Value
	MCU	USB		
31 : 8	R		Reserved	
7	R/W	R	OCACLR: Out Control 2 Auto Clear bit. If this bit is set, whenever MCU reads data from OUT FIFO, OCOPR bit is cleared automatically by USB core.	0
6 : 0			Reserved	0

15.3.16 USB Low Byte Out Write Count Register (USBLOWC)

Address : 0xA000_1840h

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R/W	(LBOWC) Low Byte OEP write count register	0x00

15.3.17 USB High Byte Out Write Count Register (USBHBOWC)

Address : 0xA000_1844h

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	
7 : 0	R/W	(HBOWC) High Byte OEP write count register	0x00

15.3.18 EP0 FIFO Data Register (USBEP0)

Address : 0xA000_1848h

Bit	*R/W*	*Description*	*Default Value*
7 : 0	R/W	EP0 FIFO Data Register	0x00

15.3.19 EP1 FIFO Data Register (USBEP1)

Address : 0xA000_184Ch

Bit	*R/W*	*Description*	*Default Value*
31 : 0	R/W	EP1 FIFO Data Register	0x00

15.3.20 EP2 FIFO Data Register (USBEP2)

Address : 0xA000_1850h

Bit	*R/W*	*Description*	*Default Value*
31 : 0	R/W	EP2 FIFO Data Register	0x00

15.3.21 EP3 FIFO Data Register (USBEP3)

Address : 0xA000_1854h

Bit	*R/W*	*Description*	*Default Value*
7 : 0	R/W	EP3 FIFO Data Register	0x00

15.3.22 EP4 FIFO Data Register (USBEP4)

Address : 0xA000_1858h

Bit	*R/W*	*Description*	*Default Value*
7 : 0	R/W	EP4 FIFO Data Register	0x00

16 LCD CONTROLLER

16.1 Features

- Supports displays resolutions up to 800 x 600
- 256 x 32 FIFO controls in LCDC block.
- Internal Color Bar Generator
- Programmable Horizontal, Vertical and Field Input Sync. Phase.
- Programmable Horizontal, Vertical Sync. and Blank Output Signal Timing and Phase

16.2 Register Description

LCD Controller Register Summary

Address	*Register Name*	*Description*
0x8002_2404H	LCD HORIZONTAL TOTAL REGISTER (LCDHT)	Horizontal Total Scan Value including horizontal active and black section
0x8002_2408H	LCD HORIZONTAL SYNC. START / END REGISTER (LCDHS)	Start(End) value in Horizontal Sync section
0x8002_240CH	LCD HORIZONTAL ACTIVE START / END REGISTER (LCDHA)	Start(End) value in Horizontal active section
0x8002_2410H	LCD VERTICAL TOTAL REGISTER (LCDVT)	Vertical Total scan value including Vertical Active and blank section
0x8002_2414h	LCD VERTICAL SYNC. START/END REGISTER (LCDVS)	Start(End) value of Vertical Sync section
0x8002_2418h	LCD VERTICAL ACTIVE START/END REGISTER (LCDVA)	Start(End) value of Vertical active section
0x8002_241Ch	LCD DISPLAY CURRENT X / Y POSITION REGISTER (LCDXY)	Horizontal/Vertical Counter value
0x8002_2420h	LCD STATUS REGISTER (LCDSTAT)	Sync status of LCD controller
0x8002_2424h	LCD CONTROL REGISTER (LCDCON)	Controls display, sync, memory, and FIFO mode of LCD
0x8002_2428h	LCD OVERLAY & DAC CONTROL REGISTER (LCDOEDAC)	Overlay / DAC control
0x8002_242Ch	LCD VESA POWER MANAGEMENT REGISTER (LCDPM)	VESA Display Power Management System (DPMS) control
0x8002_2430h	LCDC BASE ADDRESS 0	Designate the start point of screen
0x8002_2434h	LCDC BASE ADDRESS 1	Designate the start point of screen
0x8002_2438h	LCDC FRAME SYNC. COUNTER	Count the number of frame syncs.
0x8002_243Ch	LCD HORIZONTAL WIDTH	Decide the LCD's horizontal width
0x8002_2440h	LCD FLIP COMMAND	Process flip operation

Table 16-1 LCD Controller Registers Table

16.2.1 LCD Base Address Register(LCDBA)

Address : 0x8002_2400h

Bit	R/W	Description	Default Value
31 : 21	R	Reserved	-
20 : 0	R/W	Base Address These bits indicates the start position of the screen in the memory	00 0000h

16.2.2 LCD Horizontal Total Register(LCDHT)

Horizontal total scan value including horizontal active and blank section.

Address : 0x8002_2404h

Bit	R/W	Description	Default Value
31 : 11	R	Reserved	-
10 : 0	R/W	Horizontal Total The value loaded into this field is the total pixel counts per line.	000h

16.2.3 LCD Horizontal Sync. Start / End Register(LCDHS)

Start(End) value of horizontal sync section.

Address : 0x8002_2408h

Bit	R/W	Description	Default Value
31 : 27	R	Reserved	-
26 : 16	R/W	Horizontal Sync Start The value loaded into this field is the value of horizontal sync period start by the horizontal counter	000h
15 : 11	R	Reserved	-
10 : 0	R/W	Horizontal Sync End The value loaded into this field is the value of horizontal sync period end by the horizontal counter	000h

16.2.4 LCD Horizontal Active Start / End Register(LCDHA)

Start(End) value of horizontal active section.

Address : 0x8002_240Ch

Bit	R/W	Description	Default Value
31 : 27	R	Reserved	-
26 : 16	R/W	Horizontal Active Start The value loaded into this field is the value of horizontal active period start by the horizontal counter	000h
15 : 11	R	Reserved	-
10 : 0	R/W	Horizontal Active End The value loaded into this field is the value of horizontal active period start by the horizontal counter	000h

16.2.5 LCD Vertical Total Register(LCDVT)

Vertical total scan value including vertical active and blank section.

Address : 0x8002_2410h

Bit	R/W	Description	Default Value
31 : 11	R	Reserved	-
10 : 0	R/W	Vertical Total The value loaded into this field is the value of the total vertical line counts.	000h

16.2.6 LCD Vertical Sync. Start / End Register(LCDVS)

Start(End) value of vertical Sync section.

Address : 0x8002_2414h

Bit	R/W	Description	Default Value
31 : 27	R	Reserved	-
26 : 16	R/W	Vertical Sync Start The value loaded into this field is the value of vertical sync period start by the vertical counter	000h
15 : 11	R	Reserved	-
10 : 0	R/W	Vertical Sync end The value loaded into this field is the value of vertical sync period end by the vertical counter	000h

16.2.7 LCD Vertical Active Start / End Register(LCDVA)

Start(End) value of Vertical Active section.

Address : 0x8002_2418h

Bit	R/W	Description	Default Value
31 : 27	R	Reserved	-
26 : 16	R/W	Vertical Active Start The value loaded into this field is the value of vertical active period start by the vertical counter	000h
15 : 11	R	Reserved	-
10 : 0	R/W	Vertical Active end The value loaded into this field is the value of vertical active period end by the vertical counter	000h

16.2.8 LCD Display Current X / Y Position Register(LCDXY)

Display current X position register is read-only, and represent the horizontal counter value. Display current Y position register is also read-only, and represent the vertical counter value.

Address : 0x8002_241Ch

Bit	R/W	Description	Default Value
31 : 27	R	Reserved	-
26 : 16	R	The value loaded into this field is the value of the vertical counter.	000h
15 : 11	R	Reserved	-
10 : 0	R	The value loaded into this field is the value of the horizontal counter.	000h

16.2.9 LCD Status Register(LCDSTAT)

LCD status register is read-only. It shows the sync status of LCD controller. Both horizontal sync and vertical sync signal have low active status when control register [21:20] bits are "00". However, both horizontal and vertical active signal have high active status regardless of control register [21:20] value.

Address : 0x8002_2420h

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	R	External Sync. Detect	0b
6 : 5	R	Current Display Bank	00b
4	R	Field (1 : ODD Field, 0 : EVEN Field)	1b
3	R	Vertical Active (active high)	0b
2	R	Vertical Sync	1b
1	R	Horizontal Active (active high) .	0b
0	R	Horizontal Sync	1b

16.2.10 LCD Control Register(LCDCON)

LCD control register is used to control the operation mode of LCDC

* Frame Memory Bank <n> Ping-Pone Enable
: Activate/deactivate the frame memory bank switches due to graphic engine flip command
- When deactivated, LCD Frame Memory Bank is fixed
- When activated, LCD frame memory bank is switched by graphic engine flip command
(For more detailed information, reference to the explanation of CSC image capture control register bit "0")

* Vertical Double Scan
: Display twice a line in vertical direction

* Horizontal Double Scan
: Display twice a pixel in horizontal direction

Address : 0x8002_2424h

Bit	R/W	Description	Default Value
31 : 25	R	Reserved	-
24	R/W	Software Reset. : 0 = Normal operation 1=Reset,.	1b
23	R	Reserved	-
22	R/W	DOT CLOCK SELECT : 0 = NORMAL 1 = INVERTED	
21	R/W	HSYNC. Output Polarity. : 0 = LOW ACTIVE 1 = HIGH ACTIVE	0b
20	R/W	VSYNC. Output Polarity. : 0 = LOW ACTIVE 1 = HIGH ACTIVE	0b
19	R/W	Frame Memory Bank <n> Ping-Pong Enable. : 0 = Disable 1 = Enable	0b
18 : 17	R/W	FIFO Request Control(Total depth : 256) 00 : one half request(128) 01 : one fourth request(64) 10 : one eighth request(32) 11 : Don't use	00b
16 : 15	R	Reserved	0b
14	R/W	WHEN RGB 32BIT MODE, INPUT DATA SEQUENCE : 0 = dRGB 1 = RGBd	0b
13 : 12	R/W	Input Source Format : 00 = YCbCr422 : 01 = RGB 16bit : 10 = RGB 32bit	0b
11 : 4	R	Reserved	0b
3	R/W	Vertical Double Scan Enable. : 0 = Disable 1 = Enable	0b
2	R/W	Horizontal Double Scan Enable. : 0 = Disable 1 = Enable	0b
1 : 0	R/W	Screen Display Mode Control. : 00=Normal operation. : 01=Regular Pattern Generation : 1x=Screen off	00b

16.2.11 LCD Overlay & DAC Control Register(LCDOEDAC)

Address : 0x8002_2428h

Bit	R/W	Description	Default Value
31 : 24	R/W	Reserved	-
23 : 16	R/W	Contrast Control FFh : Bright 80h : Default 00h : Dark	80h
15 : 8	R	Reserved	-
7 : 0	R/W	Brightness Control FFh : Maximum Contrast 80h : Default 00h : Minimum Contrast	80h

16.2.12 LCD VESA Power Management Control Register(LCDPM)

Address : 0x8002_242Ch

Bit	R/W	Description	Default Value
31 : 2	R	Reserved	-
1 : 0	R/W	VESA Power Management Control.	00b

1:0	Stage	Vsync.	Hsync.
00	On	On	On
10	Stand-by	On	Off
10	Suspend	Off	On
11	Off	Off	Off

16.2.13 LCD Base Address n Register (LCDBARn)

Address : 0x8002_2430h / 0x8002_2434h

Bit	R/W	Description	Default Value
31 : 19	R/W	Base Address n Only SDRAM area is available	0000h
18 : 0	R	Reserved	-

16.2.14 LCD Frame Sync. Count Register (LCDFRAMECNT)

Address : 0x8002_2438h

Bit	R/W	Description	Default Value
31 : 0	R/W	Frame Sync. Count	0h

16.2.15 LCD Horizontal Width Register (LCDHWIDTH)

Address : 0x8002_243Ch

Bit	R/W	Description	Default Value
31 : 12	R	Reserved	-
11 : 0	R/W	Horizontal Width	400h

16.2.16 LCD Horizontal Width Register (LCDFCTL)

Address : 0x8002_2440h

Bit	R/W	Description	Default Value
31 : 4	R	Reserved	-
3	R	BANK1 -> BANK0 completed	0
2	R	BANK0 -> BANK1 completed	0
1	R/W	Request change to Bank1	0
0	R/W	Request change to Bank0	0

LCD Controller Block Diagram

LCD Controller is composed of Register, Timing Generation, Address Generation, FIFO Control, Sync Control, Request Generation, and External Sync Detector. Request Generation, Address Generation, and FIFO Control blocks are for reading frame memory data, and Sync Control block is for VGA mode. Timing Generation block manages overall control of timing control.

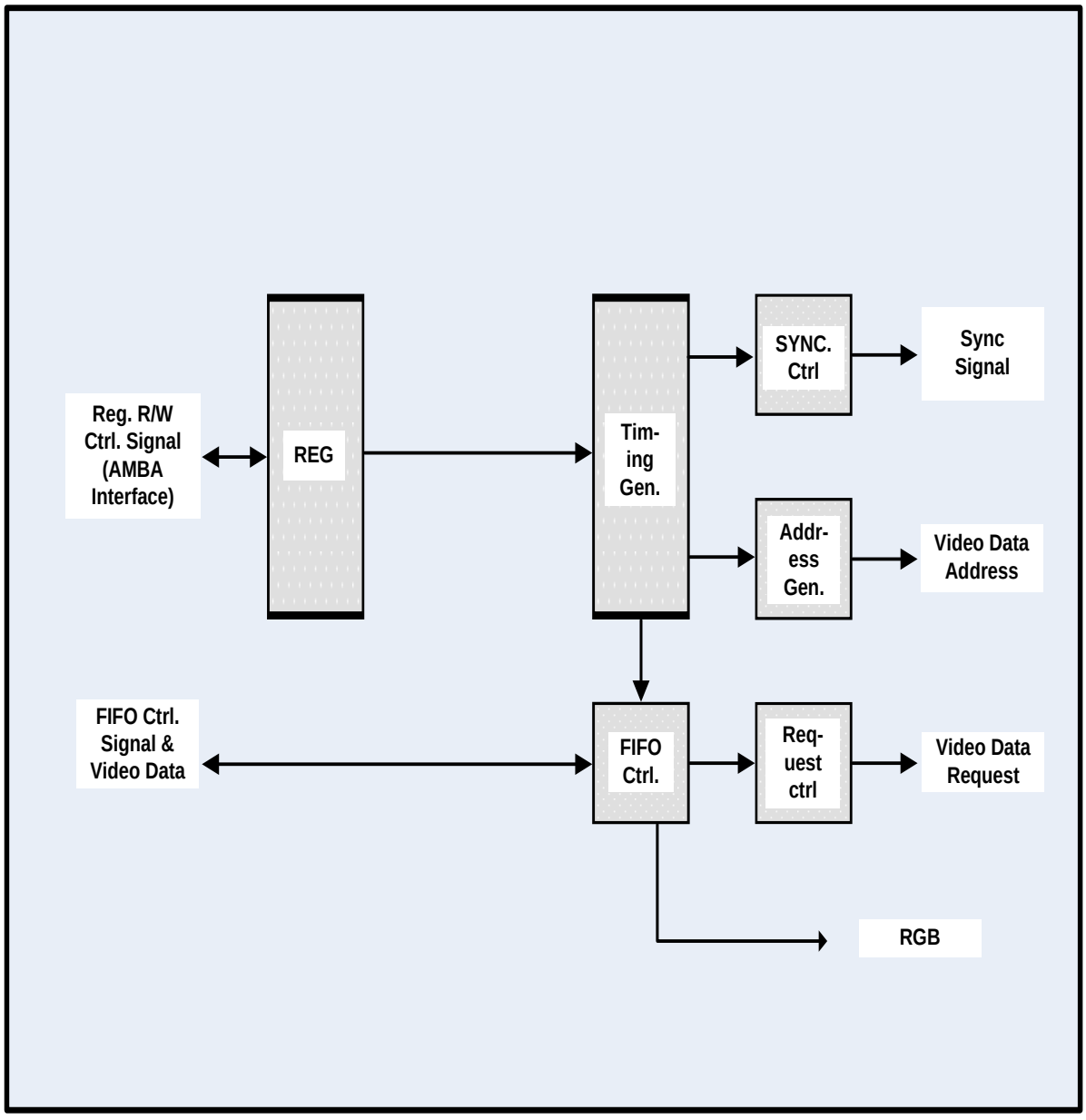


Figure 16-1 LCD Controller Block Diagram

- Address Generation

Address Generation block generates memory read request address for screen refresh. The address is generated by adding internal mode-dependent offset address to user-set LCD base address.

- FIFO / Request Control

FIFO Control block controls read request and read/write pointers of internal FIFO. Read request and read/write pointers are reset at the end of horizontal active section.

FIFO control block has two clock domains: system clock domain for writing data read from frame memory to FIFO and video clock domain for displaying data read from FIFO data on screen.

The write/read data bus of the FIFO is 32bit width. The [16] bit of control register can choose RGB color mode between 16 bits and 24 bits. Initially, it is 16 bit (5:6:5 format) color mode. If 16 bit color mode is chosen, 2 pixels can be processed for one FIFO write/read operation. The 32bit bus can transfer two pixels at a time; lower 16 bits [15:0] are displayed first and higher 16 bits [31:16] later. One pixel is 16bit width; R value is in [15:11] bits, G value is in [10:5] bits, and B value is in [4:0] bits. Otherwise, if 32 bit color mode is chosen, one transfer can deliver only 1 pixel at a time. The bus line utilization of this case is { [31:24] for dummy 8 bits, [23:16] for R value, [15:8] for G value, and [7:0] B value}.

Depending on the [18:17] bits of LCD control register, request signal for frame memory video data reading is generated while checking the FIFO's read pointer on every horizontal active section. If these are "00" or "11", request signal is generated when the half of the FIFO is empty. If these are "01", the signal is generated when the quarter of the FIFO is empty. If these are "10", the signal is generated when one eighth of the FIFO is empty. On horizontal HSYNC section of every line, FIFO is filled depending on [18:17] bits of the LCD control register: full when "00", "11"; half when "01"; quarter when "10". The size of internal FIFO is 256 x 32.

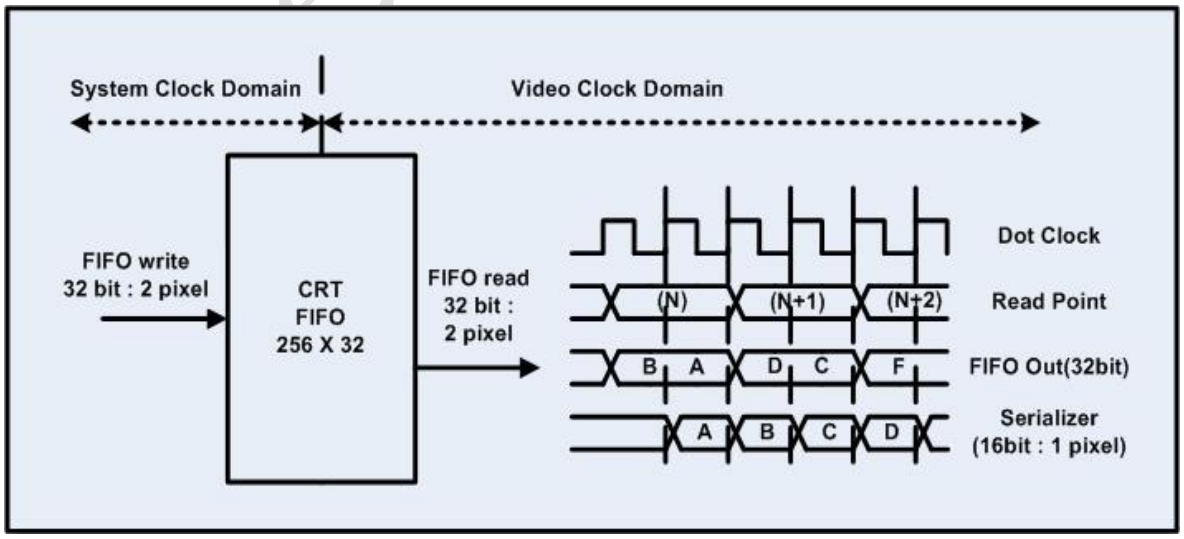


Figure 16-2 LCD FIFO Control Block – RGB 16 Bit(5:6:5) Format Operation

- Sync. Timing Generation

Below diagram shows sync signal timings of 640 by 480 definition depending on Horizontal Total, Sync Start(End), Active Start(End), Vertical Total, Sync Start(End), Active Start(End) register settings. HSYNC and VSYNC signals are low active in default, and [5:4] bits of LCD control register can control their active polarity. Horizontal and vertical active signals are high active.

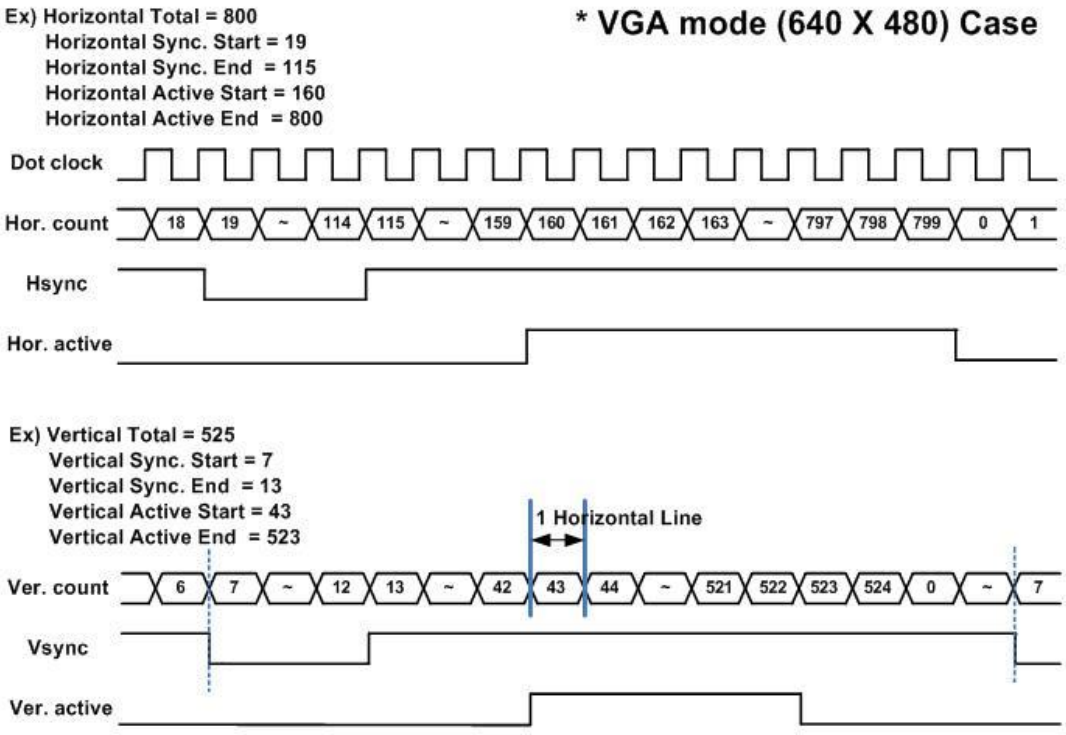


Figure 16-3 LCDC Horizontal, Vertical Sync / Active Signal Timing

- Color Bar Test Pattern Generation Block

Color bar test pattern generation is activated and request generation, address generation, and FIFO control blocks are deactivated when [1:0] bits of LCD control register is "01". Video data mux & serialization block outputs selected color bar pattern video data. Color bar pattern is generated in black, white, yellow, blue-green, green, purple, red, and blue color order from left, and has even distribution regardless of screen definition. If active section is not exact multiple of 8, right side of the screen can have black outputs.

Registers Programming Resolution Reference Table for LCDC

Reg Name	LCDBA	LCDHT	LCDHS	LCDHA	LCDVT	LCDVS	LCDVA	LCDCON
320x240	00000000							
640x480 (800x525)	00000000	00000320	00130073	00A00320	0000020D	0007000D	002B020B	00080000
800x600 (1056x628)	00000000	00000420	002300C3	01000420	00000274	0004000A	001A0272	00080000
NTSC (720x480)	00000000	000006B4	002000A0	011406B4	0000020D	0007000D	002B020B	000820C0
PAL (720x572)	00000000	000006C0	00180098	012006C0	00000271	00010007	002F026B	000820F0

Table 16-2 Registers Programming Resolution Reference Table for LCDC

* Register Values are Hexa-Decimal.
* Memory Read Request is based on half position of FIFO.
* Screen Display Mode is based on Normal operation.
* H(V)SYNC. Output Polarity is based on Low Active.
* H(V)SYNC. Output Select is based on SYNC. Output generated from Internal block

17 TIMERS

adStar includes 4-channel 16-bit timer/counter which support timer/counter, capture, and PWM functions.

17.1 Features

- 15-bit Pre-scale
- 16-bit Timer/Counter
- 16-bit Capture
- 16-bit PWM
- 16-bit Timer Counter Wave-Out

17.2 Function Description

17.2.1 15-bit Pre-scaler with clock source selection

Pre-scaler choose an input source between system clock and external clock with CLKSEL bit. It divides the input source by between 2 and 32768, and transfers the divided clock to timer/counter. Timer/counter receives the divided clock, and runs 32bit counter.

When precise phase of the divided clock is needed, pre-scaler counter should be initilaized by setting CNTCLR bit of TPxCPM register.

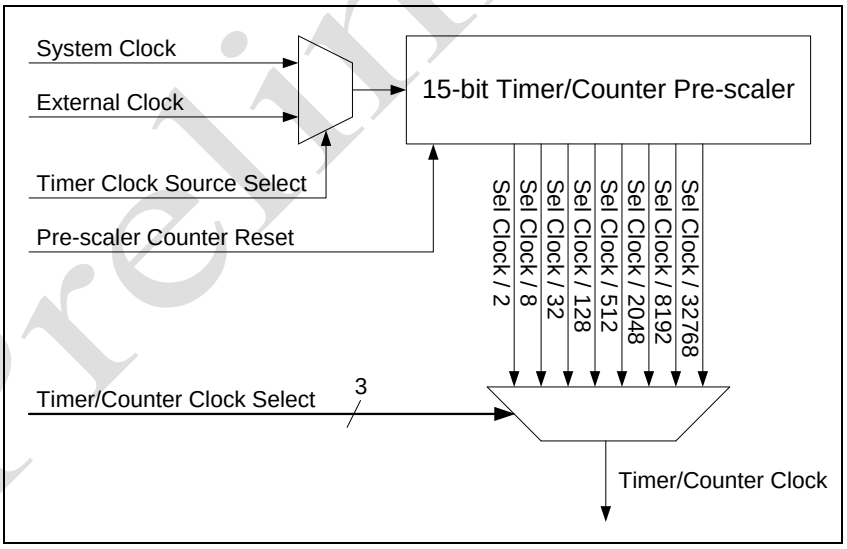


Figure 17-1 Pre-scaler Block Diagram

17.2.2 Timer/Counter

On every cycle of divided clock from pre-scaler, counter value is increment by one from 0x0 until it reaches the user-difined timer counter register value. When reached, the counter value is reset(=0) and interrupt raises.

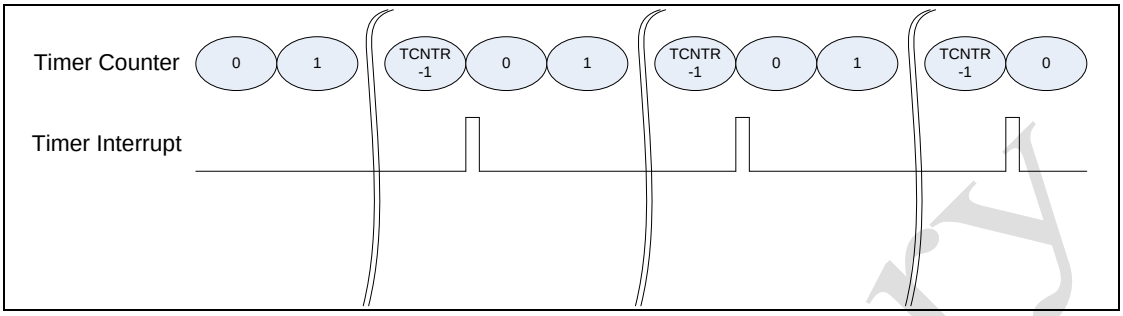


Figure 17-2 Timer Operation

The period of a timer is decided by selected clock, pre-scaler, and timer counter.

$$Timer\ \ Period = \frac{1}{Clock\ \ Source\ \ Frequency} \times \frac{1}{\Pr e-scaler\ \ Factor} \times (TMCNT)\ [\sec] \qquad \{\Pr e-scaler\ \ Factor \geq 3\}$$

$$Timer\ \ Period = \frac{1}{Clock\ \ Source\ \ Frequency} \times \frac{1}{\Pr e-scaler\ \ Factor} \times (TMCNT+1)\ [\sec] \qquad \{\Pr e-scaler\ \ Factor < 3\}$$

Timer Period Example :
- Clock Source Frequency : 12MHz System Clock
- Pre-scaler Factor : 1 / 1024
- Timer Counter Value (TMCNT) : 1000

=> 1/12MHz X 1024 X 1000 = 85.333msec = 11.718Hz

Following registers should be configured to run a timer counter.
- TPxCON : decide the clock input of pre-scaler. Also, it is used to clear pre-scaler.
- TMxCON's TMOD : decides the mode of Timer Counter
- TMxCON's WAVE: decide whether output or not the clock of timer counter period.
- TMxCON's PFSEL: decide the clock to be used for Timer Counter
- TMxCON's TMEN: Enable Timer Counter
- TMxCNT: Decide the maximum counter value of Timer Counter

Following procedure is required to run a Timer Counter.
- Set TPxCON
- Set TMxCNT
- Set TMxCTR
- Set CNTCLR bit of TPxCTRL register if necessary

17.2.3 Pulse Width Modulation (PWM)

PWM is a controller to output pulse signals of programmer-defined duty and period.

PWM references clock generated by pre-scaler, and outputs the wave form of user defined period.

PWM output pulse is toggled whenever its 32bit counter value reaches PWM duty or PWM period register value. The number of outputs is limited by PWM pulse number register. When it reaches the limit, PWM interrupt raises. However, if there is no special hanldler for the interrupt, PWM will output continuously. Thus, timer interrupt should disable PWM to stop PWM pulse.

$$PWM\ \ Pulse\ \ Period = \frac{1}{Clock\ \ Source\ \ Frequency} \times \frac{1}{\Pr e - scaler\ \ Factor} \times (TMCNT)\ [\sec] \qquad \{\Pr e - scaler\ \ Factor \geq 3\}$$

$$PWM\ \ Pulse\ \ Period = \frac{1}{Clock\ \ Source\ \ Frequency} \times \frac{1}{\Pr e - scaler\ \ Factor} \times (TMCNT + 1)\ [\sec] \qquad \{\Pr e - scaler\ \ Factor < 3\}$$

PWM Period Example :
- Clock Source Frequency : 12MHz System Clock
- Pre-scaler Factor : 1 / 1024
- PWM Period Value(TMxCNT) : 10
- PWM Duty Value : 6

=> 1/12MHz X 1024 X 10 = 0.853msec = 1.171KHz

Following registers should be configured to run PWM.
- TPxCTRL: choose clock input of pre-scaler. Also, it can be used to clear pre-scaler.
- TMxCTRL's TMOD: decide PWM mode
- TMxCTRL's PWML: decide start level of PWM output
- TMxCTRL's PFSEL: decide clock of PWM
- TMxCTRL's TMEN: enable PWM
- TMxCNT: decide the period of PWM
- TMxDUT: decide the duty of PWM
- TMxPUL: decide the number of pulse outputs of PWM. If it reaches it limit, timer interrupt raises. However, it doesn't stop PWM pulse output.

Following procedure is required to run PWM.
- Set TPxCTRL
- Set TMxCNT
- Set TMxDUT
- Set TMxPUL
- Set CNTCLR of TPxCTRL register if necessary

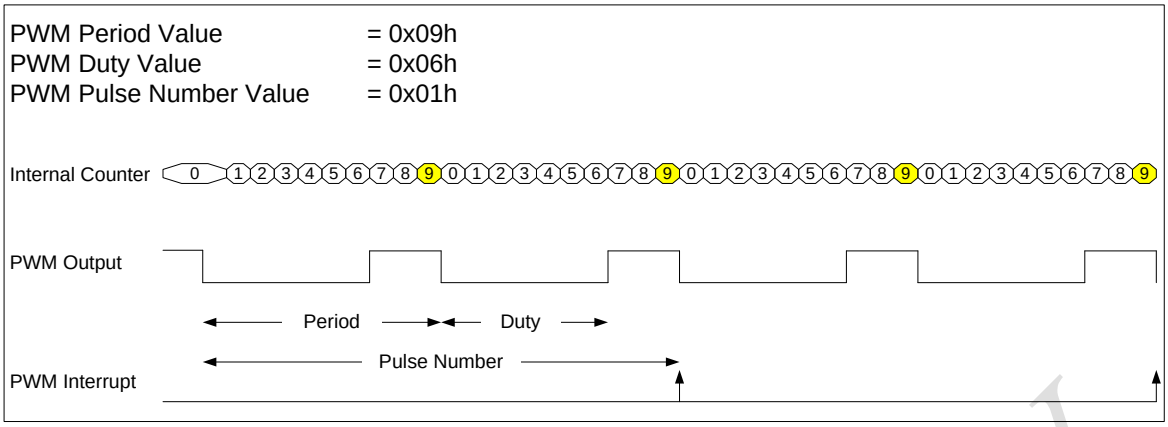


Figure 17-3 PWM Operation

17.2.4 Capture

Capture function measures the external output referencing the clock defined by pre-scaler.

Five kind of external periods can be measured: Low/High pulse, Low Pulse, High Pulse, Falling to Falling Period, Rising to Rising Period.

The first capture after enabling timer should be ignored because it is a transient value.

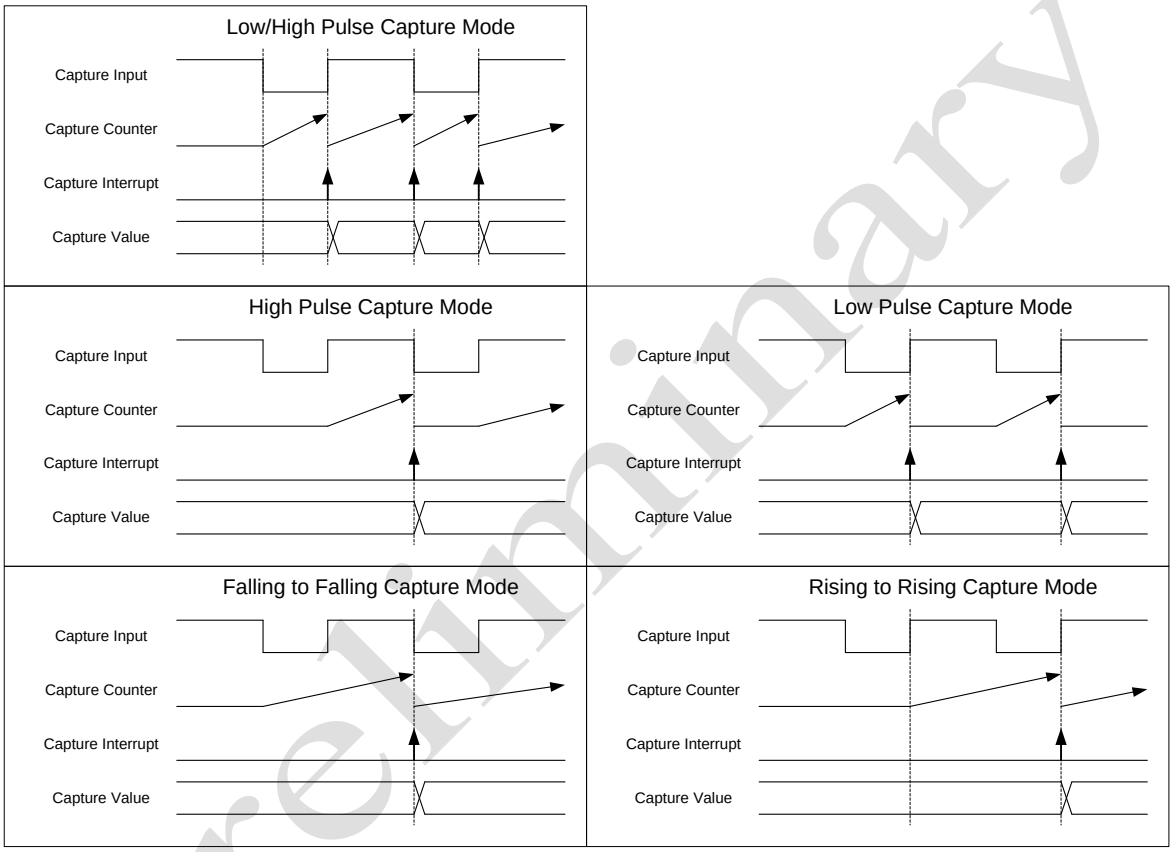


Figure 17-4 Capture Mode Operation

Calculating the period of captured pulses follows the below euqation.

$$Capture\ \ Signal\ \ Width\ \ Time = \frac{1}{Clock\ \ Source\ \ Frequency} \times \frac{1}{\mathrm{Pr}e - scaler\ \ Factor} \times (OCA + 1)\ \ [\mathrm{sec}]$$

Capture Time Example :

- Clock Source Frequency : 12MHz System Clock
- Pre-scaler Factor : 1 / 1024
- Capture Value : 9

=> 1/12MHz X 1024 X 10 = 0.853msec

To run in capture mode, following registers should be configured.
- TPxCTRL: choose the clock input of pre-scaler. Also, can clear pre-scaler
- TMxCTRL's TMOD: Change into capture mode
- TMxCTRL's CAPMOD: decide the mode of pulse capturing
- TMxCTRL's PFSEL: choose the clock for capturing
- TMxCTRL's TMEN: enable capturing

Following procedure is required to run capturing.
- Set TPxCTRL
- Set TMxCTRL
- Set the CNTCLR bit of TPxCTRL register if necessary
- Check the period of capturing by reading TMxDUT
- Check overflow by reading OVST of TMxCTRL register

17.3 Register Description

17.3.1 Timer Pre-scale Control Registers (TPxCTRL)

Address : 0x8002_0400 / 0x8002_0420 / 0x8002_0440 / 0x8002_0460

Bit	R/W	Description	Default Value
31 : 2	R	Reserved	-
1	R/W	CNTCLR : Pre-scale Counter and Timer Counter Reset When this bit is "1", the Timer Pre-scale and Counter will be reset.	0
0	R/W	CLKSEL : Pre-scale Clock Selection 0 : System clock 1 : CAPx	0

*** Each Timer channel has a CAPx.

17.3.2 Timer Control Registers (TMxCTRL)

Address : 0x8002_0404 / 0x8002_0424 / 0x8002_0444 / 0x8002_0464

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 14	R/W	TMOD : Timer/Counter Mode 00 : Timer 01 : PWM 1x : Capture	00
13	R	Reserved	-
12	R	OVST : Capture Overflow Status bit Read시 Overflow status bit가 clear된다.	0
11	R	Reserved	0
10 : 8	R/W	CAPMOD : Capture Mode Selection 00x : Low/High Pulse Capture mode 010 : Low Pulse Capture mode 011 : High Pulse Capture mode 10x : Failing to Failing Period Capture mode 11x : Rising to Rising Period Capture mode	000
7	R	Reserved	-
6	R/W	PWMO : PWM Output One Period Generation 0 : Disable 1 : Enable	0
5	R/W	PWML : PWM Output Start Level 0 : Start Level is Low 1 : Start Level is High	0
4	R/W	TMOUT : Timer Wave Output Generation 0 : Disable 1 : Enable	0
3 : 1	R/W	PFSEL : Pre-scale Factor Selection 000 : 1/2 001 : 1/8 010 : 1/32 011 : 1/128 100 : 1/512 101 : 1/2048 110 : 1/8192 111 : 1/32768	111
0	R/W	TMEN : Timer/Counter or PWM Enable 0 : Disable 1 : Enable	0

*** PWM Output One Period Generation: Decide the number of period to be generated in PWM mode. After the number, PWM is automatically disabled.

*** Timer Wave Output Generation: Decide whether output or not the toggled wave form on every period in Timer mode.

17.3.3 Timer Counter / PWM Period Registers (TMxCNT)

Address : 0x8002_0408 / 0x8002_0428 / 0x8002_0448 / 0x8002_0468

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 0	R/W	(Timer mode) - Write : Timer Counter Value - Read : Current Up-counter Value (PWM mode) - Read/Write : PWM Period Value	0xFFFF

17.3.4 Capture Counter Registers / PWM Duty Registers (TMxDUT)

Address : 0x8002_040C / 0x8002_042C / 0x8002_044C / 0x8002_046C

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 0	R/W	(Capture mode) - Read : Result value of counting at the sampling period (PWM mode) - Read/Write : PWM Duty Value	0xFFFF

*** PWM Duty : First Halt Duty of PWM Pulse

17.3.5 PWM Pulse Count Registers (TMxPUL)

Address : 0x8002_0410 / 0x8002_0430 / 0x8002_0450 / 0x8002_0470

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 0	R/W	(PWM mode) - Read/Write : PWM Pulse Number Value	0xFFFF

18 SPI (SERIAL PERIPHERAL INTERFACE)

adStar includes SPI which exchanges data with external devices and other CPUs through synchronized serial bus. This SPI is compatible with the SPI of M16HC11, M68HC05, and MC68HC16 series of Motorola, and supports full duplex 3-wire or half duplex 2-wire transmission.

For high speed SPI transmission, the SPI of adStar has FIFO of 8 bytes. The FIFO allows several Mbps of transmission rate without imposing overhead on CPU.

The SPI of adStar supports both master mode and slave mode.

18.1 Features

- Full duplex mode. Three-wired synchronous Transfer
- Master or Slave Operation
- Programmable clock polarity and phase
- End of transmission interrupt flag
- Write collision flag protection
- Master-master mode fault protection capability
- 8Bytes FIFO

18.2 Block Diagram

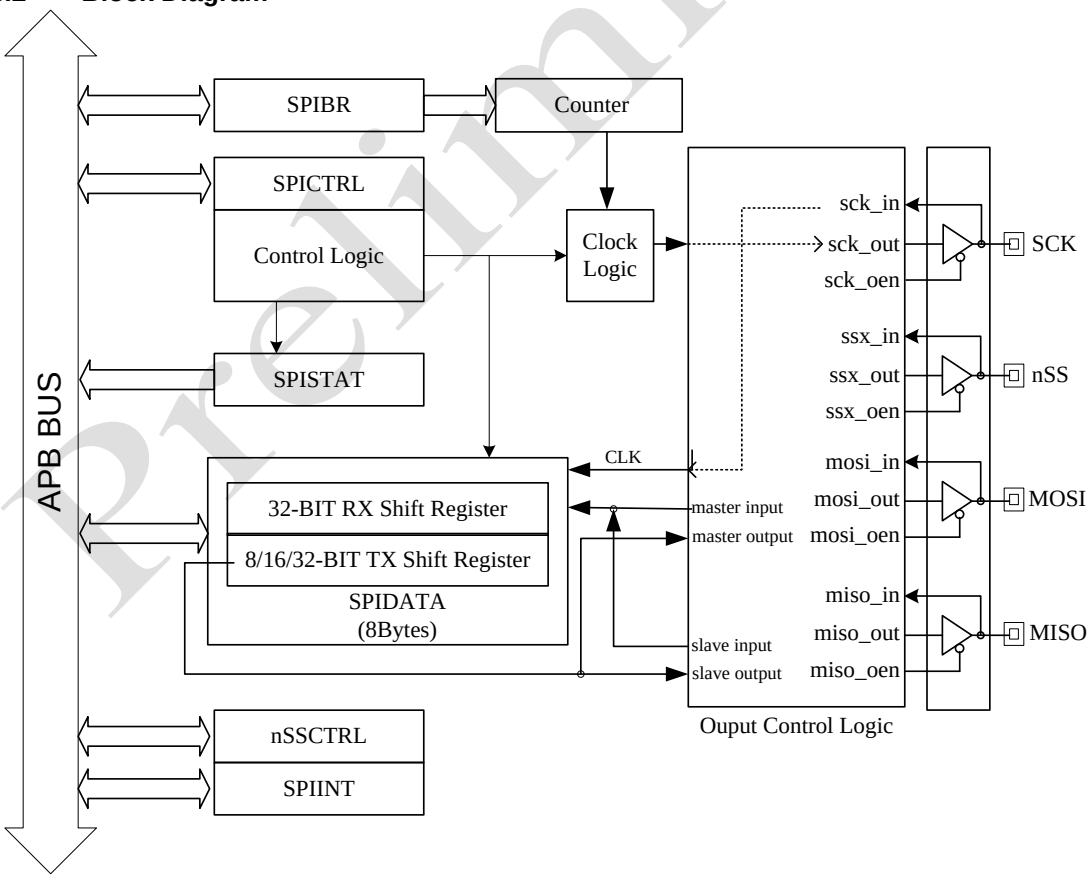


Figure 18-1 SPI Block Diagram

18.3 Function Description

The clock control circuit of the SPI can adjust its polarity and protocol so as to communicate with most of synchronized serial peripherals. When the SPI is set as a master, it can generate 256 various serial clocks in software.

The SPI can transmit and receive data at the same time. Sampling and shifting of two serial data lines are synchronized by serial clock line. Slave select line(nSS) can choose which SPI device to use. Unselected SPI devices don't affect SPI bus. The nSS line can be used to notify conflict among multiple masters in master SPI mode.

Error detection circuit is used to connect processes. When shifter register is written during transmission operation, it is a conflict. Multiple master mode failure detector disables output driver when more than one CPUs try to become bus master.

18.3.1 SPI Pins

SPI has four bi-directional pins: MISO, MOSI, SCK, and nSS. WOMP bit of SPI control register decides the output operation mode of each pins. Possible output operation modes are open drain and CMOS.

MSTR bit of SPI control register decides whether the SPI will operat as a master or a slave, and pins also follow the decision.

Table 18-1 SPI Pin Functions

Pin Name	*Mode*	*Function*
Master in, slave out(MISO)	Master	Provides serial data input to the SPI
	Slave	Provides serial data output from the SPI
Master out, slave in (MOSI)	Master	Provides serial output from the SPI
	Slave	Provides serial input to the SPI
serial clock(SCK)	Master	Provides clock output from the SPI
	Slave	Provides clock input to the SPI
Slave select(nSS)	Master	Output : Selects slave devices
	Slave	Input : chip select for SPI

18.3.2 SPI Operating Modes

SPI can become either master or slave. When its CPU controls data transmission, its mode is master. On the other hand, when a external device controls the data transmission, its mode is slave. MSTR bit of control register decides the mode.

Master Mode

If the MSTR bit of SPICTRL is set, SPI operates as master mode. Master can initialize serial transmission, and doesn't respond to initialization from external side.

In master mode, MISO pin is used for serial data input, and MOSI pin is used for serial data output. Depending on application area, one or two of these can be used.

Following procedure is required to use SPI in master mode.

1. Set BAUD, CPHA, CPOL, SIZE, MSBF, and WOMP of SPICTRL register.
2. MSTR bit should be set for master mode.
3. Set SPIEN bit to enable SPI.
4. Enable slave device.
5. Write proper data on SPIDATA register to begin transmission.
6. When the transmission finishs, SPIF flag of SPISTAT register is set by hardware, and it raises interrupt request. SPIF flag will be cleared automatically after reading SPISTAT and read or write SPIDATA register.

Data transmission is synchronized with internal serial clock(SCK). CPHA and CPOL bits of SPICTRL register controls phase and polarity of the clock. The clock is used for both transmiting data into MOSI pin and latching data from MISO pin.

Slave Mode

If MSTR bit of SPICTRL register is set to "0", the SPI becomes slave mode. In slave, SPI cannot initialize serial transmission. Transmissions are only initialized by external bus master. The slave mode is used when there are multiple masters on SPI bus because only one device can become the bus master at a time.

In slave mode, MISO pin is used for serial data output, and MOSI pin is used for data input. Depending on its application area, one or both of these can be used. SCK is input serial clock, and nSS signal is required to become active.

Data register should be written for data transmission. In slave mode, SCK, MOSI, and nSS pin are input, and MISO pin is output. CPHA, CPOL, SIZE, MSBF, and WOMP should be written. MSTR bit should be cleared for slave mode. SPIEN should be set to enable SPI. In slave mode, BAUD value doesn't affect SPI's operation.

When SPIEN is set and MSTR is cleared, "LOW" status of nSS pin initialize the operation of slave mode. nSS pin is only input.

After transmitting a byte or a word, SPI sets SPIF flag. If SPIF is set when SPIE is "1", a interrupt request raises.

Transmission is synchronized with external SCK. CPHA and CPOL are used to latch data from MOSI pin or to decide clock edge of outgoing data through MISO pin.

18.3.3 SCK Phase and Polarity Control

Two bits of control register decide the phase and polarity of SCK. CPOL bit decides the polarity of the clock(high or low). CPHA bit decide the phase of transmission which affects the timing of transmission. The polarity and phase of master and slave should be same. However, in some cases, Master can communicate with slave with different polarity and phase by changing them during a transmission. This flexibility of SPI allows it direct connection with most of synchrnoized serial peripherals.

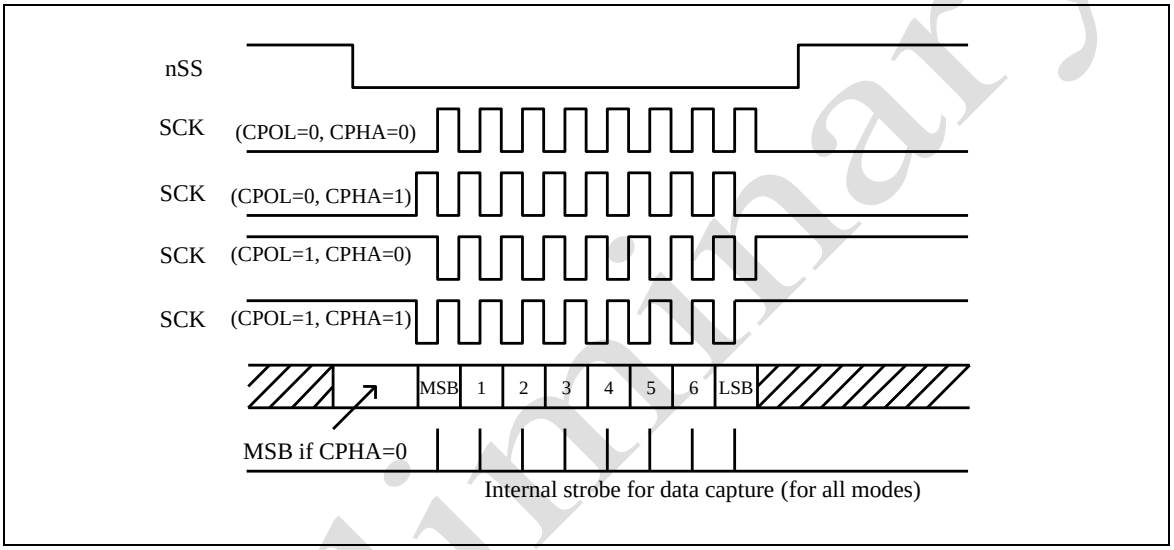


Figure 18-2 SCK Phase and Polarity

18.3.4 Data Transfer Timing

Following figure shows data transmission timing diagram when CPHA is '0' and MSB is comes first. It shows two form of SCK. One is when CPOL is '0', and the other is when CPOL is '1'. It can be a diagram of both master and slave because they share SCK, MISO, and MOSI lines. MISO signal is a output of slave, and MOSI signal is output of master. nSS signal is chip select.

If master write data on SPDR, transmission is initialized. Slave is initialized when nSS sees a falling edge. SCK signal remains inactive until the half period of SCK cycle.SPIF bit which represent the end of a transmission is set at the eighth SCK cycle. When CPHA is '0', nSS toggles from low to high after transmiting a byte. If a slave write on data register when nSS is low, write collision error raises.

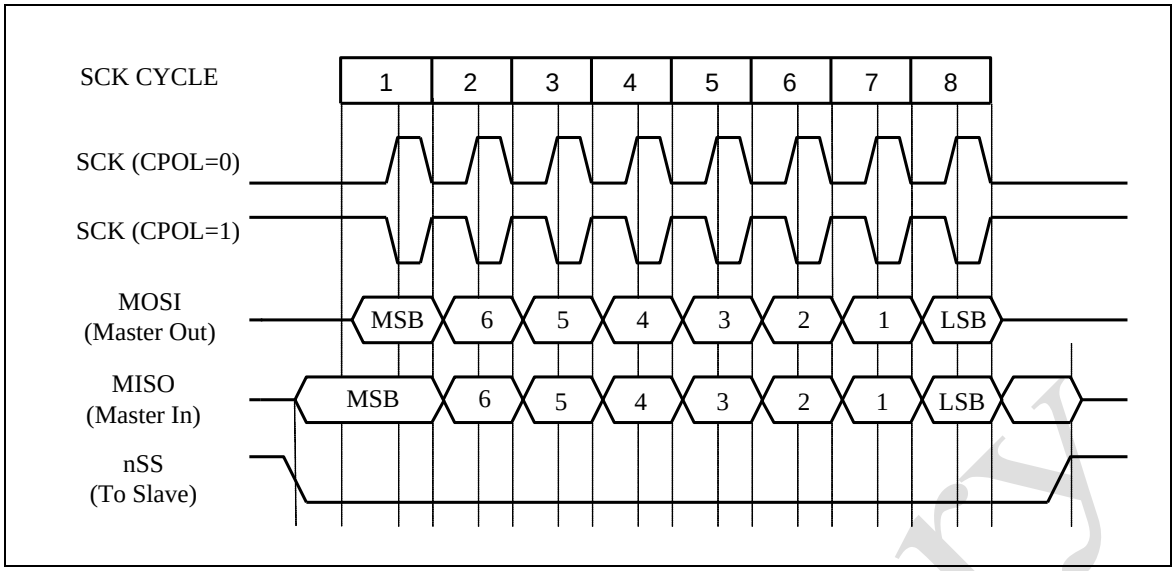


Figure 18-3 Transfer Timing when CPHA = '0'

The next figure is for CPHA='1'. SCK become inactive at the half period of the eighth cycle. SPIF bit is set at the end of the eighth SCK cycle. Because the last edge is generated at the middle of the eighth SCK cycle, slave finishes receving after samping the last data. nSS keeps "low" state during enough time after transmitting 1 byte.Thus, if CPU continuously sends data, nSS keeps low state.

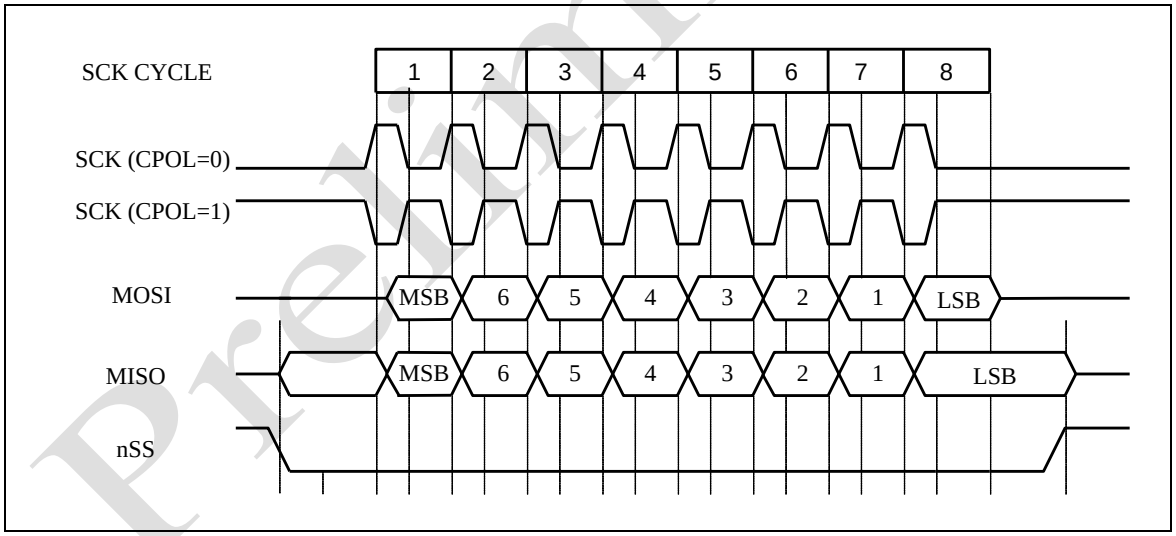


Figure 18-4 Transfer Timing when CPHA = '1'

18.3.5 SPI Serial Clock Baud Rate

SPI Baud rate can be set between 1 to 255 by writing SPBR register. In slave mode, SCK is given by external SPI master; therefore, So SPIBRR register value is ignored. However, its maximum speed is limited by system clock.

$$SCK\ Baud\ Rate = \frac{f_{PCLK}}{2 \times (SPIBR + 1)}$$

or

$$SPIBR = \frac{f_{PCLK}}{2 \times SCK\ Baud\ Rate} - 1$$

18.3.6 Open-Drain Output for Wired-OR

Unless there are multiple SPI masters, SPI bus output doesn't need to support open-drain. When open-drain output is necessary, WOMP bit of SPICTRL register should be set. Pull-up register is necessary for each open-drain output line

18.3.7 Transfer Size and Direction

SPISIZE bit of SPICTRL register decide the transfer size of SPI: 8, 16, or 32bit. MSBF bit of SPICTRL reigster decides which bit to transfer first (MSB or LSB).

18.3.8 Write Collision

Write collision raises if one try to write SPIDATA register during a transmission.

18.3.9 MODE Fault

If mode fault error happens when SPI is set to master mode and nSS signal input line is asserted, MODF bit of SPISTAT is set. MODF can be set only under master mode, and it happens when other SPI device tries to become a master.

18.3.10 Interrupt

SPIF Interrupt

It is raised when both FIFO and TX shift register become empty, and this means SPI transmission is complete.

MODF Interrupt

It is raised when mode fault happens. Mode fault happens when more than one master try to transmit data.

nSS Interrupt

It is raised when nSS port signal changes.

TX_FIFO_FULL, TX_FIFO_EMPTY, RX_FIFO_FULL, RX_FIFO_EMPTY

- TX_FIFO_FULL: Means the internal 8 byte FIFO became full. If more data are added to FIFO when it's full, data transmission will be corrupted.
- TX_FIFO_EMPTY: Means every data in the FIFO are transmitted. However, because TX shift register can be not empty yet, so this interrupt doesn't mean SPI transmission is completed.
- RX_FIFO_FULL: means RX_FIFO is full.
- RX_FIFO_EMPTY: means RX_FIFO is empty.

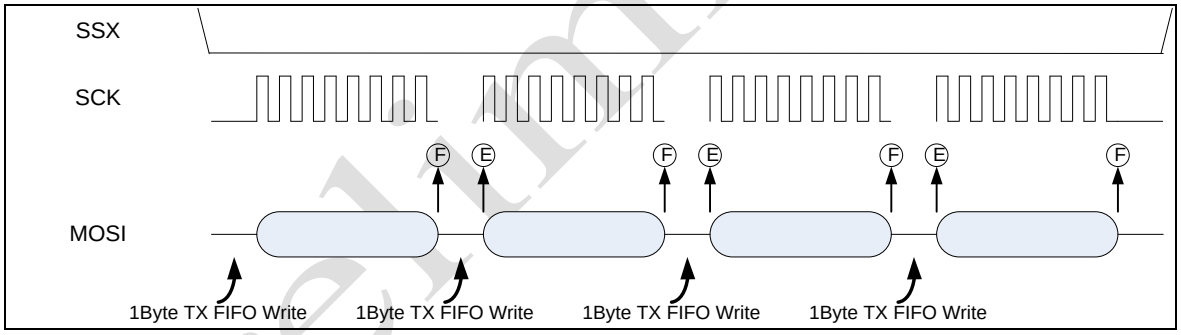


Figure 18-5 1-Byte Transfer vs. Status and Interrupt

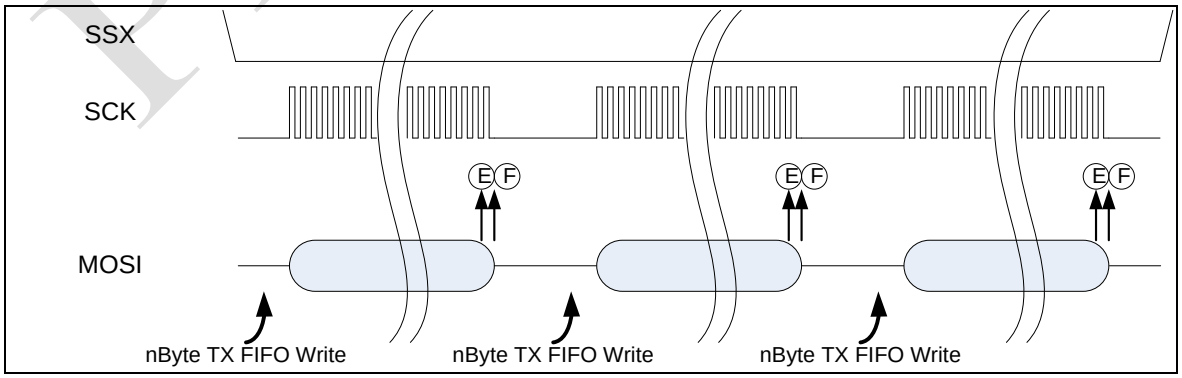


Figure 18-6 n-Bytes Transfer vs. Status and Interrupt

18.4 Register Description

18.4.1 SPI Control Register (SPICTRL)

Address : 0xA002_1000 / 0xA002_1400

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	R/W	SPIEN : SPI Enable 0 : SPI is disabled. 1 : SPI is enabled	0
6	R/W	WOMP : Wired-OR Mode for SPI Pins 0 : Outputs have normal CMOS drivers. 1 : Open-drain drivers	0
5	R/W	MSTR : Master/Slave Mode Select 0 : Slave operation 1 : Master operation	0
4	R/W	CPOL : Clock Polarity 0 : The inactive state value of SCK is logic level zero 1 : The inactive state value of SCK is logic level one.	0
3	R/W	CPHA : Clock Phase 0 : Data captured on the leading edge of SCK and changed on the trailing edge of SCK. 1 : Data is changed on the leading edge of SCK and captured on the trailing edge of SCK.	0
2	R/W	MSBF : Most Significant Bit First 0 : Serial data transfer starts with LSB. 1 : Serial data transfer starts with MSB.	0
1 : 0	R/W	SPISIZE : Transfer Data Size 00 : 8-bit data transfer. 01 : 16-bit data transfer. 10 : 32-bit data transfer.	0

18.4.2 SPI Baud Rate Register (SPIBR)

Address : 0xA002_1004 / 0xA002_1404

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7 : 0	R/W	Serial Clock Baud Rate $SCK = \frac{f_{PCLK}}{2 \times (SPIBR + 1)}$ Master Mode SCK ≤ System Clock / 2 Slave Mode SCK ≤ System Clock / 4	0xFF

18.4.3 SPI Status Register (SPISTAT)

Address : 0xA002_1008 / 0xA002_1408

Bit	R/W	Description	Default Value
15 : 8	R	Reserved	-
7	R	SPIF : SPI Finished Flag 0 : SPI is not finished. 1 : SPI is finished.	0
6	R	WCOL : Write Collision 0 : No attempt to write to the SPDR happened during the serial transfer. 1 : Write collision occurred.	0
5	R	MODF : Mode Fault Flag 0 : Normal operation 1 : Another SPI node requested to become the network SPI master while the SPI was enabled in master mode	0
4	R	nSS : Slave Select Flag 0 : Current Value of nSS port is low 1 : Current Value of nSS port is high	0
3	R	STXF : TX FIFO Full Status bit 0 : FIFO_TX is not full 1 : FIFO_TX is full	0
2	R	STXE : TX FIFO Empty Status bit 0 : FIFO_TX is not empty 1 : FIFO_TX is empty	0
1	R	SRXF : RX FIFO Full Status bit 0 : FIFO_RX is not full 1 : FIFO_RX is full	0
0	R	SRXE : RX FIFO Empty Status bit 0 : FIFO_RX is not empty 1 : FIFO_RX is empty	0

18.4.4 SPI Data Register (SPIDATA)

Address : 0xA002_100C / 0xA002_140C

Bit	R/W	Description	Default Value
31 : 0	R/W	SPI Data At 32-bit transfer mode - MSB of Data is SPDR[31] At 16-bit transfer mode - MSB of Data is SPDR[15] At 8-bit transfer mode - MSB of Data is SPDR[7] LSB of Data (received or transmit) is SPDR[0] in any transfer mode	0x0000_0000

18.4.5 SPI nSS Control Register (nSSCTRL)

Address : 0xA002_1010 / 0xA002_1410

Bit	R/W	Description	Default Value
31 : 1	R	Reserved	-
0	RW	nSSCON : nSS Output Level	1

18.4.6 SPI Interrupt Mask Register (SPIINT)

Address : 0xA002_1014 / 0xA002_1414

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	RW	SPIFE : SPIF Interrupt en/disable SPIF Interrupt occurs when transfer has completed. 0 : SPIF interrupt is disabled 1 : SPIF is enabled	0
6	RW	MODFE : MODFI Interrupt en/disable MODFI Interrupt occurs when two more master use data line. 0 : MODFI interrupt is disabled 1 : MODFI is enabled	0
5	R	Reserved	0
4	RW	nSSEN : nSS Interrupt en/disable nSS Interrupt occurs when nSS signal has changed. 0 : nSS Interrupt is disabled 1 : nSS Interrupt is enabled	0
3	RW	STXFE : FIFO_TX_FULL Interrupt en/disable FIFO_TX_FULL Interrupt occurs when FIFO_TX is full 0 : FIFO_TX_FULL Interrupt is disabled 1 : FIFO_TX_FULL Interrupt is enabled	0
2	RW	STXEE : FIFO_TX_EMPTY Interrupt en/disable FIFO_TX_EMPTY Interrupt occurs when FIFO_TX is empty 0 : FIFO_TX_EMPTY Interrupt is disabled 1 : FIFO_TX_EMPTY Interrupt is enabled	0
1	RW	SRXFE : FIFO_RX_FULL Interrupt en/disable FIFO_RX_FULL Interrupt occurs when FIFO_RX is full 0 : FIFO_RX_FULL Interrupt is disabled 1 : FIFO_RX_FULL Interrupt is enabled	0
0	RW	SRXEE : FIFO_RX_EMPTY Interrupt en/disable FIFO_RX_EMPTY Interrupt occurs when FIFO_RX is empty 0 : FIFO_RX_EMPTY Interrupt is disabled 1 : FIFO_RX_EMPTY Interrupt is enabled	0

19 TWI (TWO WIRED INTERFACE)

adStar has a TWI controller to interface with general TWI bus. TWI has two signals: SCL and SDA.

19.1 Features

- Master transmitter mode
- Master receive mode
- Slave transmitter mode
- Slave receive mode
- Software programmable clock frequency
- Software programmable acknowledge bit
- Interrupt driven data-transfers
- Start/Stop/Repeated Start/Acknowledge generation
- Multi master operation

19.2 Block Diagram

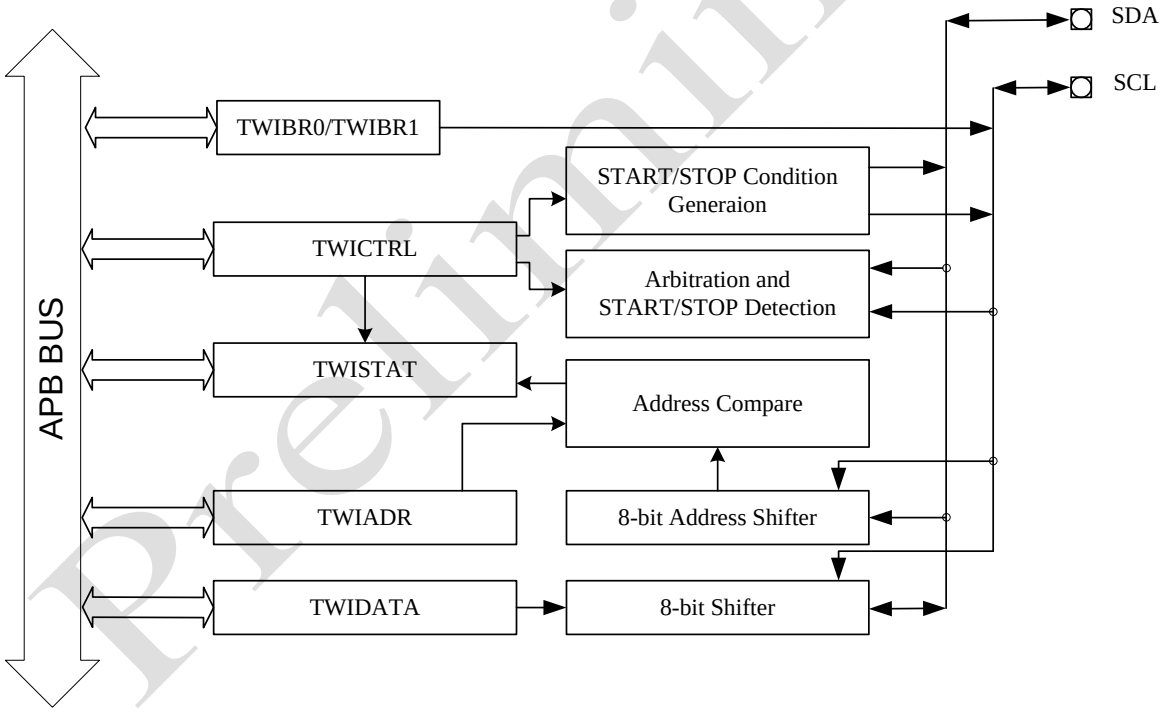


Figure 19-1 TWI Block Diagram

19.3 Function Description

19.3.1 DATA TRANSFER FORMAT

Every data on SDA line has 8bit width. The number of byte for a transfer is not limited. The first byte after start condition is address field. When TWI bus is in master mode, the master sends the address field. Every bytes are followed by ACK bit. And always MSB bits are tranfered first.

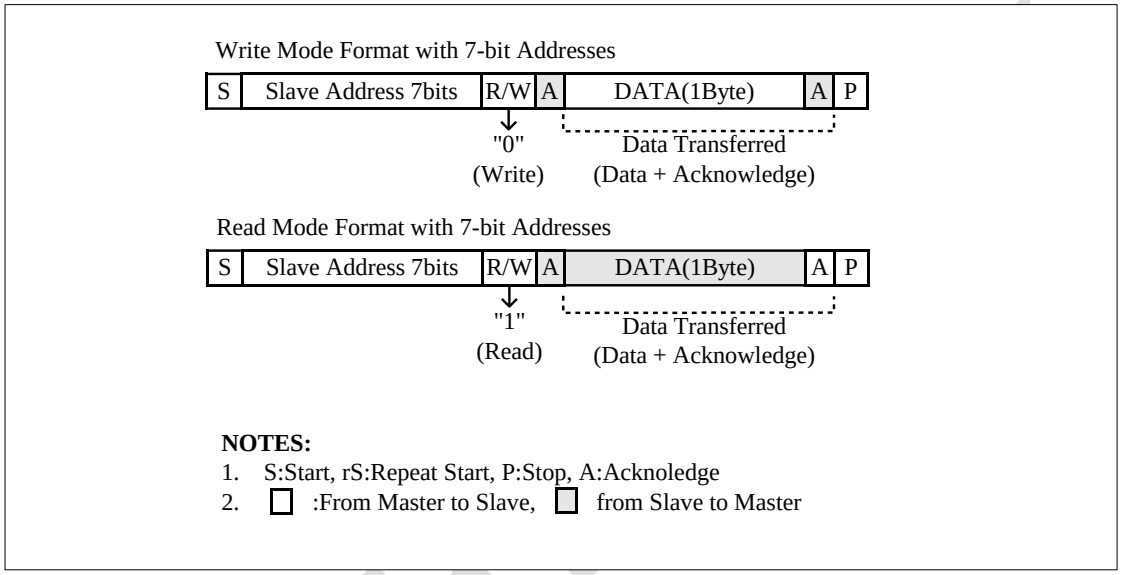


Figure 19-2 TWI-Bus Interface Data Format

19.3.2 START AND STOP CONDITION

Start condition initalizes a transfer, and stop condition finishes it. Start condition is the transition of SDA line from high-to-low during SCL line is high. Stop condition is the transition of SDA line from low-to-high when SCL is high. If a start condition happens, TWI bus become busy. After a stop condition, TWI bus become free.

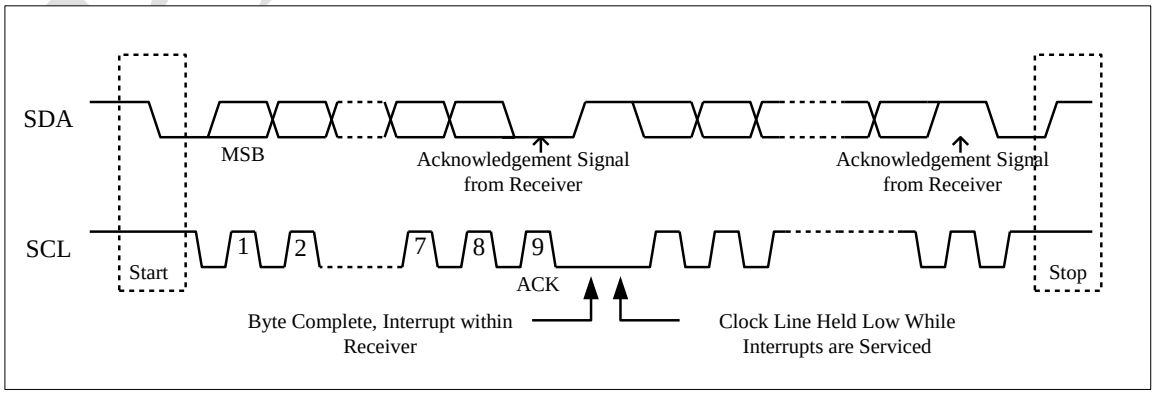


Figure 19-3 Data Transfer on the TWI-Bus

19.3.3 ACK SIGNAL TRANSMISSION

To finish a byte transfer, receiver should send a ACK bit to its sender. ACK pulse should happen at the ninth clock of SCL line. So we need 9 clocks to transfer a byte. Master should generate clock pulses fot ACK bit reception.

Sender should release SDA line to receive a ACK clock pulse. Receiver should should lower SDA line at ninth SCL period to change SDA line into “low”.

Software can set ACK bit can be ACK or NACK by setting TXACK bit of control register.

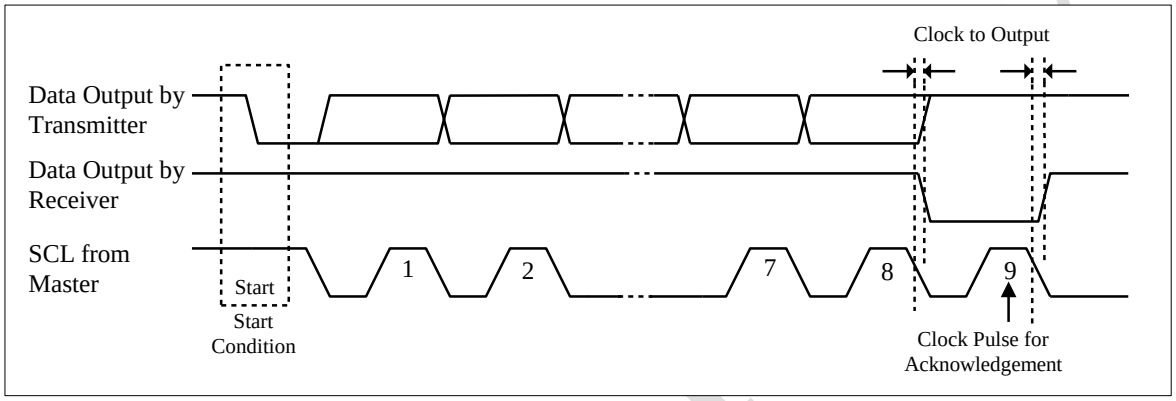


Figure 19-4 Acknowledgement of TWI

19.3.4 READ-WRITE OPERATION

In sending operation mode, TWI bus interface should wait until data shifter register become ready after transfering data. Until data writing completes, SCL line will be kept low. SCL is released after new data is written in shifter register.

When interruption is enabled, TWI raises interrupt after transfering current data.CPU writes new data into buffer after handling the interrupt request.

In receiving mode, TWI bus waits until TWI bus reads data after receiving data . During the reading, SCL is kept “low”. SCL is released after new data is read.

When interruption is enabled, TWI raises interrupt when data is received. The interrupted CPU reads the data.

19.3.5 BUS ARBITRATION PROCEDURES

Prevents multiple masters from controlling bus at the same time. If a master which sent high signal on SDA line senses other master's low level SDA signal, the first master recognize that multiple masters are on bus, and stops its transfer.

When two devices become master mode at the same time, to say master 1 and master 2, the SCL line is synchronized as following clock wave form.

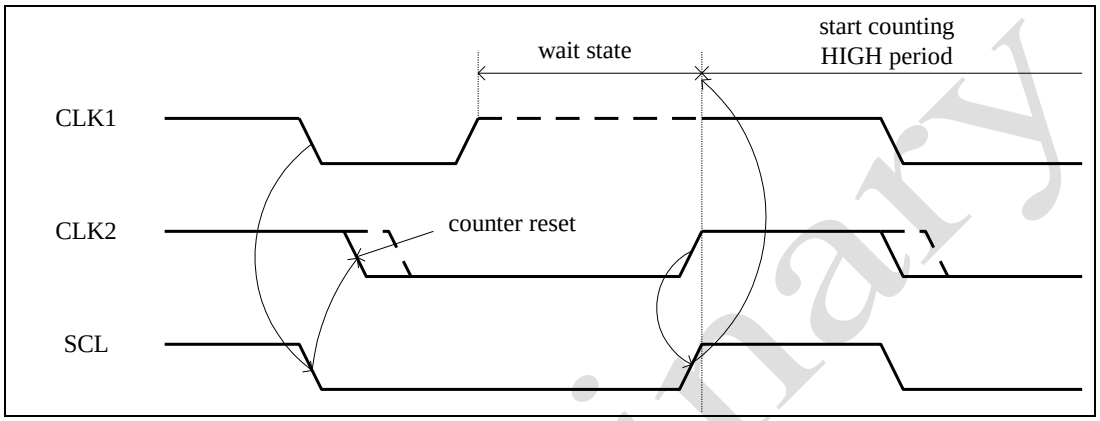


Figure 19-5 Bus arbitration 1 of TWI

In the above situation, either device 1 or device 2 will have priority depending on SDA line value as shown in the next diagram

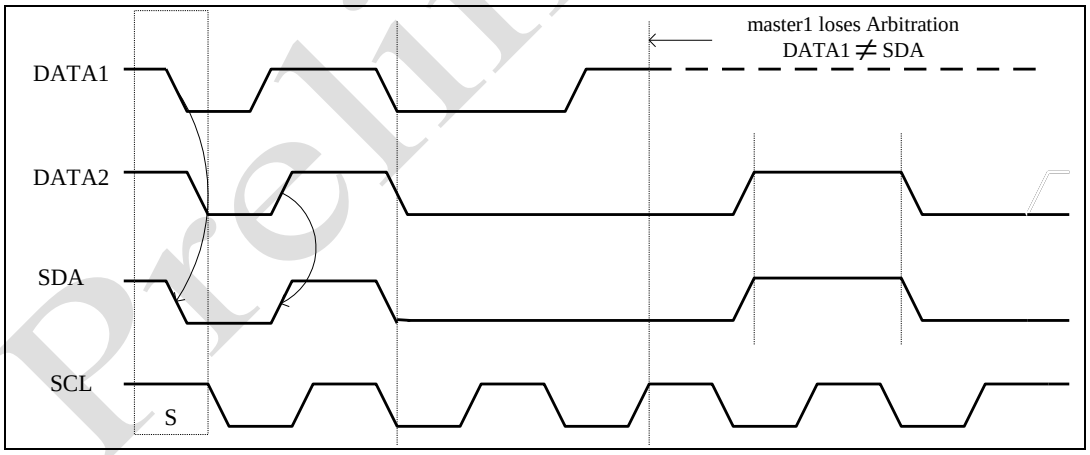


Figure 19-6 Bus arbitration 2

19.3.6 ABORT CONDITIONS

With arbitration

1. If MSTR bit of TWICTRL register is cleared, stop condition is generated.
2. No Ack generates stop condition. That is to say,SDA signal is not “low” under ACK period.

Without arbitration

Arbitration takes away control and clears MSTR bit, however, stop condition isn’t generated. SCL clock lasts until a byte transfer finishes, and SDA become “high”.

19.3.7 Operational Flow Diagrams

TWI initialization

First, TWI should be initialized.

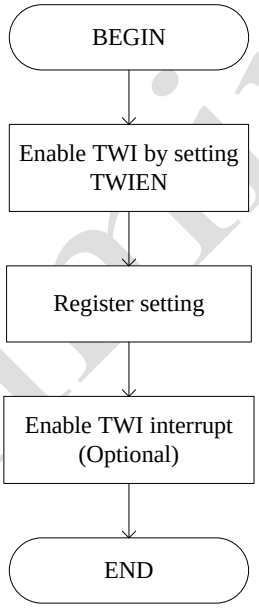


Figure 19-7 TWI Initialization Flow Char

Master Transmit /Receive

Below is the flow chart of TWI transmission and reception. For reception, additional steps are required. First, ACK bit should be set NO ACK upon the last data. This is to notify slave that master has sent its last data. Inaddition, dummy reading of TWIDATA register is required to generate SCL clock.

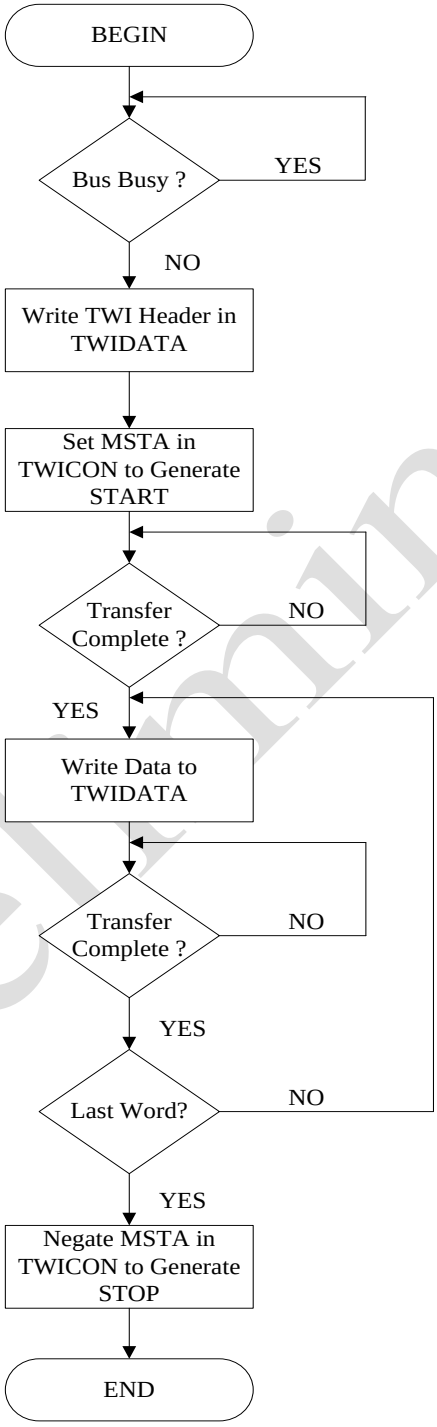


Figure 19-8 Master Transmit Flow Char

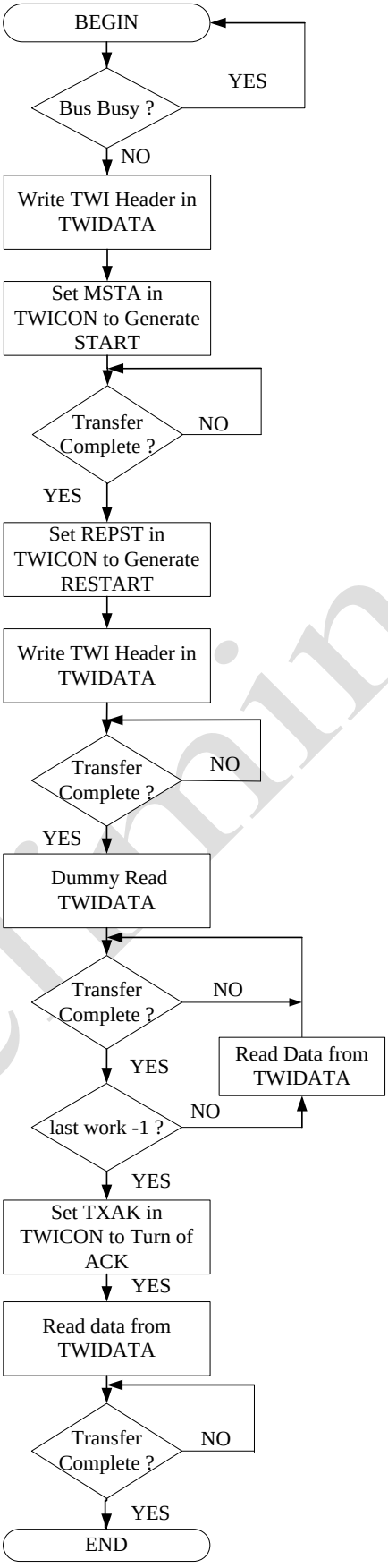


Figure 19-9 Master Receive Flow Char

Slave Mode (Polling mode)

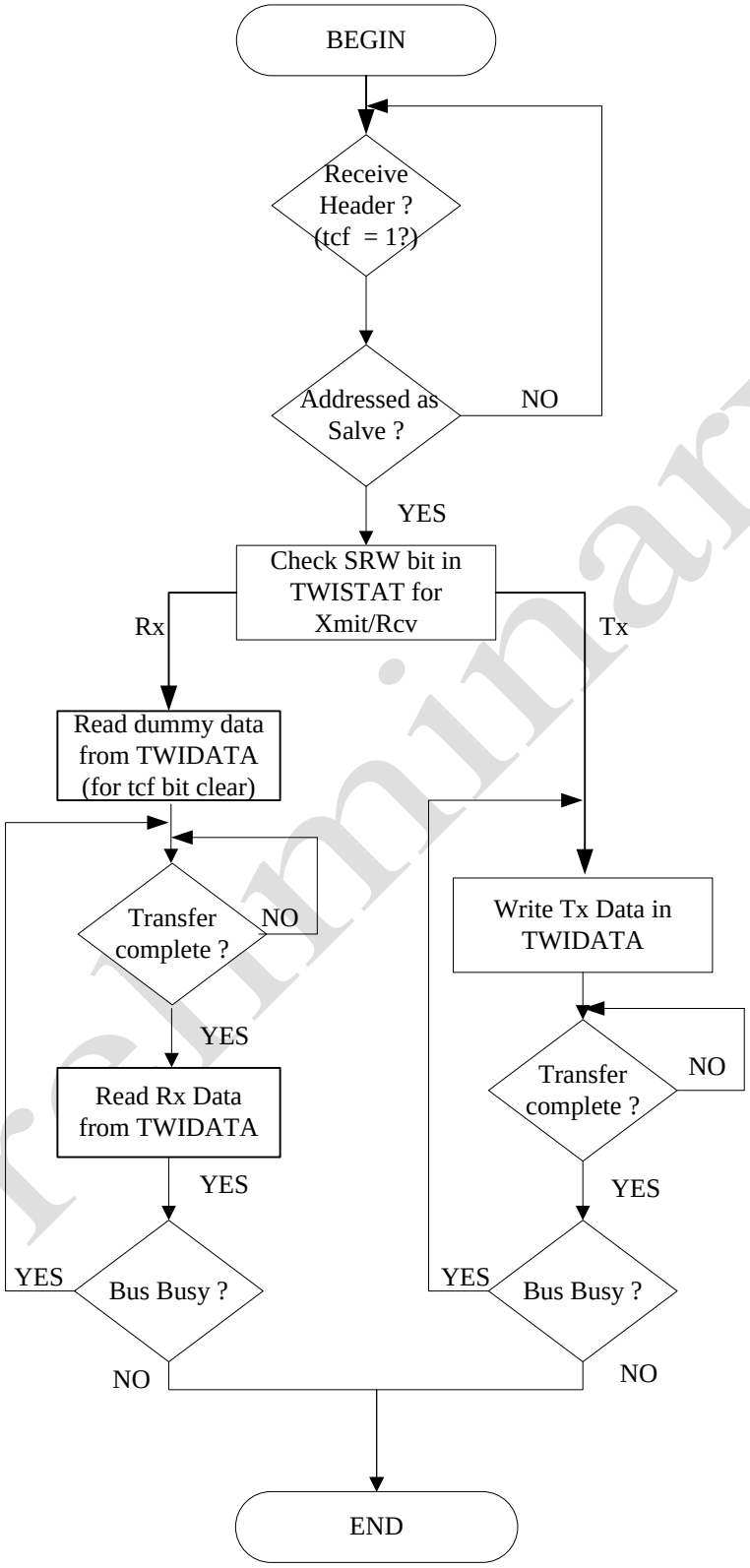


Figure 19-10 Slave Mode Flow Chart (Polling)

Slave Mode (Interrupt mode)

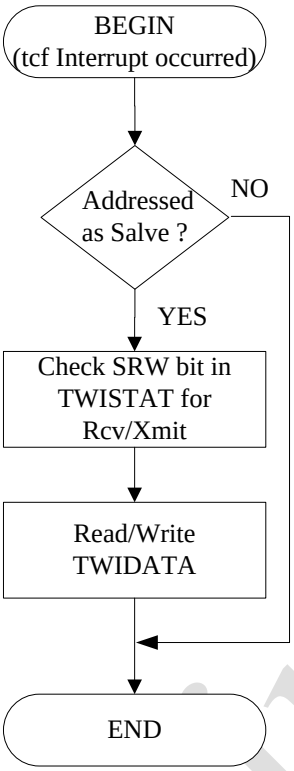


Figure 19-11 Slave Mode Flow Chart (Interrupt)

19.4 Register Description

19.4.1 TWI Control Register (TWICTRL)

Address : 0x8002_1800

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7	RW	TWIEN : TWI Controller Enable. For TWI transmission and reception, this bit should be set first. 0: Disable 1: Enable	0
6	R	Reserved.	-
5	RW	TWIMOD : Master/Slave Mode Select. When it toggles from 0 to 1, TWI enters into master mode, and START condition is generated. When it is cleared (1 to 0), STOP condition is generated, and TWI enters into slave mode. Though cleared, if TWI lost control right, STOP condition is not generated. 0: generates STOP condition 1: generates START condition	0
4	RW	TWITR : Transmit/Receive Mode Select. Decide operation in Master Mode 0: TWI Master receives 1: TWI Master transmits	0
3	RW	TWIAK : Transmit Acknowledge Enable. Decide SDA line value during ACK period. If it is in master receive mode and transmitting its last byte, NO ACK means that it is the last data transmission. After the last transmission, NO ACK generates STOP condition. 0: ACK bit = "0" – ACK (acknowledge) 1: ACK bit = "1" – NO ACK (no acknowledge)	0
2	RW	REPST : Repeated Start. If this be is set (=1) and TWI controller is in master mode, repeated START condition is generated. It is cleared after the repeated START condition is generated, 0: N/A 1: generates repeated START condition	0
1	R/W	TCIE : Transfer complete Interrupt enable bit Decide signaling interrupt or not when byte-unit transmission completes 0: Disable 1: Enable	0
0	R/W	LSTIE : Lost arbitration Interrupt enable bit Decide signaling interrupt or not when TWI lost its transmission write in master mode. 0: Disable 1: Enable	0

19.4.2 TWI Status Register (TWISTAT)

Address : 0x8002_1804

Bit	R/W	Description	Default Value
31 : 10	R	Reserved.	-
9	RW	TXEMPTY : TX Buffer Empty. Represent the status of transmitting buffer. This bit can be written when it is 0. 0: TX buffer has data to transmit 1: TX buffer is empty	1
8	RW	RXFULL : RX Buffer Full. Represent the status of receiving buffer. This bit can be written when it is 1. 0: RX buffer is empty 1: RX buffer has data to be read	0
7	R	TWIDT : Data Transferring Bit. Set whenever a byte is transmitted, and cleared when TWIDATA register is read or written. Also, writing "1" clears this bit. 0: byte is being transmitted 1:byte transmission completed	0
6	R	TWIAS : Addressed as Slave Bit. When its address and received address coincide, TWI controller become slave. This bit is cleared when TWICON register is written or when STOP condition happens. 0: Address doesn't coincides 1: Addresses coincides	0
5	R	TWIBUSY : Bus Busy Bit. Represent the status of TWI bus. Set by START condition and cleared by STOP condition. Also, writing "0" clears this bit. 0: Bus is in idle status 1: Bus is in busy status	0
4	RW	TWILOST : Lost Arbitration Bit. This bit is set when bus loses its control in master mode. Software can clear this bit by writing "1" to this bit. 0: Lost arbitration doesn't happen 1: Lost arbitration happen	0
3	R	TWISRW : Slave Read/Write Bit. Represent transmit or receive mode in slave mode. 0: Slave receive mode 1: Slave transmit mode	0
2	R	Reserved.	-
1	RW	RSF : Repeated start flag Represent whether repeated START condition has happened or not. Set when repeated START condition happens, and cleared when STOP condition happens. Also, writing "1" when this bit	0

		is set will clear this bit. 0: Repeated START condition didn't happen, or STOP condition happened. 1: Repeated START condition has happened.	
0	R	TWIRXAK : Received Acknowledge Bit. Represent SDA line value during ACK period. 0: Acknowledge received 1: No Acknowledge received	1

19.4.3 TWI Address Register(TWIADR)

Address : 0x8002_1808

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7: 0	RW	(At only slave mode) 7-bit slave address. Represent the device address of TWI controller [7:1] = Slave Address [0] = Not mapped	0x00

19.4.4 TWI Data Register (TWIDATA)

Address : 0x8002_180C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7 : 0	RW	TWI data : Represent TWI data Write – written data or the address of accessing device Read – received data	0x00

19.4.5 TWI Baud-Rate 0 Register (TWIBR0)

Address : 0x8002_1810

Bit	R/W	Description	Default Value
31 : 4	R	Reserved.	-
7 : 0	RW	Baud-rate 0 Value. TWIBR0 ≥ 3	0x0F

19.4.6 TWI Baud-Rate 1 Register (TWIBR1)

Address : 0x8002_1814

Bit	R/W	Description	Default Value
31 : 9	R	Reserved.	-
8 : 0	RW	Baud-rate 1 Value.. TWIBR1 ≥ 0	0xFF

$$TWIBR0 = f_{PCLK} \times 700ns + 3$$

$$SCL = \frac{f_{PCLK}}{(2TWIBR1 + TWIBR0 + 7)}$$

$$TWIBR1 = \frac{f_{PCLK}}{2SCL} - \frac{TWIBR0 + 7}{2}$$

* f_{PCLK} = AMBA APB clock frequency

*SCL = TWI transmission rate

ex) If APB clock is 50MHz and TWI transmission rate is 400Kbps, (f_{PCLK} = 50MHz, SCL = 400Kbps)

$$TWIBR0 = 50MHz \times 700ns + 3 = 50 \times 10^{6} \times 700 \times 10^{-9} + 3 = 38$$

$$SCL = \frac{f_{PCLK}}{(2TWIBR1 + TWIBR0 + 7)} \Rightarrow 400Kbps = \frac{50MHz}{(2TWIBR1 + 38 + 7)} \Rightarrow 400 \times 10^{3} = \frac{50 \times 10^{6}}{(2TWIBR1 + 45)}$$

<Baud-rate Register Setting Reference Table>

f_{PCLK}	TWIBR0	TWIBR1			
		400Kbps	300Kbps	200Kbps	100Kbps
48Mhz	37(0x25)	38(0x26)	58(0x3A)	98(0x62)	218(0xDA)
24Mhz	20(0x14)	17(0x11)	27(0x1B)	47(0x2F)	107(0x6B)
12Mhz	12(0xC)	6(0x6)	11(0xB)	21(0x15)	51(0x33)
6Mhz	7(0x7)	1(0x0)	3(0x3)	8(0x8)	23(0x17)
11.2896Mhz	11(0xB)	5(0x5)	10(0xA)	19(0x13)	48(0x30)
5.6448Mhz	7(0x7)	0(0x0)	3(0x3)	7(0x8)	21(0x16)

* Above table can bear some errors.

20 UART

adStar has 5 channel UART(Universal Asynchronous Receiver/Transmitter) controller, and it allows asynchronous communication with general PC or I/O devices equipping RS-232 interface.

20.1 Features

- Compatible with standard 16450/16550 UARTs
- Fully programmable serial-interface protocols
  - 5,6,7,8-bit characters
  - Even, odd or no-parity, stick parity generation and detection
  - 1, 1.5, 2 stop bit generation
  - Baud rate generator
- Line break generation and detection
- False start bit detection
- Prioritized transmit, receive and line status control interrupts
- Independent 16 characters transmit and receive 16Bytes FIFOs
- 5 Ch. UARTs

20.2 Block Diagram

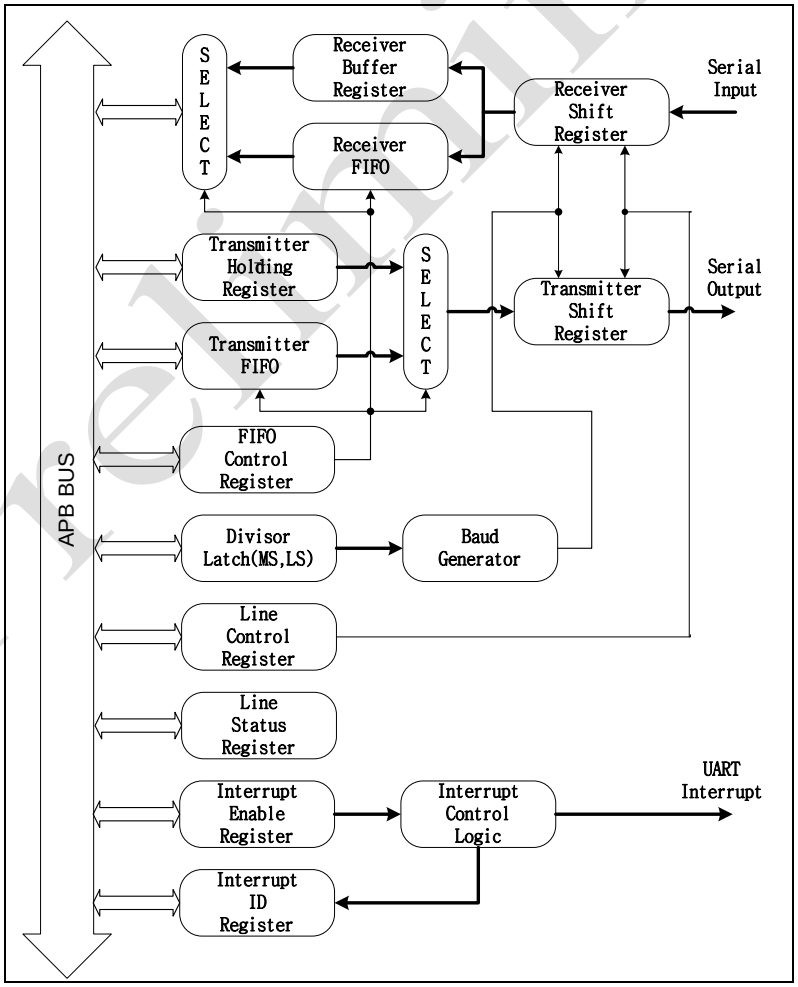
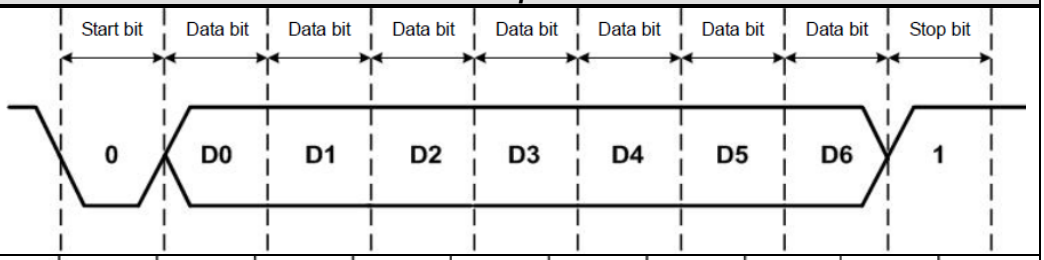
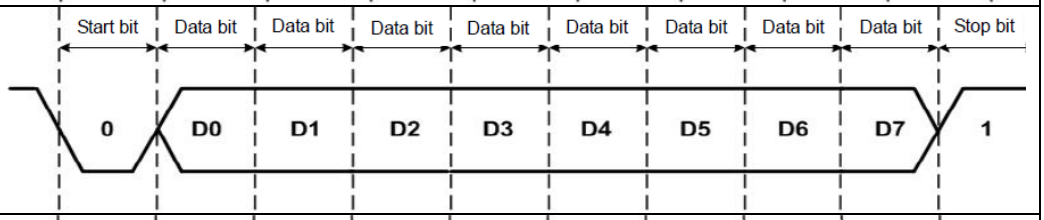
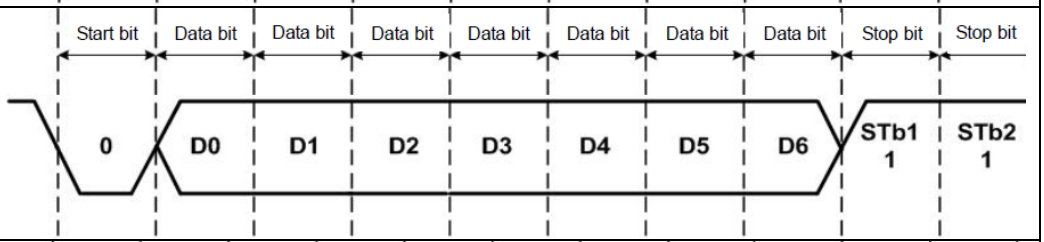
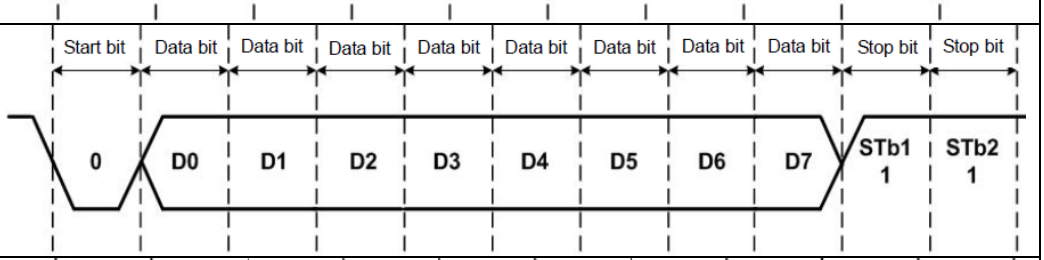
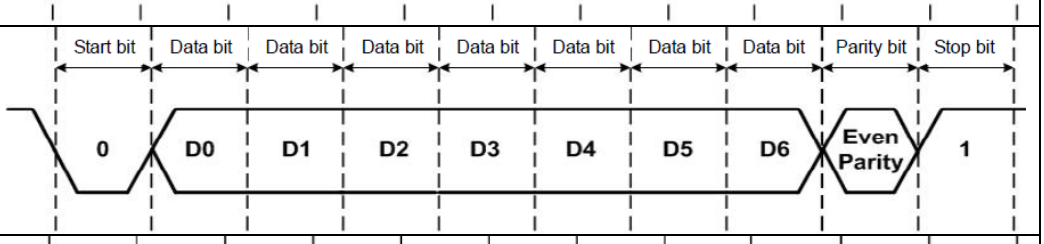
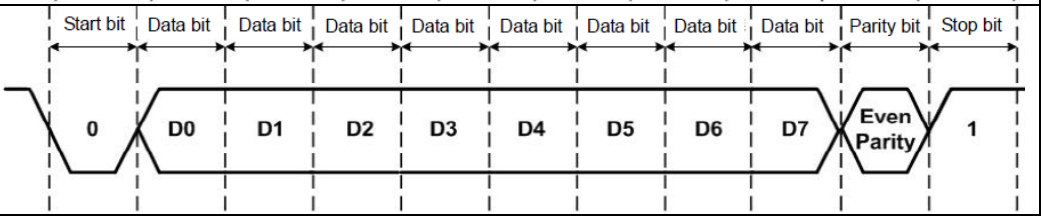


Figure 20-1 UART Block Diagram

20.3 Function Description

20.3.1 Serial Data Format

UART of adStar can change the serial data format of UART communication by configuring ULCRn[4:0] bits. Following table explains available data formats.

ULCRn[4:0]	Description
00010 No Parity / 1 Stop bit / 7 Data bit	
00011 No Parity / 1 Stop bit / 8 Data bit	
00110 No Parity / 2 Stop bit / 7 Data bit	
00111 No Parity / 2 Stop bit / 8 Data bit	
11010 Even Parity / 1 Stop bit / 7 Data bit	
11011 Even Parity / 1 Stop bit / 8 Data bit	

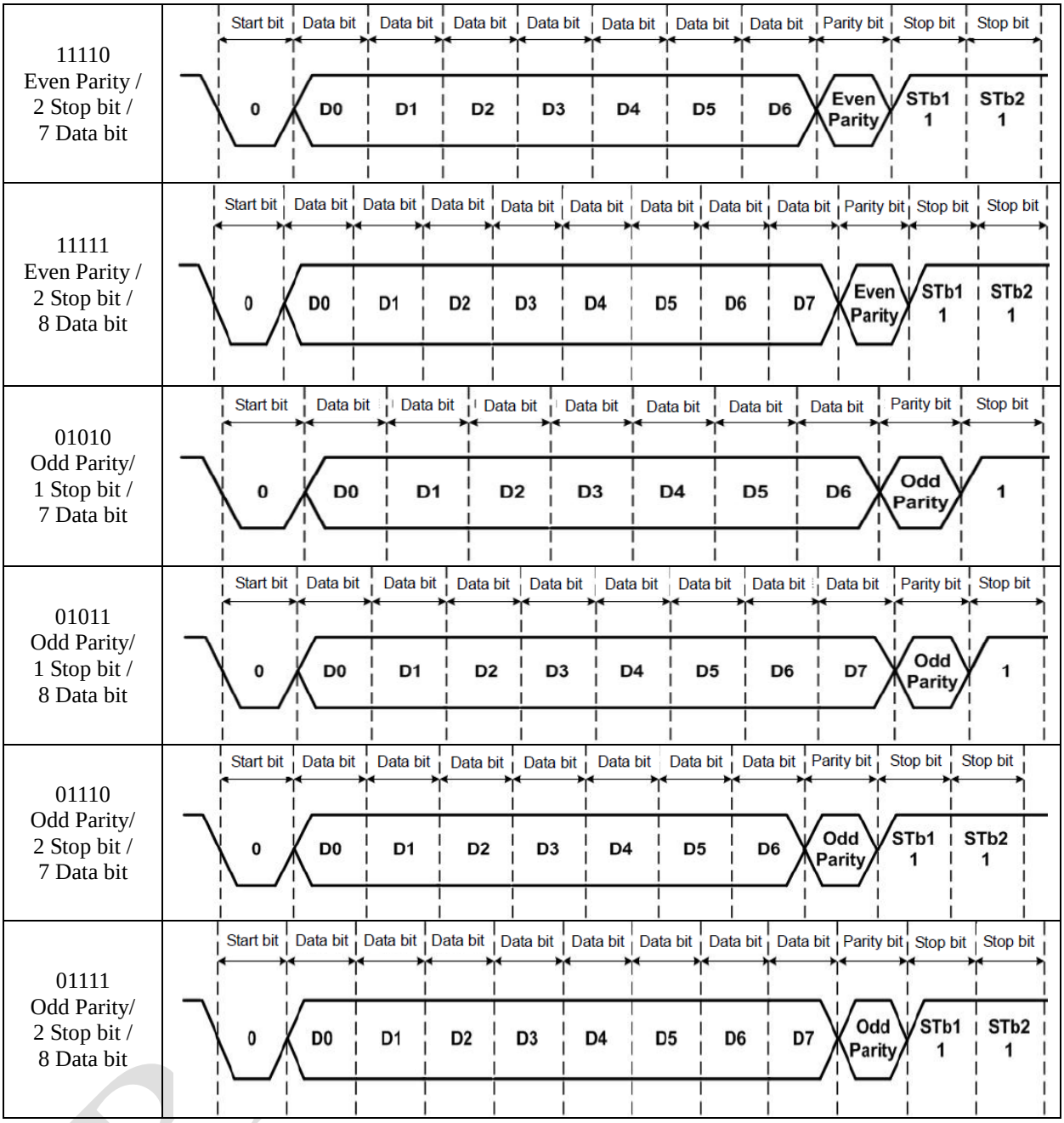


Figure 20-2 UART LCR Register Setting and Serial Data Format

20.3.2 UART Baud Rate

TX/RX Baud Rate can be calculated from the following equation.

$$UART\ \ Baud\ \ Rate = \frac{f_{PCLK}}{16\ \times\ UDL}$$

UART Divisor Latch Value (UDL) = UDLM[7:0] << 8 + UDLL[7:0]

Table 20-1 UART Baud Rate

f_{PCLK} (MHz)		1.024	2.048	5.6448	11.2896	24.0	48.0
2400 bps	UDL	27	53	147	294	625	1250
	ERR(%)	1.23	0.63	0.00	0.00	0.00	0.00
4800 bps	UDL	-	27	74	147	313	625
	ERR(%)	-	1.23	0.68	0.00	0.16	0.00
9600 bps	UDL	-	-	37	74	156	313
	ERR(%)	-	-	0.68	0.68	0.16	0.16
14400 bps	UDL	-	9	25	49	104	208
	ERR(%)	-	1.23	2.00	0.00	0.16	0.16
19200 bps	UDL	-	-	18	37	78	156
	ERR(%)	-	-	2.08	0.68	0.16	0.16
38400 bps	UDL	-	-	9	18	39	78
	ERR(%)	-	-	2.08	2.08	0.16	0.16
57600 bps	UDL	-	-	6	12	26	52
	ERR(%)	-	-	2.08	2.08	0.16	0.16
115200bps	UDL	-	-	3	6	13	26
	ERR(%)	-	-	2.08	2.08	0.16	0.16

*** UART is assumed to be unreliable when ERR is higher than 2.2%.

20.4 Register Summery

Table 20-2 UART Register Summery

Bit No.	DLAB = 0 0x00	DLAB = 0 0x00	DLAB = 0 0x04	DLAB = 0 0x08	DLAB = X 0x08	DLAB = X 0x0C	DLAB = X 0x14	DLAB = 1 0x00	DLAB = 1 0x04
	Receiver Buffer Register	Transmitter Holding Register	Interrupt Enable Register	Interrupt Ident. Register	FIFO Control Register	Line Control Register	Line Status Register	Divisor Latch (LSB)	Divisor Latch (MSB)
	RBR	THR	IER	IIR	FCR	LCR	LSR	DLL	DLM
	R	R/W	R/W	R	R/W	R/W	R	R/W	R/W
0	Data Bit 0	Data Bit 0	Enable Received Data Available Interrupt	"0" if Interrupt Pending	FIFO Enable	Word Length Select Bit 0	Data Ready	Bit 0	Bit 0
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt	Interrupt ID Bit 0	RCVR FIFO Reset	Word Length Select Bit 1	Overrun Error	Bit 1	Bit 1
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt	Interrupt ID Bit 1	XMIT FIFO Reset	Number of Stop Bits	Parity Error	Bit 2	Bit 2
3	Data Bit 3	Data Bit 3	0	Interrupt ID Bit 2	0	Parity Enable	Framing Error	Bit 3	Bit 3
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select	Break Interrupt	Bit 4	Bit 4
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	Transmitter Holding Register	Bit 5	Bit 5
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled	RCVR Trigger(LSB)	Set Break	Transmitter Empty	Bit 6	Bit 6
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled	RCVR Trigger(MSB)	Divisor Latch Access Bit (DLAB)	Error in RCVR FIFO	Bit 7	Bit 7

* DLAB = LCR[7](Divisor Latch Access Bit)
* FIFO Control Register :
  - DLAB = 0 : Register Write
  - DLAB = 1 : Register Read
* Address 0x10(0x30), 0x18(0x38), 0x1C(0x3C) are reserved for compatibility with 16550 UART standard..

20.5 Register Description

20.5.1 UART Channel Receiver Buffer Registers (UxRB)

Address : 0x8002_0800 / 0x8002_0820 / 0x8002_0840 / 0x8002_0860 / 0x8002_0880

Bit	R/W	Description	Default Value
31: 8	R	Reserved.	-
7 : 0	R	Receive Buffer Data	-

*** Accessible when DLAB is "0".

20.5.2 UART Channel Transmitter Holding Registers (UxTH)

Address : 0x8002_0800 / 0x8002_0820 / 0x8002_0840 / 0x8002_0860 / 0x8002_0880

Bit	R/W	Description	Default Value
31: 8	W	Reserved.	-
7 : 0	W	Transmit Holding Data	-

*** Accessible when DLAB is "0".

20.5.3 UART Channel Interrupt Enable Registers (UxIE)

Address : 0x8002_0804 / 0x8002_0824 / 0x8002_0844 / 0x8002_0864 / 0x8002_0884

Bit	R/W	Description	Default Value
31: 3	R	Reserved.	-
2	RW	RLSIEN : Receiver Line Status Interrupt Enable bit 0 : Disable 1 : Enable	0
1	RW	THEIEN : Transmitter Holding Empty Interrupt Enable bit 0 : Disable 1 : Enable	0
0	RW	RDAIEN : Received Data Available Interrupt Enable bit 0 : Disable 1 : Enable	0

*** Accessible when DLAB is "0".

20.5.4 UART Channel Interrupt Identification Register (UxII)

Address : 0x8002_0808 / 0x8002_0828 / 0x8002_0848 / 0x8002_0868 / 0x8002_0888

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7 : 6	R	FIFOST : FIFOs Enabled Status bit. 00 : not in FIFO mode 11 : FIFO mode	00
5 : 4	R	Reserved	0
3 : 0	R	INTID : UART Interrupt ID (Note, UART Interrupt Control Function)	0001

*** Accessible in read mode only when DLAB is "0".

Table 20-3 UART Interrupt Control Function

Interrupt Identification Register				Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Condition
Bit 3	Bit 2	Bit 1	Bit 0				
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available or Trigger Level Reached	Reading the Receiver Buffer Register or the FIFO Drops Below the Trigger Level
1	1	0	0	Second	Character Timeout Indication	No Characters have been removed from or input to the RCVR FIFO during the last 4 Char. times, and there is at least 1 Char. in it during this Time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register

20.5.5 UART Channel FIFO Control Register (UxFC)

Address : 0x8002_0808 / 0x8002_0828 / 0x8002_0848 / 0x8002_0868 / 0x8002_0888

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7 : 6	RW	RFTL : Receiver FIFO Trigger Level 00 : 1 Byte 01 : 4 Byte 10: 8 Byte 11 : 14 Byte	00
5 : 3	R	Reserved	-
2	RW	XFR : XMIT FIFO Reset All data in XMIT FIFO is reset when XFR is “1”. However, data is shift register isn’t reset.	0
1	RW	RFR : RCVR FIFO Reset All data in RCVR FIFO is reset when RFR is “1”. However, data is shift register isn’t reset.	0
0	RW	FIFOEN : FIFO Enable Bit 0 : 16450 UART Mode 1 : Enables FIFO	0

*** DLAB = “0” ➔ write mode, DLAB =”1” ➔ read mode.

20.5.6 UART Channel Line Control Register (UxLC)

Address : 0x8002_080C / 0x8002_082C / 0x8002_084C / 0x8002_086C / 0x8002_088C

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7	RW	DLAB : Divisor Latch Access Bit When this bit is "1", divisor latch register can be read/written and FIFO control register can be read.	0
6	RW	SB : Set Break When this bit is "1", serial data output pin outputs logic "0". SB doesn't affect internal transmitter logic. It only affects serial output.	0
5	RW	SP : Stick Parity 0 : Disables Stick Parity 1 : PEN, EPS, and SP are "1" ➔ Parity bit="0" PEN and SP are "1", EPS is "0" ➔ Parity bit="1"	0
4	RW	EPS : Even Parity Select 0 : Select Odd Parity 1 : Select Even Parity	0
3	RW	PEN : Parity Enable Bit 0 : Disables Parity 1 : Enables Parity	0
2	RW	STB : Number of Stop Bit 0 : 1 Stop bit 1 : 2 Stop bits (If WLS bit is set to 00(=5bits/character), it will be 1.5 instead of 2	0
1 : 0	RW	WLS : Word Length Select 00 : 5 Bits/Character 01 : 6 Bits/Character 10 : 7 Bits/Character 11 : 8 Bits/Character	00

20.5.7 UART Channel Line Status Register (UxLS)

Address : 0x8002_0814 / 0x8002_0834 / 0x8002_0854 / 0x8002_0874 / 0x8002_0894

Bit	R/W	Description	Default Value
31 : 8	R	Reserved.	-
7	R	EIRF : Error in RCVR FIFO If not in FIFO mode, EIRF is always "0". In FIFO mode, EIRF become "1" if any of OE, PE, FE, or BI of RCVR FIFO is set "1". EIRF is cleared (="0") when LSR register is read and FIFO doesn't have consecutive errors.	0
6	R	TEMP : Transmitter Empty If not in FIFO mode, TEMT become "1" when both transmitter holding register (THR) and Transmitter shift register (TSR) are empty. If either of THR or TSR has data, it is cleared. In FIFO mode, it is set when both of transmitter FIFO and TSR are empty.	1
5	R	THRE : Transmitter Holding Register Empty If not in FIFO mode, THRE is set when THR become empty by transmitting data to TSR. At this moment, THR can be written new data to transmit. In FIFO mode, THRE is set when transmit FIFO is empty, and cleared when any byte is written into transmit FIFO. If both THRE interrupt (ETHREI) and THRE are "1", interrupt raises.	1
4	R	BINT : Break Interrupt : BI is set when input data is "0" during the full word transmission time. Full word transmission time is the sum	0

		of start, data, parity, and stop bit transmission time. In FIFO mode, this error applies to each byte inside FIFO, and FIFO are cleared when BI happens. This bit is cleared when CPU reads LSR.	
3	R	FERR : Framing Error FE is set when input data doesn't have valid stop bit. In FIFO mode, this error applies to each byte inside FIFO. It is cleared when CPU reads LSR.	0
2	R	PERR : Parity Error PE is set when input data doesn't coincide with parity bit chosen by LCR register. In FIFO mode, this error applies to each byte inside FIFO. It is cleared when CPU read LSR.	0
1	R	OERR : Overrun Error In not FIFO mode, OE is set when new data is written before data inside RBR is read. In FIFO mode, it is set if a new full word comes to receiver shift register (RSR) when FIFO is full. In this case, RSR is updated; however, FIFO doesn't transmit. It is cleared when CPU reads LSR.	0
0	R	DRDY : Data Ready DR is set when received data is written on RBR or FIFO. It is cleared when every data inside RBR or FIFO is read.	0

20.5.8 UART Channel Divisor Latch LSB Register (UxDLL)

Address : 0x8002_0800 / 0x8002_0820 / 0x8002_0840 / 0x8002_0860 / 0x8002_0880

Bit	*R/W*	*Description*	*Default Value*
31: 8	R	Reserved.	-
7 : 0	RW	Divisor Latch Least Significant Byte	0x00

*** Accessible when DLAB is "1".

20.5.9 UART Channel Divisor Latch MSB Register (UxDLM)

Address : 0x8002_0804 / 0x8002_0824 / 0x8002_0844 / 0x8002_0864 / 0x8002_0884

Bit	*R/W*	*Description*	*Default Value*
31: 8	R	Reserved.	-
7 : 0	RW	Divisor Latch Most Significant Byte	0x00

*** Accessible when DLAB is "1".

20.5.10 UART IrDA Mode Register (UxIRM)

Address : 0x8002_0898

Bit	*R/W*	*Description*	*Default Value*
31: 6	R	Reserved.	-
5	RW	IrDA Rx Polarity Inversion	0
4	RW	IrDA Rx Decoding Enable 0 : Not decoding 1 : decoding the IR Frame	0
3 : 2	R	Reserved	00
1	RW	IrDA Tx Polarity Inversion	0
0	RW	IrDA Tx Encoding Enable 0 : not encoding 1 : encoding the UART frame	0

21 USB HOST CONTROLLER (*TBD)

*Notice. TBD means "To be determined"

USB 1.1 Host Controller of *adStar* supports OpenHCI(ver1.0a).

21.1 Features

- OpenHCI1.0 compatible
- USB 1.1 compatible

21.2 Operational Registers

Address	*Registers*
A0000000	HcRevision
A0000004	HcControl
A0000008	HcCommandStatus
A000000C	HcInterruptStatus
A0000010	HcInterruptEnable
A0000014	HcInterruptDisable
A0000018	HcHCCA
A000001C	HcPeriodCurrentED
A0000020	HcControlHeadED
A0000024	HcControlCurrentED
A0000028	HcBulkHeadED
A000002C	HcBulkCurrentED
A0000030	HcDoneHead
A0000034	HcFmInterval
A0000038	HcFmRemaining
A000003C	HcFmNumber
A0000040	HcPeriodicStart
A0000044	HcLSThreshold
A0000048	HcRhDescriptorA
A000004C	HcRhDescriptorB
A0000050	HcRhStatus
A0000054	Reserved.
A0000058	HcRhPortStatus[1]

Table 21-1 USB Host Registers List

22 SOUND MIXER

22.1 Features

- 4-CH. Player, 1-CH Recorder
- Re-Sampler
- Gain Controller
- 32-Depth Buffer for each channel
- 4-CH. Out (2-CH I2S, 2-CH Digital Modulator)

22.2 Block Diagram

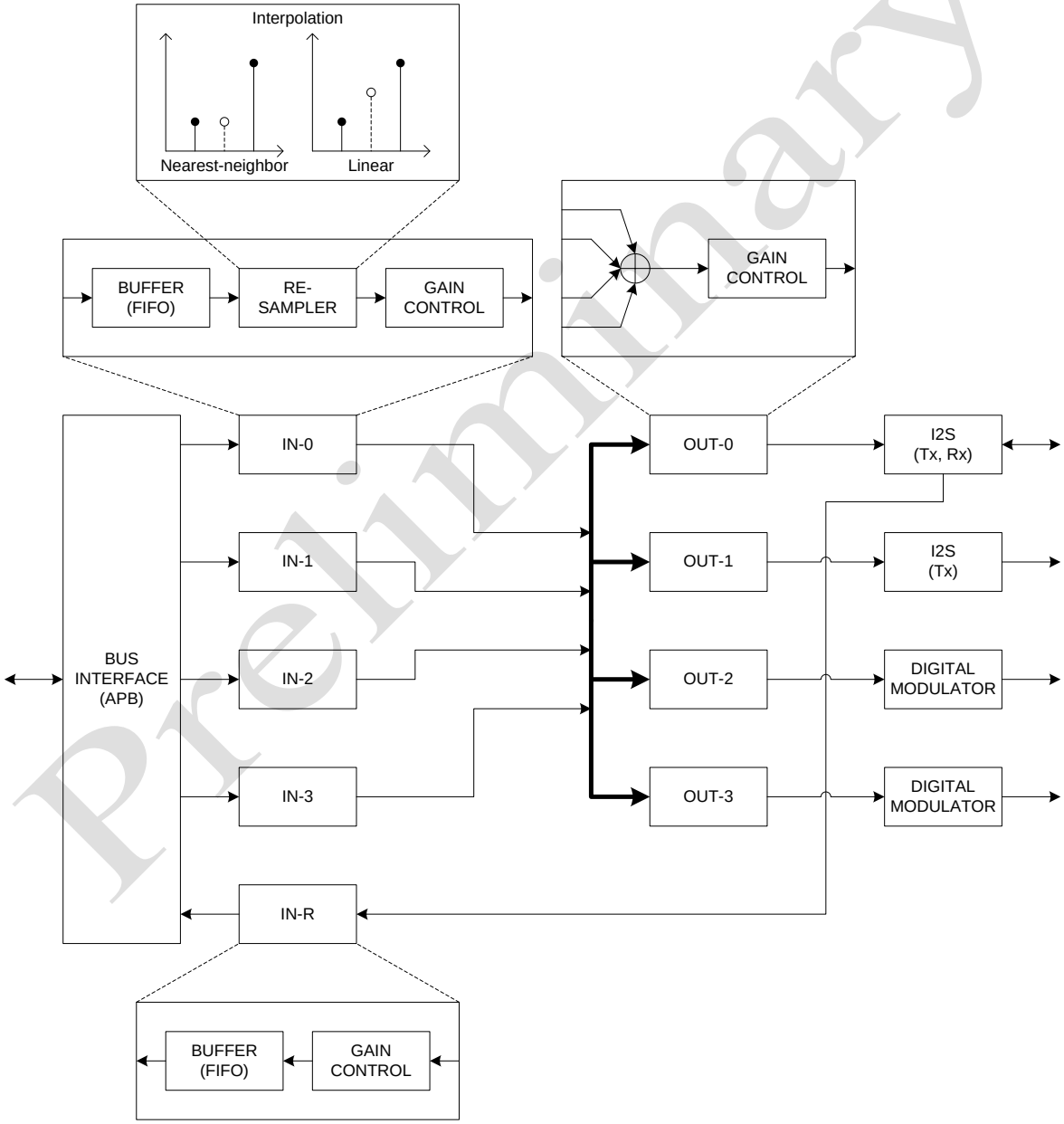


Figure 22-1 Mixer Block Diagram

22.3 Low Pass Filter for Digital Modulator

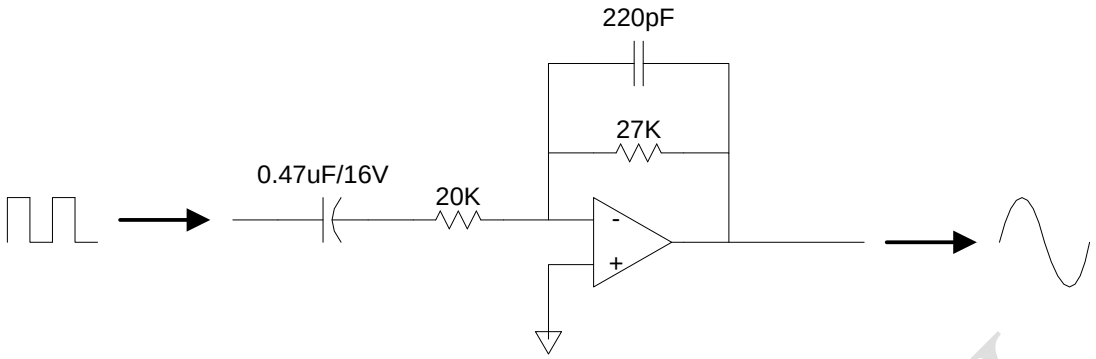


Figure 22-2 Low pass filter for digital modulator

22.4 I2S Frequency Control

SCLK, LRCK, and MCLK frequency should be configured to use I2S controller. Following table shows the relationship between MCLK and LRCK. For example, if master frequency is set 256fs for 44.1kHz, MCLK should be set 11.2896MHz. The corresponding MCLK can be configured by using pre-scaler.

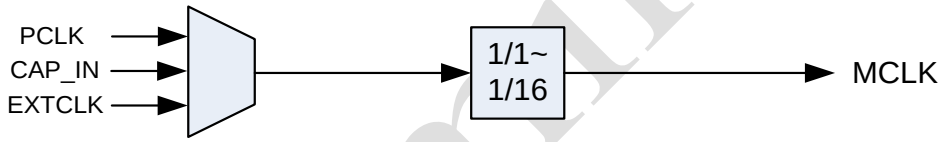


Figure 22-3 I2S Pre-Scaler

Table 22-1 I2S Sampling Frequency(LRCK) and MCLK Clock

LRCK (fs)	***8.000 KHz***	***11.025 KHz***	***16.000 KHz***	***32.000 KHz***	***44.100 KHz***	***48.000 KHz***	***96.000 KHz***
MCLK (MHz)	256fs						
	2.048	2.8224	4.096	8.1920	11.2896	12.2880	24.5760
	384fs						
	3.072	4.2336	6.144	12.2880	16.9344	18.4320	36.8640
	512fs						
	4.096	5.6448	8.192	16.3840	22.5792	24.5760	49.1520

Also, following table shows SCLK configuration

Table 22-2 I2S sampling frequency and serial bit clock

Serial bit per channel	***8bit***	***16bit***
CODEC Clock(MCLK)	Serial clock frequency(SCLK)	
256fs	16fs, 32fs, 64fs	32fs, 64fs
384fs	16fs, 32fs, 48fs, 64fs	32fs, 48fs, 64fs
512fs	16fs, 32fs, 64fs	32fs, 64fs

22.5 Register Description

22.5.1 Mixer Control Register (MIXER_ CON)

Address: 0xA002_1C00, 0xA002_1C10, 0xA002_1C20, 0xA002_1C30 (IN-0 ~ IN-3)

Bit	R/W	Description	Default Value
31 : 29	R	Reserved	-
28	R/W	Method of interpolation 0: Nearest-neighbor 1: Linear	0x0
27 : 25	R	Reserved	-
24 : 16	R/W	Step for re-sampling N = ((InFs * 256) / OutFs) – 1, (N=0~511)	0x0FF
15 : 10	R	Reserved	-
9 : 8	R/W	Out selection 00: Out-0 01: Out-1 10: Out-2 11: Out-3	0x0
7 : 4	R/W	Mode 0000: Unsigned stereo 8-bit PCM 0001: Unsigned mono 8-bit PCM 0010: Signed stereo 8-bit PCM 0011: Signed mono 8-bit PCM 0100: Unsigned stereo 16-bit PCM 0101: Unsigned mono 16-bit PCM 0110: Signed stereo 16-bit PCM 0111: Signed mono 16-bit PCM 1xxx: Reserved	0x0
3	R/W	DMA request 0: Disable 1: Enable	0x0
2	R/W	Interrupt 0: Disable 1: Enable	0x0
1	R/W	L/R swap 0: Disable 1: Enable	0x0
0	R/W	Active 0: Disable 1: Enable	0x0

Address: 0xA002_1C70 (IN-R)

Bit	R/W	Description	Default Value
31 : 2	R	Reserved	-
3	R/W	DMA request 0: Disable 1: Enable	0x0
2	R/W	Interrupt 0: Disable 1: Enable	0x0
1	R/W	Reserved	-
0	R/W	Active 0: Disable 1: Enable	0x0

Address: 0xA002_1C80, 0xA002_1C90, 0xA002_1CA0, 0xA002_1CB0 (OUT-0 ~ OUT-3)

Bit	R/W	Description	Default Value
31 : 1	R	Reserved	-
0	R/W	Active 0: Disable 1: Enable	0x0

22.5.2 Mixer Volume Register (MIXER_VOL)

Address: 0xA002_1C04, 0xA002_1C14, 0xA002_1C24, 0xA002_1C34, 0xA002_1C74, 0xA002_1C84, 0xA002_1C94, 0xA002_1CA4, 0xA002_1CB4
(IN-0 ~ IN-3, IN-R, OUT-0 ~ OUT-3)

Bit	R/W	Description	Default Value
31 : 16	R	Reserved	-
15 : 8	R/W	Right gain (±0.5dB) 0xFF(0dB) ~ 0x80(-63.5dB), 0x7F~0x0(-∞dB)	0xFF
7 : 0	R/W	Left gain (±0.5dB) 0xFF(0dB) ~ 0x80(-63.5dB), 0x7F~0x0(-∞dB)	0xFF

22.5.3 Mixer Buffer Status Register (MIXER_BST)

Address: 0xA002_1C08, 0xA002_1C18, 0xA002_1C28, 0xA002_1C38, 0xA002_1C78
(IN-0 ~ IN-3, IN-R)

Bit	R/W	Description	Default Value
31 : 6	R	Reserved	-
5 : 0	R	Buffer count value 0(Empty) ~ 32(Full)	0x0

22.5.4 Mixer Data Register (MIXER_DAT)

Address: 0xA002_1C0C, 0xA002_1C1C, 0xA002_1C2C, 0xA002_1C3C, 0xA002_1C7C
(IN-0 ~ IN-3, IN-R)

Bit	R/W	Description	Default Value
31 : 0	R/W	PCM data	-

22.5.5 Mixer Out Register (MIXER_OUT)

Address: 0xA002_1C8C, 0xA002_1C9C (OUT-0, OUT1)

Bit	R/W	Description	Default Value
31 : 6	R/W	Reserved	-
5	R/W	Left of LRCK signal 0: High 1: Low	0x0
4	R/W	Format 0: I2S-bus 1: MSB(Left)-justified	0x0
3 : 2	R/W	MCLK frequency 00: 256fs 01: 384fs 10: 512fs 11: Reserved	0x0
1 : 0	R/W	SCLK frequency 00: 16fs 01: 32fs 10: 48fs 11: 64fs	0x0

Address: 0xA002_1CAC, 0xA002_1CBC (OUT-2, OUT3)

Bit	R/W	Description	Default Value
31 : 10	R/W	Reserved	-
9 : 8	R/W	Step for over-sampling 00: x1 01: x2 10: x4 11: x8	0x0
7 : 4	R/W	Sine wave generation (For test) 0000: Disable otherwise: Enable	0x0
3 : 2	R/W	PWM modulation 00: Class-AD single side modulation 01: Class-AD double side modulation 10: Class-BD single side modulation 11: Class-BD double side modulation	0x0
1 : 0	R/W	Noise transfer function 00: Disable 01: 4^{th}-order FIR filter 10: 5^{th}-order FIR filter 11: 5^{th}-order optimal FIR filter	0x0

22.5.6 Mixer Interrupt Status Register (MIX_IST)

Address: 0xA002_1CC0

Bit	R/W	Description	Default Value
31 : 8	R	Reserved	-
7	R	IN-R interrupt	0x0
6 : 4	R	Reserved	-
3	R	IN-3 interrupt	0x0
2	R	IN-2 interrupt	0x0
1	R	IN-1 interrupt	0x0
0	R	IN-0 interrupt	0x0

23 ADC CONTROLLER

adStar includes 1MSPS 10-bit SAR ADC. Recommended operation frequency is 12MHz. Conversion cycle is 13 cycles of ADC input clock.

23.1 Features

- Various SOC source select
- Continuous Mode support
- 4-depth FIFO
- DMA Mode (in FIFO Mode)
- 4 channel input

23.2 Register Description

23.2.1 ADC Control Register (ADCCTRL)

Address : 0xA002_3800

Bit	R/W	Description	Default Value
15 : 12	R	Reserved	-
11	R/W	Periodic Mode Selection 0: Normal Operation Mode (1 pulse SOC Generation) 1: Periodic Mode (Continuous SOC Generation)	0
10	R/W	DMA Last Transfer If it is set in FIFO and DMA mode, it initiates DMA last request, and cleared after the initiation.	0
9	R/W	DMA Mode Enable If it is set in FIFO mode, it requests DMA transfer until FIFO is full. It is cleared when DMA last request happens.	0
8	R/W	FIFO Mode 1: Using FIFO 0: NOT using FIFO	0
7	R	Reserved	
6 : 5	R/W	ADC Channel Selection 000: ADCIN0 001: ADCIN1 010: ADCIN2 011: ADCIN3	00
4 : 2	R/W	ADC Source clock selection 000: APB Clock / 2 001: APB Clock / 4 010: APB Clock / 8 011: APB Clock / 16 100: APB Clock / 32 101: APB Clock / 64 110: APB Clock / 128 111: APB Clock / 256 * Sampling period is as long as twelve times the period of ADC source clock.	00
1	R/W	ADC Start Conversion(STC) SOC happens when it is set. Cleared after one period of ADC clock.	0
0	R/W	ADC Enable 0: ADC Disable 1: ADC Enable	0

23.2.2 ADC Data Register (ADCDATA)

Address: 0xA002_3804

Bit	R/W	Description	Default Value
31 : 10	R	Reserved	-
9 : 0	R/W	10-bit ADC data	0x000

23.2.3 ADC FIFO Register (ADCFIFO)

Address: 0xA002_3808

Bit	R/W	Description	Default Value
31 : 10	R	Reserved	-
9 : 0	R/W	In case of ADC FIFO Mode 10-bit ADC FIFO Data	0

23.2.4 ADC Status Register (ADCSTAT)

Address : 0xA002_380C

Bit	R/W	Description	Default Value
31 : 7	R	Reserved	-
6	R	FIFO Overflow "1" represents FIFO is overflowed. If new data arrive in overflowed status, old data are deleted and new data are stored inside FIFO.	0
5	R	FIFO Full 1: FIFO is Full 0: FIFO is not Full	0
4	R	FIFO Empty 1: FIFO is Empty 0: FIFO is not empty	1
3 : 1	R	FIFO Level (0~4)	0
0	R	ADC Data Ready 1: ADC Data is valid 0: ADC Data is not ready	0

24 ELECTRICAL CHARACTERISTIC

24.1 DC Electrical Characteristic

The ESD of VeriSilicon CSMC 0.18μm 1.8/3.3V I/O Cell Library meets HBM-2KV and MM-200V.

The following table summarizes the electrical design specifications of DC specifications:

Table 24-1 I/O DC Electrical Characteristic

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High level output voltage	V_{OH}	I_{OH} = -8mA	2.4			V
Low level output voltage	V_{OL}	I_{OL} = 8mA			0.4	V
High level input voltage	V_{IH}	LVTTL/CMOS interface	2.0		IOVDD + 0.5	V
Low level Input voltage	V_{IL}	LVTTL/CMOS interface			0.8	V
Switch threshold	V_{th}	CMOS interface	1.2	1.3	1.4	V
		Schmitt-falling-trigger	0.8	0.9	1.0	V
		Schmitt-rising-trigger	1.45	1.55	1.65	V
Hysteresis	⊓	Schmitt-trigger interface	0.55	0.65	0.7	V
Input pull-up resistance	R_{PU}	V_{IN} = 0	34	41	64	kΩ
Input pull-down resistance	R_{PD}	V_{IN} = VDDH	33	44	79	kΩ
Input current	I_I	Vdd = MAX, 0V £ Vin £ 3.6V	-10		10	μA
Input current with pull down		Vin = Vdd	40		160	μA
Input current with pull up		Vin = 0	-160		40	μA

24.2 Operating Conditions

The following table gives the recommended operating conditions for the integrated circuit (IC) chips using this library:

Table 24-2 I/O Recommended Operating Conditions

Operating Conditoins	Min	Typ	Max
Core DC Supply (CoreVDD)	1.62V	1.8V	1.98V
I/O DC Supply Voltage (IOVDD)	3.0V	3.3V	3.6V

24.3 LDO Electrical Specification

Table 24-3 LDO Electrical Specifications
(VDD33=3.3V, COUT=1uF, TA=25˚C unless otherwise noted)

Parameters	Symbol	Test Condition	Min	Typ	Max	Units
Quiescent Current	Iq	Iout = 0 PD = 0		35		uA
Shutdown Current	Isd	PD = VDD33			1	uA
Input Voltage	VDD33		VDD18+ Vdrp		3.6	V
Output Voltage	VDD18	Iout = 0	1.8-3%		1.8+ 3%	V
Output Ripple		Iout = 10~100mA		40		mV
Wake up Time				10		us
Band Gap Output	VBG			1.2		V
External Capacitor				1		uF
Line Regulation		VDD33=2.8~3.8V Iout=10mA		0.16		%
		VDD33=2.8~3.8V Iout=100mA		0.63		
Dropout Voltage	Vdrp	Iout=100mA		290		mV
Ripple Rejection	PSRR	Iout=10mA Without bypass Cap (1kHz)		60		db
		Iout=100mA Without bypass Cap (1kHz)		40		
		Iout=100mA With bypass Cap (1kHz)		69		
Output Current	Iout			100		mA
PD Logic input High	ViH		1.2			V
PD Logic input Low	ViL				0.6	V
VDD18 Temperature Coefficient	TC	25~150˚C		-80		ppm

24.4 POR Electrical Specification

Table 24-4 POR Specification (Unless otherwise specified, Topr=25˚C, VDD=1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VDD	Supply voltage		1.6	1.8	2	V
Is	Supply current	VDD=1.8V		3	5	uA
Vtd	Minimum power up trigger level		1			V
Vtdr	Maximum power drop trigger level				0.9	V
Tr	Rising time of VDD		10u		10m	s
Tf	Falling time of VDD to VTH-100Mv (0.9V)		5			us
Td	Reset delay time after VTH trigger	Tr=80us		20		us
VOH	POR output high voltage	No load		VDD		V
		Isource=30uA, VDD≥1V		0.8*VDD		V
		Isource=100uA , VDD≥1.8V		0.8*VDD		V
VOL	POR output low voltage	No load		GND		V

24.5 PLL Electrical Specification

Table 24-5 PLL DC Characteristics (Unless otherwise specified, Topr=25˚C, VDD=1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
AVDD	Supply Voltage		1.6	1.8	2	V
DVDD	Digital Supply Voltage		1.6	1.8	2	V
Is	Supply Current	normal		5		mA
VIH	Input High Voltage		DVDD-0.3			V
VIL	Input Low Voltage				DGND+ 0.3	V

Table 24-6 PLL Input Frequency (Unless otherwise specified, Topr=25˚C, VDD=1.8V)

Symbol	Parameter	Min	Typ	Max	Unit
Fin	Input Frequency	1		16	Mhz

24.6 ADC Electrical Specification

Table 24-7 ADC Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
AVDD	Analog Supply Voltage	3	3.3	3.6	V
DVDD	Digital Supply Voltage	1.6	1.8	2	V
IR	Input Voltage	0		AVDD	

Table 24-8 ADC DC Characteristics (Unless otherwise specified, Topr=25˚C, VDD=1.8V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIH	Input High Voltage		1.5			V
VIL	Input Low Voltage				0.8	V
PWR	Power Consumption (AVG)	Normal		0.9		mA
		Power Down		1		uA

24.7 Power Consumption

Table 24-9 Power Consumption from different conditions

Condition	Freq.	Typ.
CPU running from flash LCD displaying and Sound playing from NAND Flash file system	101Mhz	512.7mW
	108Mhz	525.3mW
CPU running from flash	96Mhz	341mW

25 PACKAGE DIMENSION

Unit: mm

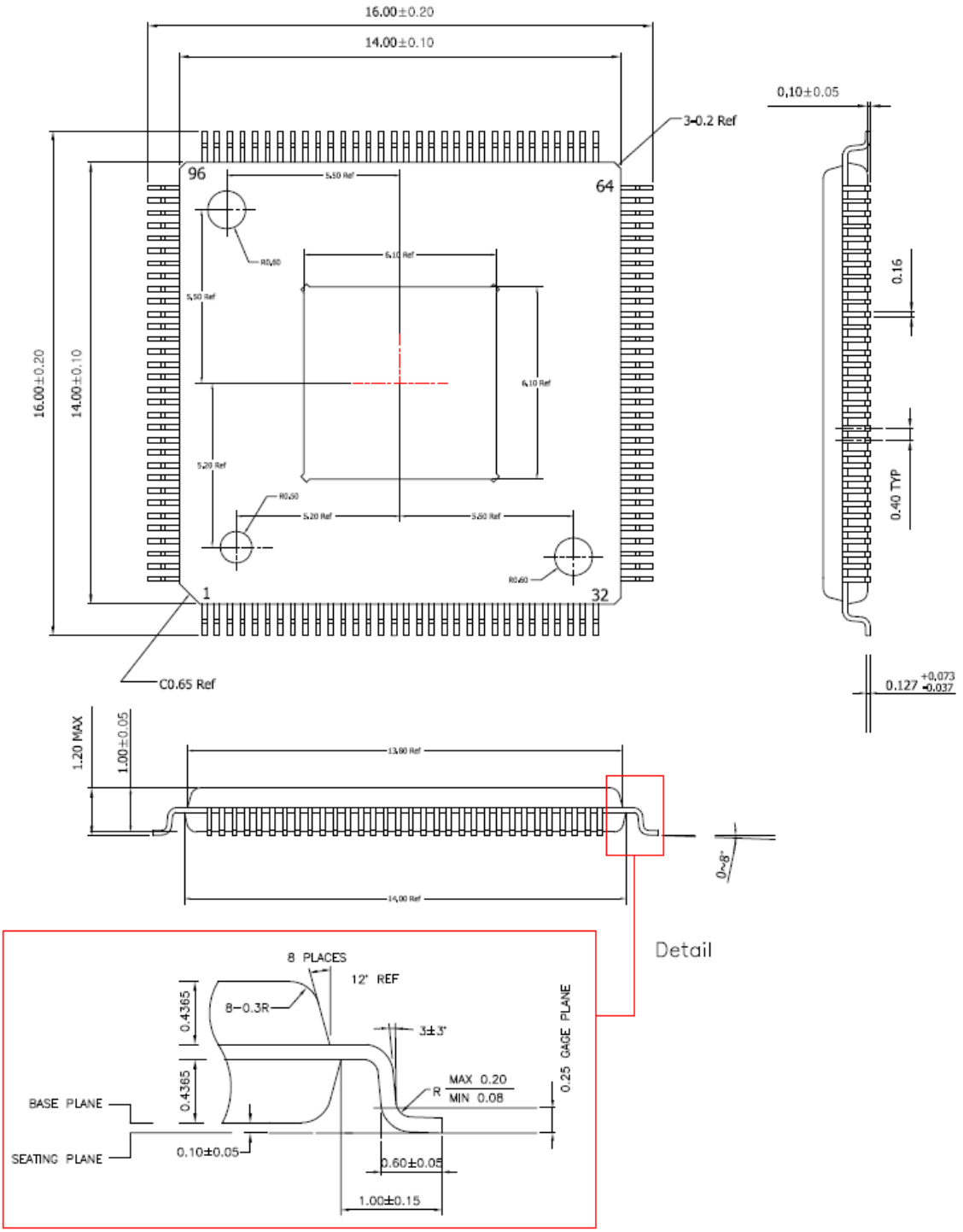


Figure 25-1 Package Dimension